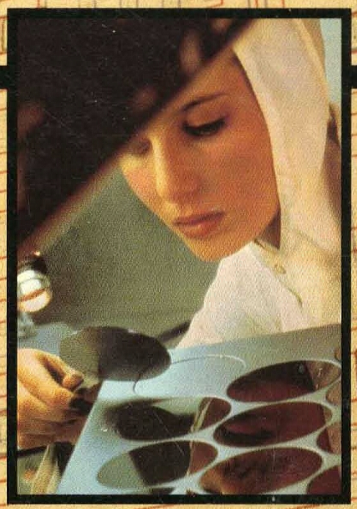
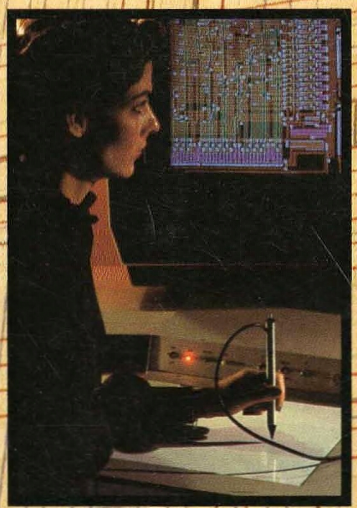
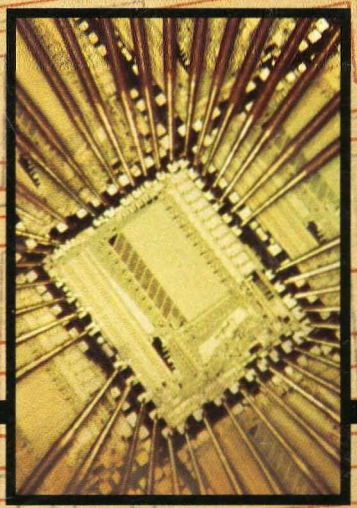
Microelectronics Data Catalog







GENERAL INSTRUMENT

GENERAL INSTRUMENT

Microelectronics Data Catalog

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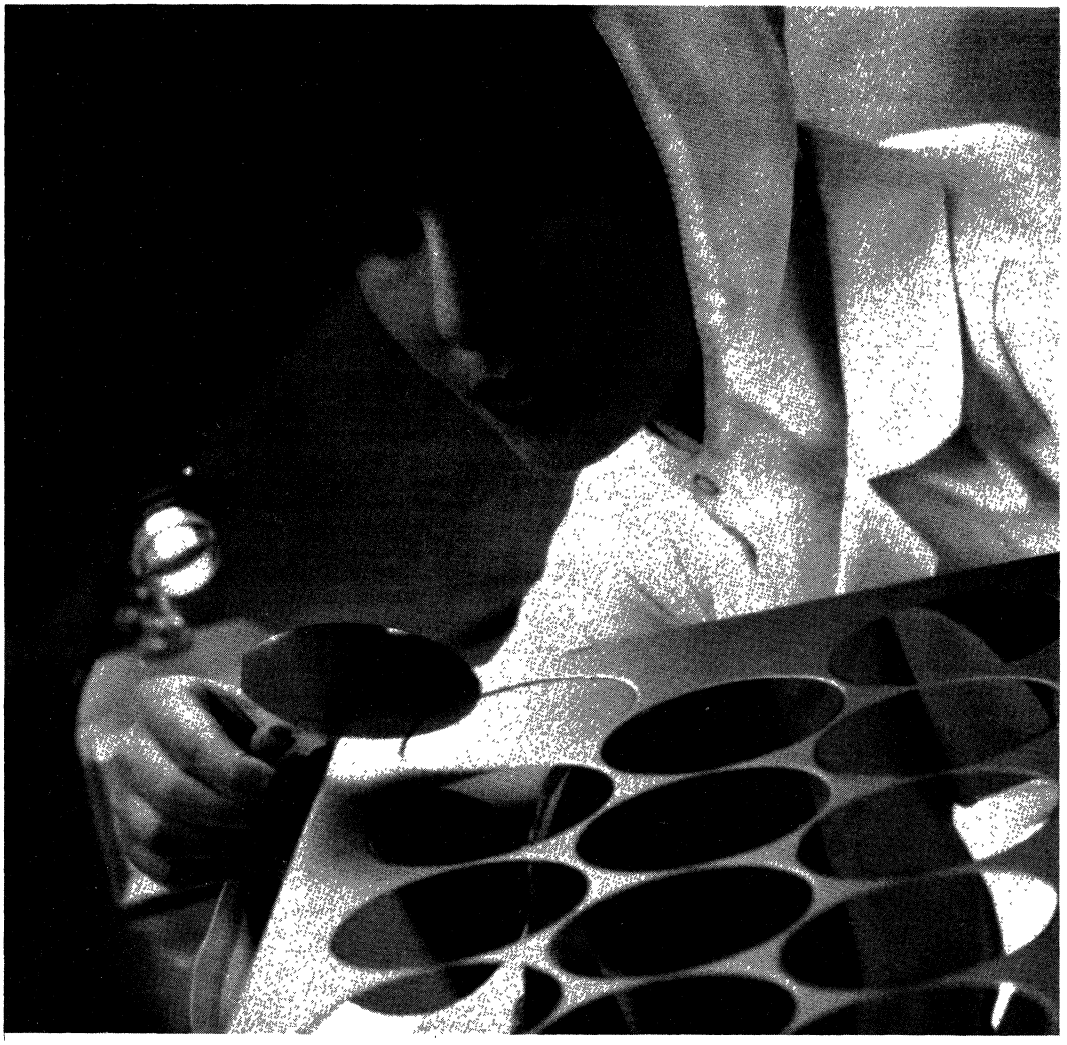

PART NUMBER INDEX

ROM 2

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
		Read Only Memories	
16K ROM	16,384 bits organized 2048 x 8	RO-3-9316A/B/C	2-4
		RO-3-9316HR	2-4
32K ROM	32,768 bits organized 4096 x 8	RO-3-9332A/B/C	2-7
		RO-3-9332HR	2-7
		RO-3-9333B/C	2-10
		RO-3-9333HR	2-10
		RO9432B/C/D	2-12
		RO9433B/C/D	2-14
64K ROM	65,536 bits organized 8192 x 8	RO-3-9364B/C	2-16
		RO-3-9364HR	2-16
		RO-3-9365B/C	2-19
		RO9464B/C/D	2-22
		RO9464AB/AC/AD	2-22
		RO9864B/C/D	2-25
		RO9864AB/AC/AD	2-25
128K ROM	131,072 bits organized 16,384 x 8	RO9128B/C/D	2-28
256K ROM	262,144 bits organized 32,768 x 8	RO9256	2-31
20K CARTRIDGE ROM	20,480 bits organized 2048 x 10	RO-3-9504	2-32
40K CARTRIDGE ROM	40,960 bits organized 4096 x 10	RO9508	2-34
80K CARTRIDGE ROM	81,920 bits organized 8192 x 10	RO9580	2-37
160K CARTRIDGE ROM	163,840 bits organized 16,384 x 10	RO9160	2-39
		Keyboard Encoder	
CAPACITIVE KEYBOARD ENCODER	4,592 bits organized as 112 keys x 4 modes x 10 bits, plus 112 bits for internal programing of function keys	AY-3-4592	2-42
		Character Generators	
CHARACTER GENERATOR	2,560 bits organized a 64-5 x 8 characters	RO-3-2513	2-54
	16,384 bits organized as 2048-8 bit words	RO-3-9316CGII	2-59
		Speech ROMs	
SERIAL SPEECH ROM	16,384 bits organized 2048 x 8	SPR016	2-64
	32,768 bits organized 4096 x 8	SPR032	2-70
	131,072 bits organized 16K x 8	SPR128	2-73

EANVM 3

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
		Electrically Alterable Non-Volatile Memory	
82 BIT EAROM	82 bits organized 82 x 1	ER0082	3-5
700 BIT SERIAL EAROM	700 bits organized 50 x 14	ER1451	3-8
1400 BIT SERIAL EAROM	1400 bits organized 100 x 14	ER1400	3-11
512 BIT EAROM	512 bits organized 32 x 16	ER2051	3-14
		ER2051IR	3-14
		ER2051HR	3-14
512 BIT EAROM	512 bits organized 64 x 8	ER2055	3-17
		ER2055IR	3-17
		ER2055HR	3-17
1K N-CHANNEL EEPROM	1K bits organized 128 x 8	ER5901	3-20
		ER5901IR	3-20
		ER5901HR	3-20
4096 BIT EAROM	4096 bits organized 1024 x 4	ER3400	3-22
		ER3400I/IR	3-22
		ER3400HR	3-22
8192 BIT EAROM	8192 bits organized 2048 x 4	ER2810IR	3-28
		ER2810HR	3-28
16K N-CHANNEL EEPROM	16K bits organized 2048 x 8	ER5716	3-32
		ER5716IR	3-32
		ER5716HR	3-32
WORD ALTERABLE 16K BIT EEPROM	Electrically word alterable 16K bits organized 2048 x 8, 5V operation in read mode	ER5816	3-36
		ER5816IR	3-36
		ER5816HR	3-36
WORD ALTERABLE 16K BIT EEPROM	Electrically word alterable 16K bits organized 2048 x 8, 5V operation in all modes	ER5916	3-41
		ER5916IR	3-41
		ER5916HR	3-41
		Non-Volatile Static RAM	
4K N-CHANNEL NON-VOLATILE STATIC RAM	4K bits organized 512 x 8	ER5304	3-48

Microcomputer 4

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			PIC Series
8 BIT MICROCOMPUTER	The PIC1650 series of microcomputers contain RAM I/O and a central processing unit as well as a customer defined ROM to specify overall functional characteristics of the device	PIC1650A	4-4
		PIC1650XT	4-16
		PIC1654	4-28
		PIC1655A	4-38
		PIC1655XT	4-50
		PIC16C55	4-62
		PIC1656	4-72
		PIC1670	4-85
			PIC Development Series
8 BIT DEVELOPMENT MICROCOMPUTER	PIC microcomputer without ROM and with addition of a HALT pin.	PIC1664	4-96
		PIC16C63	4-110
		PIC1665	4-121
			PICAL/PICES II
PIC ASSEMBLER	Converts symbolic source programs for PIC series into object code	PICAL	4-132
PIC DEVELOPMENT SYSTEM	In-circuit emulation and debug system—stand alone or peripheral.	PICES II	4-134
			PIC Field Demo Systems
PIC FIELD DEMO SYSTEMS	Contains PIC microcomputer, PROMs and provisions for on-board RC oscillator or external clock	PFD Systems	4-138

Audio 5

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			Speech Synthesis
NARRATOR™ SPEECH PROCESSOR	Natural speech, stand alone operation, wide operating voltage, expandable ROM, simple interface.	SP0256	5-5
		SP0256-AL2	5-9
		SP0232	5-9
		SPR000	5-9
VOICE SYNTHESIS MODULE	Complete speech system, 16 seconds of speech, custom vocabularies, simple interface, 5V operation	VSM2032	5-10
SPEECH SYNTHESIZER	High quality speech, programmable filter, 5V operation, simple interface, double buffered input.	SP0250	5-12
SPEECH FIELD DEVELOPMENT BOARD	5V operation, expandable EPROM, multiple speech synthesis, on-board oscillator.	SFD2000	5-15
			Sound Generation
PROGRAMMABLE SOUND GENERATOR	Full software control, 5V operation, simple interface, triple analog output, general purpose I/O ports.	AY-3-8910	5-18
		AY-3-8912	5-18
		AY-3-8913	5-18
TUNES SYNTHESIZER	Produces musical tunes from pre-programmed microcomputer	AY-3-1350	5-24

Telephony 6

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			Dialers
PUSHBUTTON TELEPHONE DIALERS	Converts pushbutton input to rotary dial pulses.	AY-5-9151A/B	6-4
		AY-5-9152/B	6-4
		AY-5-9153A/B	6-4
		AY-5-9154A	6-4
LOOP DISCONNECT DIALER	Pushbutton-rotary dial converter with re-dial.	AY-5-9158	6-11
MULTI-FREQUENCY DIALER	Dialer with dual tone.	AY-5-9559	6-14
			Multi-Frequency Generators
DUAL TONE MULTI-FREQUENCY GENERATORS	Generates DTMF/tone telephone frequencies.	AY-3-9400	6-18
		AY-3-9410	6-18
			Code Conversion
CODEC	Duplex Delta-Sigma/PCM converter.	AY-3-9900	6-22
			Programmable Dialers
PROGRAMMABLE MICRO-COMPUTER TELEPHONE DIALERS	Single chip microcomputer pre-programmed for in-telephone applications.	TZ-2001	6-30
		TZ-2002	6-30
		TZ-2003	6-30

Data Communications 7

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			UAR/T Devices
UAR/T	Complete 5-8 bit receiver/transmitter interface.	AY-3-1015D	7-4
DUAL BAUD RATE GENERATORS	16 Frequency, UART/USRT compatible.	AY-5-8116	7-13
		AY-5-8116T	7-13
		AY-5-8136	7-13
		AY-5-8136T	7-13
			Clocks
4 DIGIT CLOCK RADIO	12/24 Hour clock, 24 hour alarm, sleep timer, battery standby.	CK3300	7-18
			Appliances
DIGITAL THERMOMETER	Digital thermometer and temperature controller.	AY-3-1270	7-32
			Remote Control
REMOTE CONTROL TRANSMITTER	256 Command PCM infrared transmitter.	AY-3-8470	7-42
REMOTE CONTROL RECEIVER	256 Command PCM infrared receiver.	AY-3-8475	7-48

ULAs 8

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
Uncommitted Logic Arrays			
HIGH SPEED CMOS UNCOMMITTED LOGIC ARRAYS	Single mask, 5ns gate delay, single supply voltage, CMOS technology, on-chip power-on reset.	LA03	8-3
		LA05	8-3
		LA10	8-3
		LA15	8-3
		LA20	8-3

Video 9

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
Video Display			
TELEVIEW SYSTEM	The Teleview system is a powerful system to display information on a TV receiver. It can store data from either telephone lines or TV RF signal information.	TELEVIEW System	9-4
		PIC1650A	9-9
		PIC1650-536	9-15
		AY-3-9710	9-28
		AY-3-9735	9-33
Video Graphics			
PERSONAL TERMINAL	The 8900 system is a programable video display system, capable of detailed graphics definition and manipulation	General Information	9-42
		CP1610	9-22
		AY-3-8900	9-43
		AY-3-8900-1	9-43
		RO-3-9502	9-46
		RO-3-9503	9-49
		RO-3-9600	9-51
		RO-3-9504	9-54
		AY-3-8910	9-56
		AY-3-8912	9-56
		AY-3-8913	9-56
		AY-3-8915	9-57
Video Games			
BALL & PADDLE	Six selectable games for one or two players, with vertical paddle motion	AY-3-8500	9-60
		AY-3-8500-1	9-60
8600 SERIES	The 8600 series games consist of a set of single chip TV game integrated circuits.	General Information	9-63
ROADRACE	One or two player games where racing skill in "traffic" generates the highest score.	AY-3-8603	9-64
WARFARE	One or two player games featuring subs, destroyers, cargo ships, and spaceships.	AY-3-8605	9-65
WIPEOUT	One or two player games where players "wipe out" objects by controlling a ball in the play area.	AY-3-8606	9-66
SHOOTING GALLERY	Twelve games for one or two players using external photocell rifles for shooting.	AY-3-8607	9-68
SUPERSPORT	Ten selectable games for one or two players, with vertical and horizontal paddle motion.	AY-3-8610	9-70
MOTOR CYCLE	One player cycle game with variable skill selection.	AY-3-8765	9-72

Tuning 10

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			Television
ECONOMEGA IIA DIGITAL TUNING SYSTEM	Provides electronic control of a varactor tuned TV from keyboard entry.	AY-3-8211	10-4
FREQUENCY LOCKED LOOP TUNING SYSTEMS	Provides frequency locked loop tuning in radio, TV applications.	Economega III	10-8
PHASED LOCKED LOOP TUNING SYSTEM SYNTHESIZER	Provides PLL frequency synthesis for color TV tuning.	Economega IV	10-19
		AY-3-2012	10-22
		CT2010	10-27
		CT2017	10-29
PHASED LOCKED LOOP TV TUNING SYSTEM CONTROL	Provides control and interface for PLL television tuning	PIC1650-020	10-33
		ER1400	10-33
			Synthesizer/Counter
FREQUENCY SYNTHESIZER/ COUNTER	Provides a time base for frequency synthesizer counting.	AY-5-8105	10-44
			EAROM
512 BIT EAROM	512 bits organized 32 x 16.	ER2051	10-48
		ER2051 IR	10-48
		ER2051 HR	10-48

ROM 2

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
		Read Only Memories	
16K ROM	16,384 bits organized 2048 x 8	RO-3-9316A/B/C	2-4
		RO-3-9316HR	2-4
32K ROM	32,768 bits organized 4096 x 8	RO-3-9332A/B/C	2-7
		RO-3-9332HR	2-7
		RO-3-9333B/C	2-10
		RO-3-9333HR	2-10
		RO9432B/C/D	2-12
		RO9433B/C/D	2-14
64K ROM	65,536 bits organized 8192 x 8	RO-3-9364B/C	2-16
		RO-3-9364HR	2-16
		RO-3-9365B/C	2-19
		RO9464B/C/D	2-22
		RO9464AB/AC/AD	2-22
		RO9864B/C/D	2-25
		RO9864AB/AC/AD	2-25
128K ROM	131,072 bits organized 16,384 x 8	RO9128B/C/D	2-28
256K ROM	262,144 bits organized 32,768 x 8	RO9256	2-31
20K CARTRIDGE ROM	20,480 bits organized 2048 x 10	RO-3-9504	2-32
40K CARTRIDGE ROM	40,960 bits organized 4096 x 10	RO9508	2-34
80K CARTRIDGE ROM	81,920 bits organized 8192 x 10	RO9580	2-37
160K CARTRIDGE ROM	163,840 bits organized 16,384 x 10	RO9160	2-39
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CAPACITIVE KEYBOARD ENCODER	4,592 bits organized as 112 keys x 4 modes x 10 bits, plus 112 bits for internal programing of function keys.	AY-3-4592	2-42
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	16,384 bits organized as 2048-8 bit words	RO-3-9316CGII	2-59
		Speech ROMs	
SERIAL SPEECH ROM	16,384 bits organized 2048 x 8	SPR016	2-64
	32,768 bits organized 4096 x 8	SPR032	2-70
	131,072 bits organized 16K x 8	SPR128	2-73

GENERAL INSTRUMENT

Read Only Memories

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
16K ROM	16,384 bits organized 2048 x 8	RO-3-9316A/B/C	2-4
		RO-3-9316HR	2-4
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		RO-3-9332HR	2-7
		RO-3-9333B/C	2-10
		RO-3-9333HR	2-10
		RO9432B/C/D	2-12
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64K ROM	65,536 bits organized 8192 x 8	RO-3-9364B/C	2-16
		RO-3-9364HR	2-16
		RO-3-9365B/C	2-19
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80K CARTRIDGE ROM	81,920 bits organized 8192 x 10	RO9580	2-37
160K CARTRIDGE ROM	163,840 bits organized 16,384 x 10	RO9160	2-39

READ ONLY MEMORY

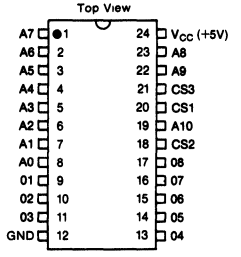
16,384 Bit Static Read Only Memory

FEATURES

- 2048 x 8 Organization — Ideal for Microprocessor Memory Systems
- Single +5 Volt Supply
- TTL Compatible — All Inputs and Outputs
- Static Operation — No Clocks Required
- 850ns Maximum Access Time: RO-3-9316A
- 450ns Maximum Access Time: RO-3-9316B
- 350ns Maximum Access Time: RO-3-9316C
- Three-State Outputs — Under the Control of Three Mask-Programable Chip Select Inputs to Simplify Memory Expansion
- Totally Automated Custom Programing
- Zener Protected Inputs
- Glass Passivation Protection
- Pin Compatible With 2716 16K EPROM

PIN CONFIGURATION

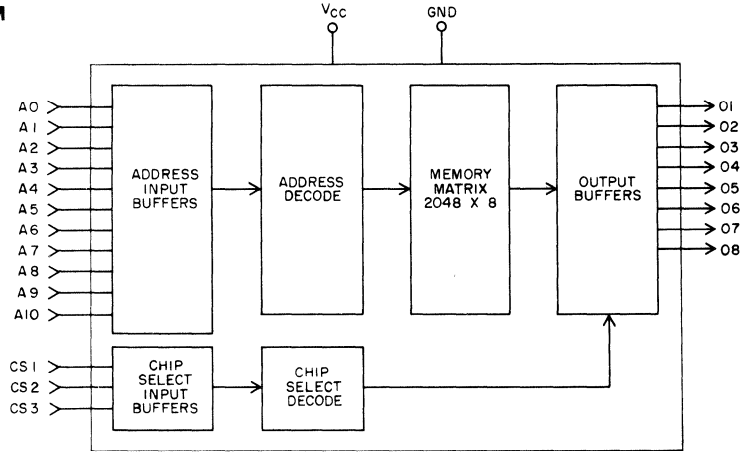
24 LEAD DUAL IN LINE



DESCRIPTION

The General Instrument RO-3-9316 is a 16,384 static Read Only Memory organized as 2048 8-bit words and is ideally suited for microprocessor memory applications. Fabricated in the General Instrument N-Channel Ion Implant process to enable operation from a single +5 Volt power supply, the RO-3-9316 offers the best combination of high performance, large bit storage and simple interfacing.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C (HR: T_A = −55°C to +125°C)
Output Loading: One TTL load, $C_{L\,TOTAL}$ = 100pf

RO-3-9316A/B/C ■ RO-3-9316HR

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select Inputs						
Logic "1"	V_{IH}	2	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = −100μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
RO-3-9316A	I_{CC}	—	50	85	mA	Outputs open
RO-3-9316B	I_{CC}	—	65	115	mA	Outputs open
RO-3-9316C	I_{CC}	—	—	125	mA	Outputs open

RO-3-9316A ■ RO-3-9316AHR

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	800	—	—	ns	
Capacitance	C_1	—	5	8	pf	F = 1MHz
	C_1	—	8	10	pf	F = 1MHz; RO-3-9316AHR only
Data Outputs						
Access Time	t_{ACC}	—	600	850	ns	
Chip Select Response Time	t_R	—	200	300	ns	
Capacitance	C_O	—	8	10	pf	F = 1MHz

RO-3-9316B ■ RO-3-9316BHR

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_1	—	5	8	pf	F = 1MHz
	C_1	—	8	10	pf	F = 1MHz; RO-3-9316BHR only
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pf	F = 1MHz

RO-3-9316C ■ RO-3-9316CHR

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	300	—	—	ns	
Capacitance	C_1	—	5	8	pf	F = 1MHz
	C_1	—	8	10	pf	F = 1MHz; RO-3-9316CHR only
Data Outputs						
Access Time	t_{ACC}	—	250	350	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pf	F = 1MHz

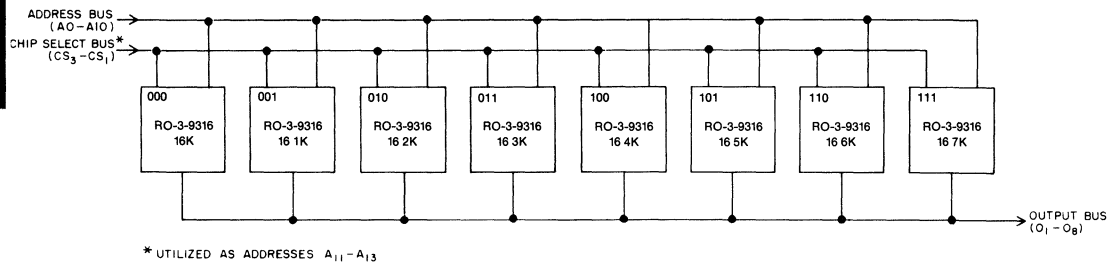
**Typical Values are at +25°C and nominal voltages

TYPICAL SYSTEM APPLICATION

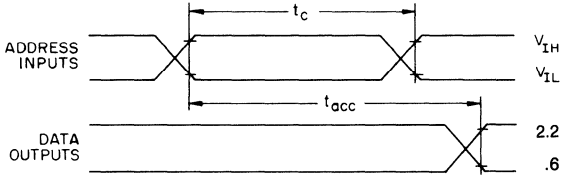
A complete system of 16K words of ROM (8 bits/word) is easily obtained without any external address decoding by making use of programable chip select features and by wiring the outputs of eight different RO-3-9316 as shown in the figure below.

CHIP SELECT TABLE

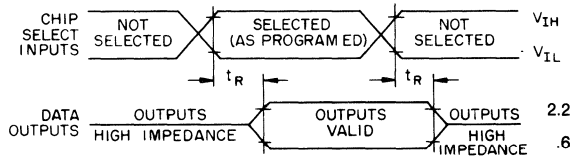
CS3	CS2	CS1	DEVICE SELECTED
0	0	0	16K0
0	0	1	16K1
0	1	0	16K2
0	1	1	16K3
1	0	0	16K4
1	0	1	16K5
1	1	0	16K6
1	1	1	16K7



TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)



CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

32,768 Bit Static Read Only Memory

FEATURES

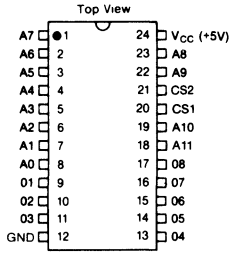
- 4096 x 8 Organization — Ideal for Microprocessor Memory Systems
- Single +5 Volt Supply
- TTL Compatible — All Inputs and Outputs
- Static Operation — No Clocks Required
- 850ns Maximum Access Time: RO-3-9332A
- 450ns Maximum Access Time: RO-3-9332B
- 350ns Maximum Access Time: RO-3-9332C
- Three-State Outputs — Under the Control of Two Mask-Programable Chip Select Inputs to Simplify Memory Expansion
- Totally Automated Custom Programing
- Zener Protected Inputs
- Glass Passivation Protection
- Pin Compatible With 2532 EPROM
- Extended Temperature Ranges

DESCRIPTION

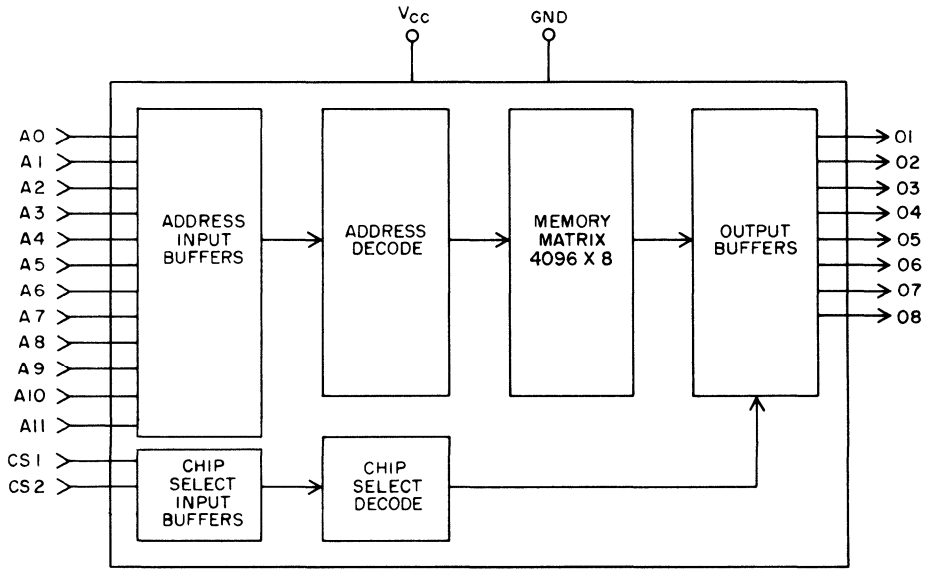
The General Instrument RO-3-9332 is a 32,768 static Read Only Memory organized as 4096 eight bit words and is ideally suited for microprocessor memory applications. Fabricated in the General Instrument N-Channel Ion Implant process to enable operation from a single +5 Volt power supply, the RO-3-9332 offers the best combination of high performance, large bit storage, and simple interfacing of any MOS Read-Only Memory available today.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±10%
Operating Temperature (T_A) = 0°C to +70°C
(HR: T_A = −55°C to +125°C)
Output Loading: Two TTL Loads, $C_{L\ TOTAL}$ = 100pf

RO-3-9332A/B ■ RO-3-9332HR

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select Inputs						
Logic "1"	V_{IH}	2	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = −200μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 3.2mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
RO-3-9332A	I_{CC}	—	—	80	mA	Outputs open
RO-3-9332BHR	I_{CC}	—	—	125	mA	Outputs open
RO-3-9332C	I_{CC}	—	—	140	mA	Outputs open

RO-3-9332A

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	800	—	—	ns	
Capacitance	C_1	—	5	8	pf	F = 1MHz
Data Outputs						
Access Time	t_{ACC}	—	600	850	ns	V_{OH} = 2.20V*
Chip Select Response Time	T_R	—	200	300	ns	
Capacitance	C_O	—	8	10	pf	F = 1MHz

RO-3-9332B ■ RO-3-9332BHR

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	450	—	—	ns	
Capacitance	C_1	—	5	8	pf	F = 1MHz
	C_1	—	8	10	pf	F = 1MHz; RO-3-9332BHR only
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	V_{OH} = 2.20V*
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pf	F = 1MHz

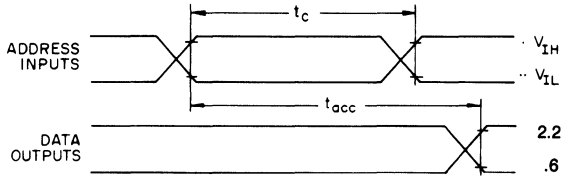
RO-3-9332C

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	300	—	—	ns	
Capacitance	C_1	—	5	8	pf	F = 1MHz
Data Outputs						
Access Time	t_{ACC}	—	250	350	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_0	—	8	10	pf	F = 1MHz

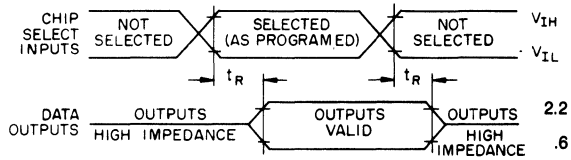
*See Timing Diagram

**Typical Values are at +25°C and nominal voltages

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)



CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

32,768 Bit Static Read Only Memory

FEATURES

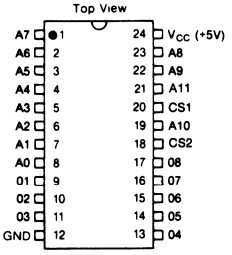
- 4096 x 8 Organization — Ideal for Microprocessor Memory Systems
- Single +5 Volt Supply
- TTL Compatible — All Inputs and Outputs
- Static Operation — No Clocks Required
- Pin Compatible With 2732 EPROM
- 450ns Maximum Access Time: RO-3-9333B
- 350ns Maximum Accent Time: RO-3-9333C
- Extended Temperature Range
- Three State Outputs — Under the Control of Two Mask-Programable Chip Select Inputs to Simplify Memory Expansion
- Totally Automated Custom Programing
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

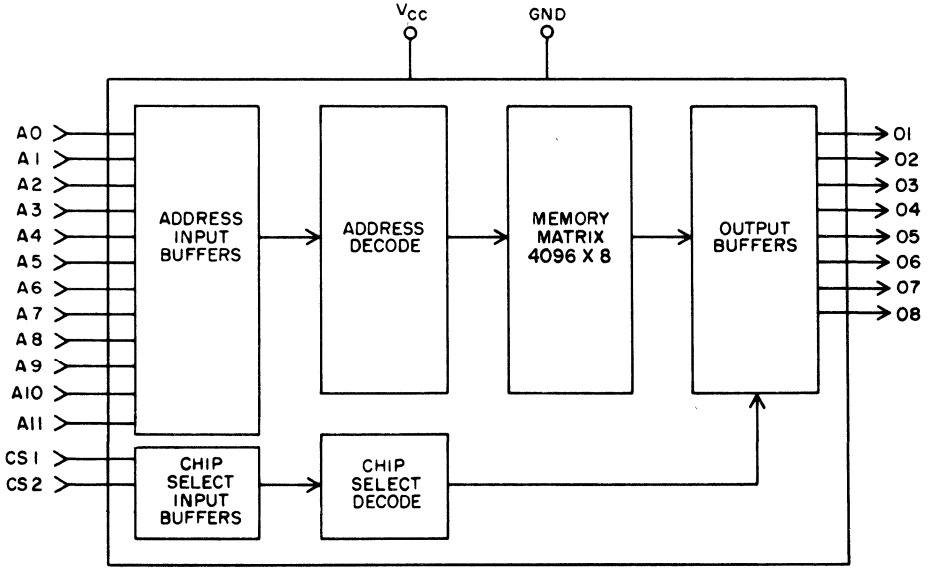
The General Instrument RO-3-9333 is a 32,768 bit static Read Only Memory organized as 4096 eight bit words and is ideally suited for microprocessor memory applications. Fabricated in the General Instrument N-Channel Ion Implant process to enable operation from a single +5 Volt power supply, the RO-3-9333 offers the best combination of high performance, large bit storage, and simple interfacing of any MOS Read-Only Memory available today.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings *

V_{CC} and input voltages (with respect to GND) . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±10%
Operating Temperature (T_A) = 0°C to +70°C
(HR: T_A = −55°C to +125°C)
Output Loading: Two TTL Loads, $C_{L\ TOTAL}$ = 100pf

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

RO-3-9333B/C ■ RO-3-9333HR

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select Inputs						
Logic "1"	V_{IH}	2	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = −200μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 3.2mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
RO-3-9333B	I_{CC}	—	—	125	mA	Outputs Open
RO-3-9333BHR	I_{CC}	—	—	120	mA	Outputs Open
RO-3-9333C	I_{CC}	—	—	140	mA	Outputs Open

RO-3-9333B ■ RO-3-9333BHR

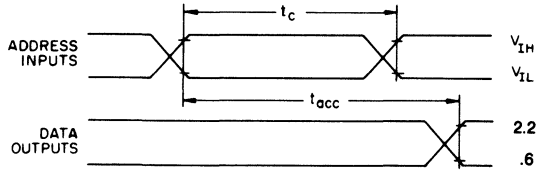
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	450	—	—	ns	
Capacitance	C_I	—	5	8	pf	F = 1MHz
	C_I	—	8	10	pf	F = 1MHz; RO-3-9333BHR only
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	V_{OH}=2.20V*
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pf	F = 1MHz

RO-3-9333C

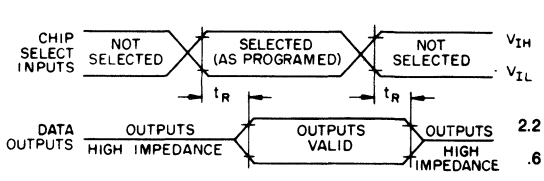
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	300	—	—	ns	
Capacitance	C_I	—	5	8	pf	F = 1MHz
Data Outputs						
Access Time	t_{ACC}	—	250	350	ns	V_{OH}=2.20V*
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pf	F = 1MHz

*See Timing Diagram
**Typical values are at +25°C and nominal voltages

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)



CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

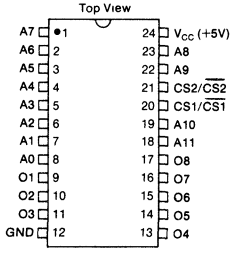
32,768 Bit Static Read Only Memory

FEATURES

- 4096 x 8 Organization
- Fully Static Operation—No Clocks Required
- Single +5V ± 10% Supply
- 450ns Access Time: RO9432B
- 300ns Access Time: RO9432C
- 200ns Access Time: RO9432D
- Inputs and Outputs TTL Compatible
- Three State Outputs—Under the Control of Two Mask Programable Chip Select Inputs
- Output Drive Capability of 2 TTL Loads and 100pf
- Low Power Dissipation
- Totally Automated Custom Programing
- All Inputs Protected Against Static Charge
- Pin Compatible With 2532 EPROM

PIN CONFIGURATION

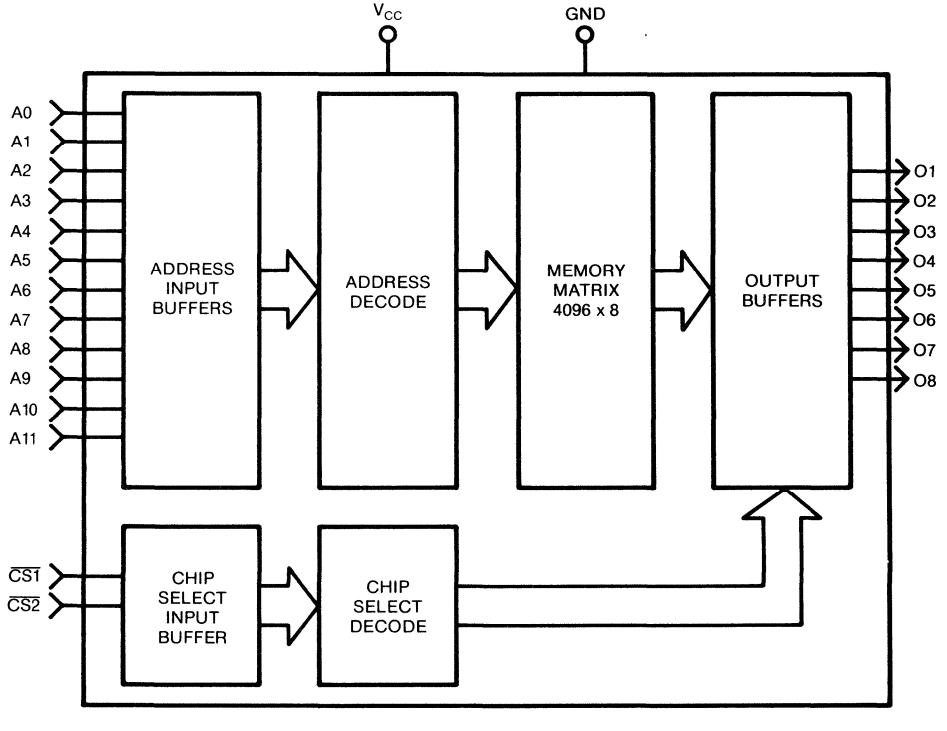
24 LEAD DUAL IN LINE



DESCRIPTION

The RO9432 is a 32,768 bit fully static Read Only Memory utilizing MOS N-Channel Silicon Gate Ion Implanted technology. It is organized 4096 words by 8 bits and operates from a single +5 Volt power supply with ±10% supply tolerance. All inputs are TTL compatible, and the three-state outputs can drive 2 standard TTL loads each.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages (with Respect to GND) ..... −0.5V to +7.0V
Storage Temperature ..... −65°C to +150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

$V_{CC} = +5V \pm 10\%$
Operating Temperature $T_A = 0°C$ to $+70°C$
Output Loading: Two TTL Loads + $C_{L\ TOTAL} = 100pf$

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Low Voltage	V_{IL}	−0.5	—	0.8	V	
Input High Voltage	V_{IH}	2	—	V_{CC}	V	
Input Load Current	I_{IL}	—	—	10	μA	$V_{IN} = 0$ to V_{CC}
Output Low Voltage	V_{OL}	—	—	0.40	V	$I_{OL} = +3.2mA$
Output High Voltage	V_{OH}	2.4	—	V_{CC}	V	$I_{OH} = -200\mu A$
Output Leakage Current	I_{LO}	—	—	10	μA	$V_{OUT} = 0V$ to V_{CC}
Power Supply Current	I_{CC}	—	—	100	mA	All Inputs +5.5V, Outputs Unloaded

AC CHARACTERISTICS

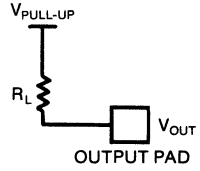
		RO9432B		RO9432C		RO9432D			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Address Access Time	t_{ACC}	—	450	—	300	—	200	ns	
Chip Select to Output Delay Time	t_{CO}	—	100	—	100	—	75	ns	
Chip Deselect to Output Float Time	t_{DF}	—	75	—	75	—	75	ns	
Previous Data Valid After Address Change	t_{OH}	20	—	20	—	20	—	ns	
Capacitance*									
Input Capacitance	C_{IN}	—	7	—	7	—	7	pf	$T_A = 25°C$, F = 1MHz
Output Capacitance	C_{OUT}	—	10	—	10	—	10	pf	$T_A = 25°C$, F = 1MHz

*Not tested 100%

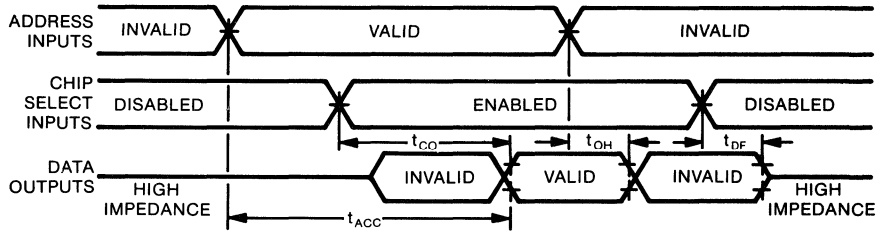
AC TEST CONDITIONS

Input Pulse Levels ..... 0.8V to 2.2V
Input Rise and Fall Times ..... 20 ns
Timing Measurement Levels:
Input 1.5V
Output ..... 0.8V and 2.0V
Output Load ..... 2 TTL Loads +100pf (See Figure 1)

CONDITIONS OF TEST FOR AC CHARACTERISTICS



TIMING DIAGRAM



DEFINITIONS

Access Time, T_{ACC}
Access time is the maximum time between the application of a valid Address and the corresponding Data Out.

Output Hold Delay, T_{OH}
Output hold delay is the minimum time after an Address change that the previous data remains valid.

Output Enable Time, T_{CO}
Output enable time is the maximum delay between Chip Selects becoming true and Output Data becoming valid.

Output Disable Time, T_{DF}
Output disable time is the delay between Chip Selects becoming false and output stages going to the high impedance state.

READ ONLY MEMORY

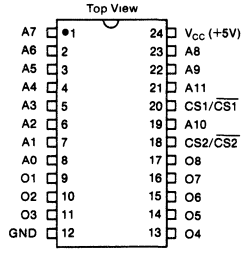
32,768 Bit Static Read Only Memory

FEATURES

- 4096 x 8 Organization
- Fully Static Operation—No Clocks Required
- Single +5V ± 10% Supply
- 450ns Access Time: RO9433B
- 300ns Access Time: RO9433C
- 200ns Access Time: RO9433D
- Inputs and Outputs TTL Compatible
- Three State Outputs—Under the Control of Two Mask Programable Chip Select Inputs
- Output Drive Capability of 2 TTL Loads and 100pf
- Low Power Dissipation
- Totally Automated Custom Programing
- All Inputs Protected Against Static Charge
- Pin Compatible With 2732 EPROM

PIN CONFIGURATION

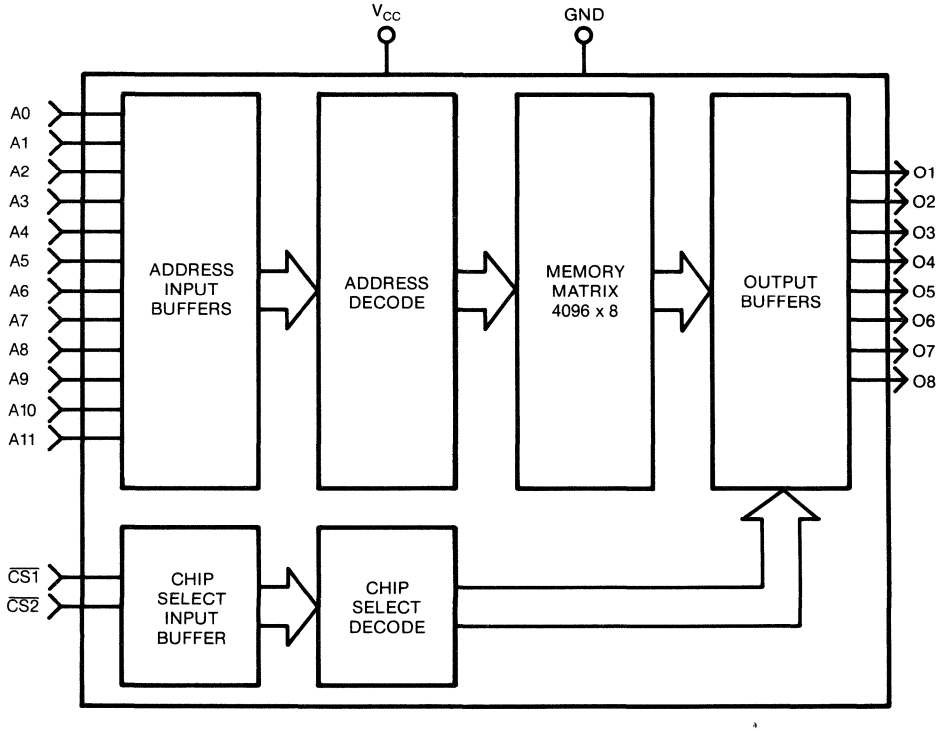
24 LEAD DUAL IN LINE



DESCRIPTION

The RO9433 is a 32,768 bit fully static Read Only Memory utilizing MOS N-Channel Silicon Gate Ion Implanted technology. It is organized 4096 words by 8 bits and operates from a single +5 Volt power supply with ± 10% supply tolerance. All inputs are TTL compatible, and the three-state outputs can drive 2 standard TTL loads each.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages (with Respect to GND) ..... −0.5V to +7.0V
Storage Temperature ..... −65°C to +150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{CC} = +5V ± 10%
Operating Temperature T_A = 0°C to +70°C
Output Loading: Two TTL Loads, $C_{L\ TOTAL}$ = 100pf

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, $\overline{\text{CHIP SELECTS}}$						
Inputs						
Logic "1"	V_{IH}	2	—	V_{CC}	V	
Logic "0"	V_{IL}	0	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	V_{IN} = 0V to V_{CC}
Data Outputs						
Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = −200μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 3.2mA
Leakage	I_{LO}	—	—	10	μA	V_{OUT} = 0V to V_{CC}
Power Supply Current	I_{CC}	—	—	100	mA	All inputs +5.5V. Outputs Unloaded

AC CHARACTERISTICS

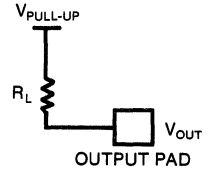
		RO9433B		RO9433C		RO9433D			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Address Access Time	t_{ACC}	—	450	—	300	—	200	ns	
Chip Select to Output Delay Time	t_{CO}	—	100	—	100	—	75	ns	
Chip Deselect to Output Float Time	t_{DF}	—	75	—	75	—	75	ns	
Previous Data Valid After Address Change	t_{OH}	20	—	20	—	20	—	ns	
Capacitance*									
Input Capacitance	C_{IN}	—	7	—	7	—	7	pf	T_A = 25°C, F = 1MHz
Output Capacitance	C_{OUT}	—	10	—	10	—	10	pf	T_A = 25°C, F = 1MHz

*Not tested 100%

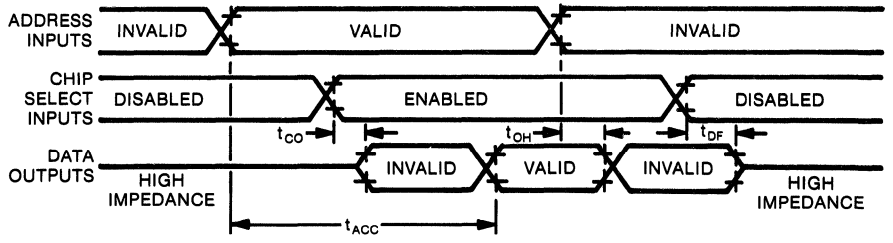
AC TEST CONDITONS

Input Pulse Levels ..... 0.8V to 2.2V
Input Rise and Fall Times ..... 20 ns
Timing Measurement Levels:
Input 1.5V
Output ..... 0.8V and 2.0V
Output Load ..... 2 TTL Loads +100pf (See Figure 1)

CONDITIONS OF TEST FOR AC CHARACTERISTICS



TIMING DIAGRAM



DEFINITIONS

Access Time, T_{ACC}
Access time is the maximum time between the application of a valid Address and the corresponding Data Out.

Output Hold Delay, T_{OH}
Output hold delay is the minimum time after an Address change that the previous data remains valid.

Output Enable Time, T_{CO}
Output enable time is the maximum delay between Chip Selects becoming true and Output Data becoming valid.

Output Disable Time, T_{DF}
Output disable time is the delay between Chip Selects becoming false and output stages going to the high impedance state.

65,536 Bit Edge-Triggered Read Only Memory

FEATURES

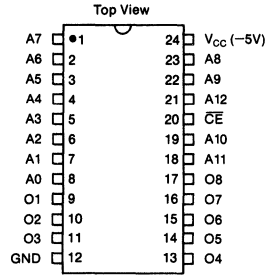
- 8192 x 8 Organization
- Single +5 Volt ± 10% Supply
- TTL Compatible — All Inputs and Outputs
- Edge Triggered Operation
- 450ns Maximum Access Time: RO-3-9364B
- 300ns Maximum Access Time: RO-3-9364C
- Three-State Outputs — Under the Control of Chip Enable Input
- 2 TTL Load/100pf Output Drive Compatibility
- Low Power Dissipation — 250mW active, 150mW Standby
- Totally Automated Custom Programing
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

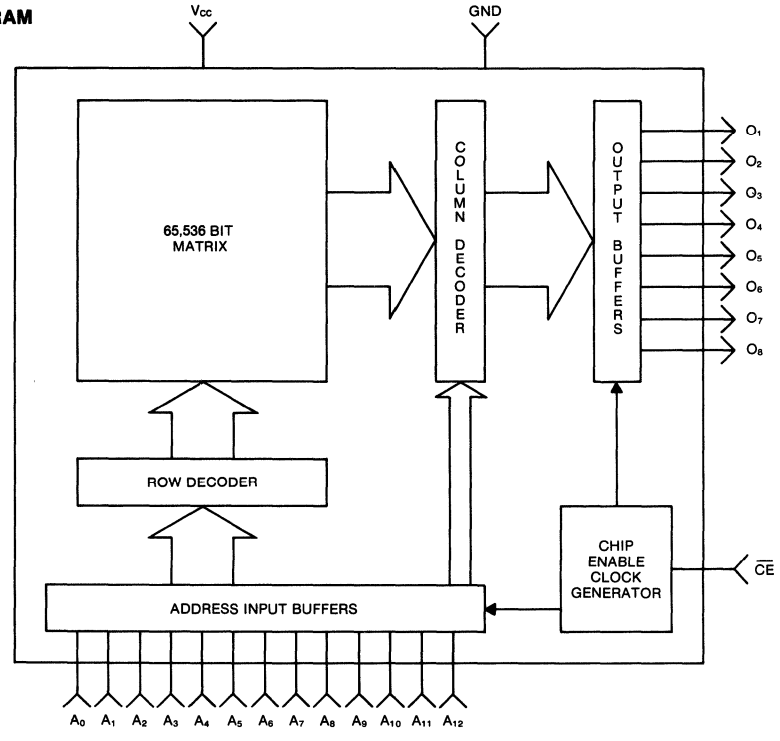
The General Instrument RO-3-9364 is a 65,536 Bit Edge-Triggered Read Only Memory organized as 8192 8-bit words and is ideally suited for microprocessor memory applications. Fabricated with General Instrument N-Channel Silicon Gate Technology, the RO-3-9364 provides the designer with a high performance, easy-to-use MOS circuit featuring operation from a single +5 Volt power supply and low power dissipation. The RO-3-9364 offers the best combination of high performance, large bit storage and simple interfacing of any MOS Read Only Memory available today.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages (with Respect to GND) ..... −0.5V to +7.0V
Storage Temperature ..... −65°C to +150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{CC} = +5V ± 10%
Operating Temperature T_A = 0°C to +70°C
HR: T_A = −55°C to +125°C
Output Loading: Two TTL Loads, $C_{L\ TOTAL}$ = 100pf

DC CHARACTERISTICS

		RO-3-9364B/C			RO-3-9364HR				
Characteristics	**Sym**	**Min**	**Typ****	**Max**	**Min**	**Typ****	**Max**	**Units**	**Conditions**
Address, CHIP ENABLE Inputs									
Logic "1"	V_{IH}	2	—	—	2	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	—	—	0.7	V	
Leakage	I_{LI}	—	—	10	—	—	10	μA	$V_{IN} = V_{CC}$
Data Outputs									
Logic "1"	V_{OH}	2.4	—	—	2.4	—	—	V	$I_{OH} = -200\mu A$
Logic "0"	V_{OL}	—	—	0.4	—	—	0.4	V	$I_{CL} = 3.2mA$
Leakage	I_{LO}	—	—	10	—	—	10	μA	$V_{OUT} = V_{CC}$
Power Supply Current									
I_{CC} (Active) RO-3-9364B		—	—	—	50			mA	Output Loading 1MΩ and 100pf
RO-3-9364C		—	—	—	50		N/A		$\overline{CE}$ at Minimum Cycle Time
I_{CC} (Standby) RO-3-9364B		—	—	—	30			mA	$\overline{CE}$ = Logic "1"
RO-3-9364C		—	—	—	30		N/A		
RO-3-9364HR				N/A		—	—	35	

AC CHARACTERISTICS

		RO-3-9364B			RO-3-9364C				
Characteristics	**Sym**	**Min**	**Typ****	**Max**	**Min**	**Typ****	**Max**	**Units**	**Conditions**
Cycle Time	t_C	600	—	—	400	—	—	ns	
$\overline{CE}$ Pulse Width	t_{CE}	450	—	—	300	—	—	ns	
$\overline{CE}$ Precharge Time	t_P	150	—	—	100	—	—	ns	All Outputs Driving
$\overline{CE}$ Access Time	t_{AC}	—	—	450	—	—	300	ns	Two TTL Loads
Output Turn Off Time	t_{OFF}	—	—	150	—	—	150	ns	and 100pf
Address Set Up Time	t_{AS}	0	—	—	0	—	—	ns	
Address Hold Time	t_{AH}	90	—	—	75	—	—	ns	
Capacitance									
Input Capacitance	C_I	—	—	7	—	—	7	pf	F = 1MHz, T_A = +25°C
Output Capacitance	C_O	—	—	10	—	—	10	pf	F = 1MHz, T_A = +25°C

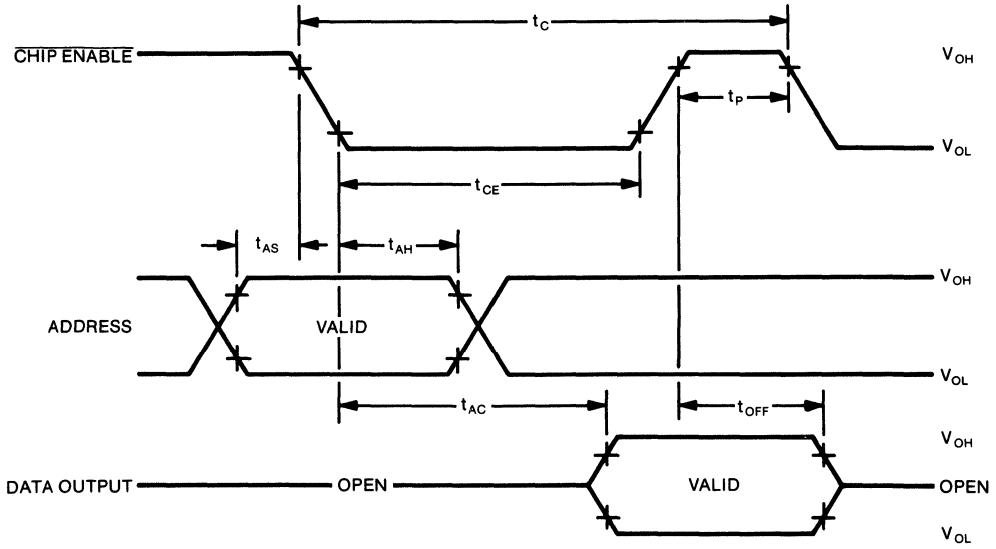
		RO-3-9364HR ***				
Characteristics	**Sym**	**Min**	**Typ****	**Max**	**Units**	**Conditions**
Cycle Time	t_C	400	—	—	ns	
$\overline{CE}$ Pulse Width	t_{CE}	300	—	—	ns	
$\overline{CE}$ Precharge Time	t_P	—	—	150	ns	All Outputs Driving
$\overline{CE}$ Access Time	t_{AC}	—	—	450	ns	Two TTL Loads
Output Turn Off Time	t_{OFF}	—	—	150	ns	and 100pf
Address Set Up Time	t_{AS}	0	—	—	ns	
Address Hold Time	t_{AH}	75	—	—	ns	
Capacitance						
Input Capacitance	C_I	—	—	7	pf	F = 1MHz, T_A = +25°C
Output Capacitance	C_O	—	—	10	pf	F = 1MHz, T_A = +25°C

**Typical values are at +25°C and nominal voltages
***Preliminary specification

OPERATION

The RO-3-9364 is controlled by the chip enable. A negative going edge at $\overline{CE}$ input will activate the device and latch the addresses into the on-chip address registers. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. The circuit can be put into an automatic low power standby mode by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced as compared to unclocked devices which draw full power continuously.

TIMING DIAGRAM



65,536 Bit Edge-Triggered Read Only Memory

FEATURES

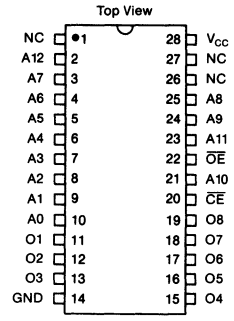
- 8192 x 8 Organization
- Single +5 Volt + 10% Supply
- TTL Compatible — All Inputs and Outputs
- Edge Triggered Operation
- 450ns Maximum Access Time: RO-3-9365B
- 300ns Maximum Access Time: RO-3-9365C
- Three-State Outputs — Under the Control of Chip Enable Input
- 2 TTL Load/100pf Output Drive Compatibility
- Low Power Dissipation — 250mW Active, 150mW Standby
- Totally Automated Custom Programing
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

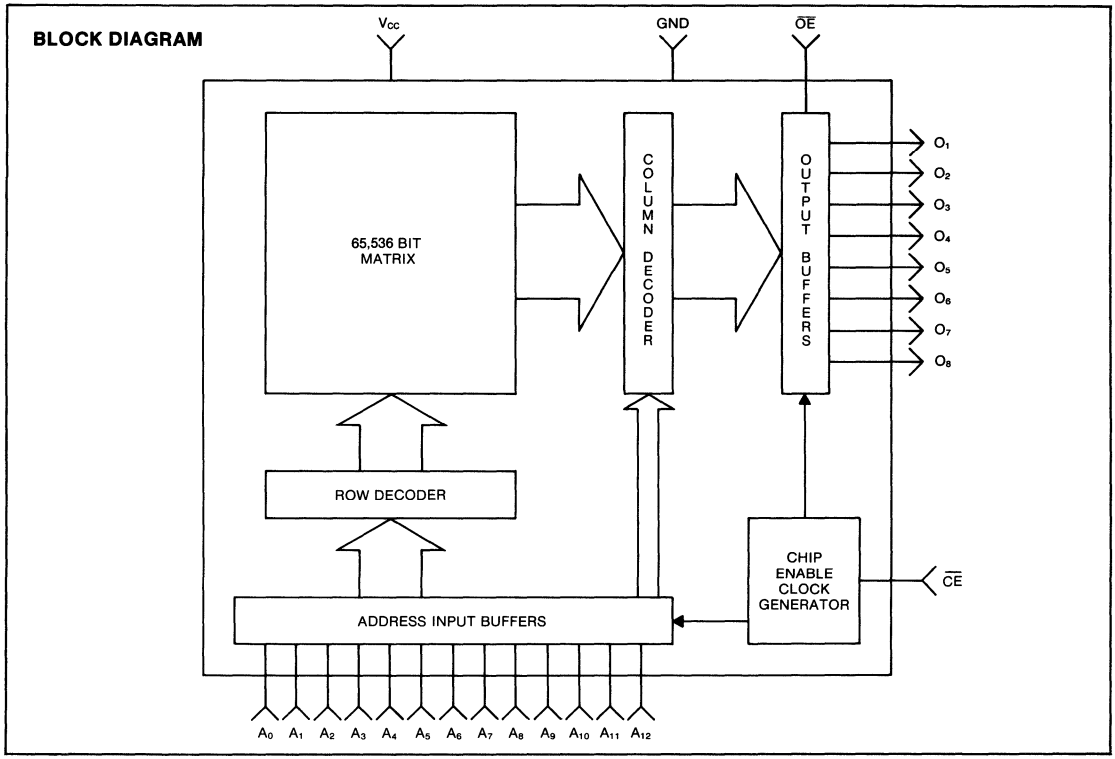
The General Instrument RO-3-9365 is a 65,536 Bit Edge-Triggered Read Only Memory organized as 8192 8-bit words and is ideally suited for microprocessor memory applications. Fabricated with General Instrument N-Channel Silicon Gate Technology,the RO-3-9365 provides the designer with a high performance, easy-to-use MOS circuit featuring operation from a single +5 Volt power supply and low power dissipation. The RO-3-9365 offers the best combination of high performance, large bit storage, and simple interfacing of any MOS Read Only Memory available today.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages (with Respect to GND) ..... −0.5V to +7.0V
Storage Temperature ..... −65°C to +150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{CC} = +5V ± 10%
Operating Temperature T_A = 0°C to +70°C
Output Loading: Two TTL Loads, $C_{L\ TOTAL}$ = 100pf

DC CHARACTERISTICS

		RO-3-9365B/C				
Characteristics	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Address, $\overline{\text{CHIP ENABLE}}$ Inputs						
Logic "1"	V_{IH}	2	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = 200μA
Logic "0"	I_{OL}	—	—	0.4	V	I_{OL} = 3.2mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC} (Active)	—	—	—	50	mA	Output Loading 1MΩ and 100pf $\overline{CE}$ at Minimum Cycle Time
I_{CC} (Standby)	—	—	—	30	mA	$\overline{CE}$ = Logic "1"

AC CHARACTERISTICS

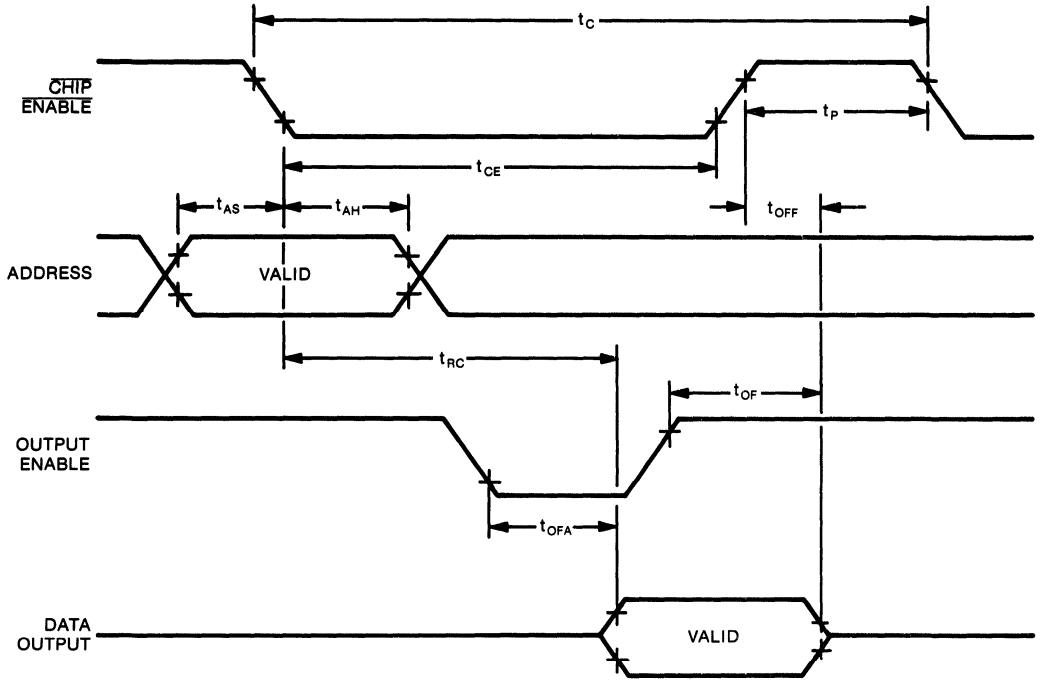
		RO-3-9365B			RO-3-9365C				
Characteristics	**Sym**	**Min**	**Typ**	**Max**	**Min**	**Typ****	**Max**	**Units**	**Conditions**
Cycle Time	t_C	600	—	—	400	—	—	ns	
$\overline{CE}$ Pulse Width	t_{CE}	450	—	—	300	—	—	ns	
$\overline{CE}$ Precharge Time	t_P	150	—	—	100	—	—	ns	
$\overline{CE}$ Access Time	t_{AC}	—	—	450	—	—	300	ns	All Outputs Driving
Output Turn Off Time	t_{OFF}	—	—	90	—	—	75	ns	Two TTL Loads
Address Set Up Time	t_{AS}	0	—	—	0	—	—	ns	and 100pf
Address Hold Time	t_{AH}	90	—	—	75	—	—	ns	
Output Enable Access Time	t_{OEA}	—	—	80	—	—	100	ns	
Output Enable Data Off Time	t_{OEZ}	—	—	60	—	—	75	ns	
Capacitance									
Input Capacitance	C_I	—	—	7	—	—	7	pf	F = 1MHz, T_A = +25°C
Output Capacitance	C_O	—	—	10	—	—	10	pf	F = 1MHz, T_A = +25°C

**Typical Values are at +25°C and Nominal Voltages.

OPERATION

The RO-3-9365 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$). A negative going edge at the $\overline{CE}$ input will activate the device and latch the addresses into the on-chip address registers. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access time (t_{ac}) if the output enable access time (t_{OEA}) requirement is met. The on chip address register allows addresses to be changed after the specified hold time (t_{ah}) in preparation for the next cycle. The outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the inactive state. After output turn off time (t_{off}) the output buffers will go to a high impedance state. The $\overline{CE}$ input must remain inactive (high) between subsequent cycles for time (t_p) to allow for precharging the nodes of the internal circuitry.

TIMING DIAGRAM



READ ONLY MEMORY

65,536 Bit Static Read Only Memory

FEATURES

- 8192 x 8 Organization
- Fully Static Operation
- Single +5V ± 10% Supply
- Inputs and Outputs TTL Compatible
- Three State Outputs
- Output Drive Capability of 2 TTL Loads and 100pf
- 24 Pin JEDEC Approved Pinout

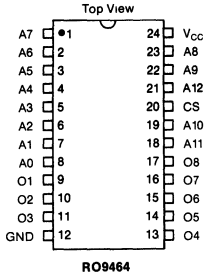
DESCRIPTION

The General Instrument RO9464 and RO9464A are 65,536 Bit Static Read Only Memories organized as 8192 eight-bit words and are ideally suited for microprocessor memory applications. Fabricated with General Instrument N-Channel Silicon Gate Technology, the RO9464 and RO9464A provide the designer with a high performance, easy to use MOS circuit featuring operation from a single +5 Volt power supply and low power dissipation. The RO9464 and RO9464A offer the best combination of high performance, large bit storage and simple interfacing of any MOS Read Only Memory available today.

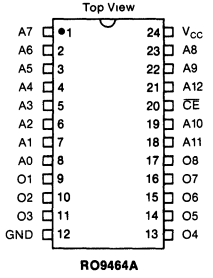
The RO9464 offers a programable chip select on pin 20. The RO9464A offers an automatic power down feature on pin 20. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high.

PIN CONFIGURATION

24 LEAD DUAL IN LINE

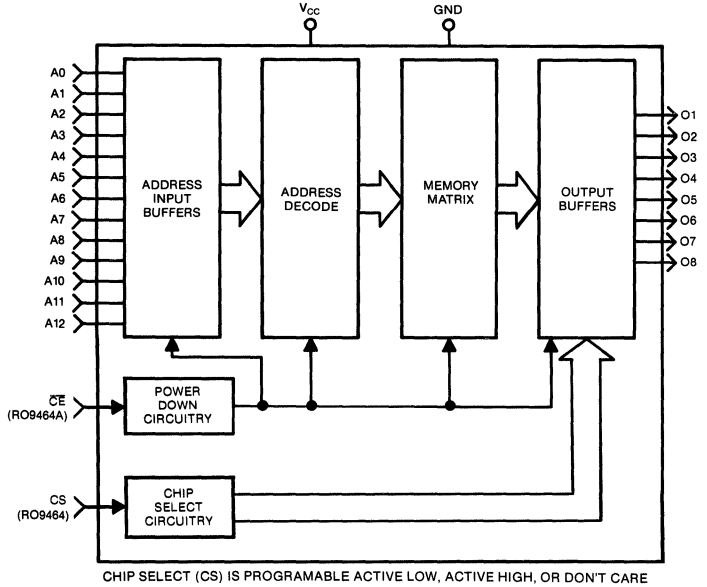


RO9464



RO9464A

BLOCK DIAGRAM



CHIP SELECT (CS) IS PROGRAMABLE ACTIVE LOW, ACTIVE HIGH, OR DON'T CARE

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature ..... −65°C to +150°C
Supply Voltage to Ground Potential ..... −0.5V to +7.0V
Applied Output Voltage ..... −0.5V to +7.0V
Applied Input Voltage ..... −0.5V to +7.0V
Power Dissipation 1.0W

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):
Operating Temperature $T_A = 0°C$ to $+70°C$
$V_{CC} = +5V \pm 10\%$

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Output High Level	V_{OH}	2.4	—	V_{CC}	V	$I_{OH} = -200\mu A$
Output Low Level	V_{OL}	—	—	0.4	V	$I_{OL} = 3.2mA$
Input High Level	V_{IH}	2	—	V_{CC}	V	
Input Low Level	V_{IL}	−0.5	—	0.8	V	
Input Leakage Current	I_{LI}	—	—	10	μA	$V_{IN} = 0V$ to V_{CC}
Output Leakage Current	I_{LO}	—	—	10	μA	$V_{OUT} = 0V$ to V_{CC}
Operating Supply Current	I_{CC}	—	—	100	mA	Note 1
Standby Supply Current	I_{SB}	—	—	12	mA	Note 2

AC CHARACTERISTICS

		RO9464B RO9464AB		RO9464C RO9464AC		RO9464D RO9464AD			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Cycle Time	t_{CYC}	450	—	300	—	200	—	ns	
Address Access Time	t_{AA}	—	450	—	300	—	200	ns	
Output Hold After Address Change	t_{OH}	20	—	20	—	20	—	ns	
Chip Enable Access Time	t_{ACE}	—	450	—	300	—	200	ns	Note 4
Chip Select Access Time	t_{ACS}	—	150	—	100	—	85	ns	Note 3
Output Low Z Delay	t_{LZ}	20	—	20	—	20	—	ns	Note 5
Output High Z Delay	t_{HZ}	—	75	—	75	—	75	ns	Note 6
Power Up Time	t_{PU}	0	20	0	20	0	20	ns	Notes 4, 7
Power Down Time	t_{PD}	—	150	—	100	—	100	ns	Note 4
Capacitance**									
Input Capacitance	C_I	—	7	—	7	—	7	pf	F = 1MHz, $T_A = +25°C$
Output Capacitance	C_O	—	10	—	10	—	10	pf	F = 1MHz, $T_A = +25°C$

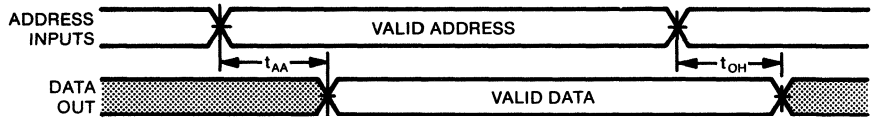
**Capacitance is periodically sampled and is not 100% tested.

NOTES:
1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only and measured with $\overline{CE} = 2.0V$.
3. Applies to Non-"A"versions only.
4. Applies to "A" versions (power down) only.
5. Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ going low or CS going active.
6. Output high impedance delay (t_{HZ}) is measured from $\overline{CE}$ going high or CS going inactive.
7. Power Up Time (t_{PU}) is not additive to Chip Enable Access Time (t_{ACE}).

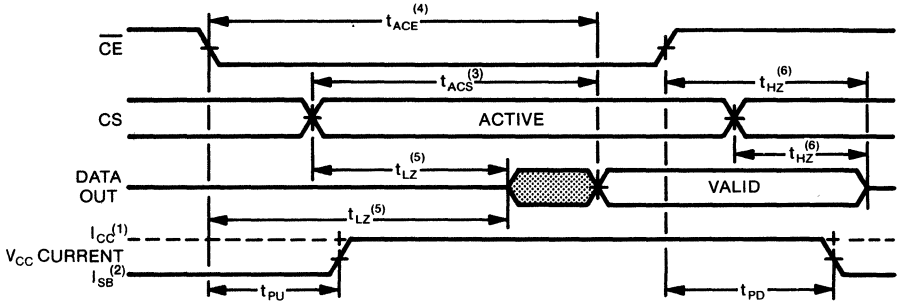
Part Number	Maximum Access Time	Operating Current	Standby Current
RO9464B	450ns	100mA	NA
RO9464C	300ns	100mA	NA
RO9464D	200ns	100mA	NA
RO9464AB	450ns	100mA	12mA
RO9464AC	300ns	100mA	12mA
RO9464AD	200ns	100mA	12mA

TIMING DIAGRAMS

Propagation Delay from Address ($\overline{CE}$ LOW or CS = Active)



Propagation Delay from Chip Enable, Chip Select or Output Enable (Address Valid)



AC TEST CONDITIONS

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	20 nsec
Timing Measurement Levels: Input	1.5V
Output	0.8V and 2.0V
Output Load	See Figure 1

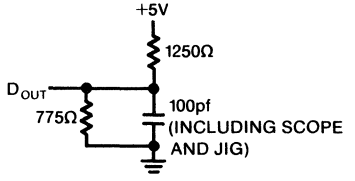


Fig. 1

65,536 Bit Static Read Only Memory

FEATURES

- 8192 x 8 Organization
- Fully Static Operation
- Single +5V ± 10% Supply
- Inputs and Outputs TTL Compatible
- Three State Outputs
- 28 Pin JEDEC Approved Pinout (RO9864A)

DESCRIPTION

The General Instrument RO9864 and RO9864A are 65,536 Bit Static Read Only Memories organized as 8192 eight-bit words and are ideally suited for microprocessor memory applications. Fabricated with General Instrument N-Channel Silicon Gate Technology, the RO9864 and RO9864A provide the designer with a high performance, easy to use MOS circuit featuring operation from a single +5 Volt power supply and low power dissipation. The RO9864 and RO9864A offer the best combination of high performance, large bit storage and simple interfacing of any MOS Read Only Memory available today.

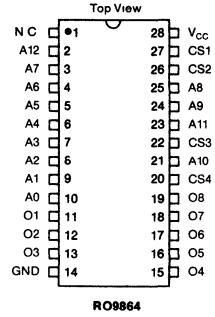
The RO9864 offers a four input chip select (CS3 and CS4 are on Pin 22 and 20 respectively) enables usage in large memory applications.

The RO9864A offers an automatic power down feature. On Pin 20 power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high.

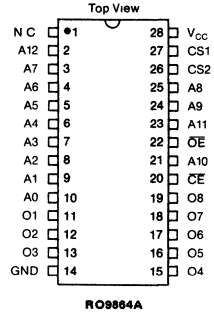
The RO9864A offers an Output Enable ($\overline{OE}$), on Pin 22, that eliminates bus contention in applications using large memory systems.

PIN CONFIGURATION

28 LEAD DUAL IN LINE

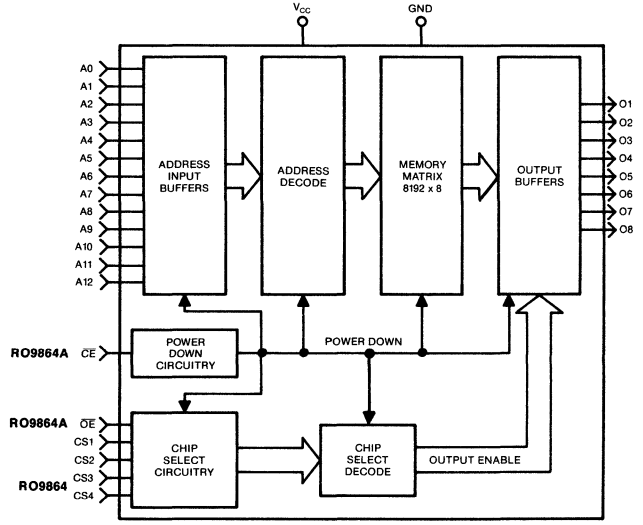


RO9864



RO9864A

BLOCK DIAGRAM



CHIP SELECT (CS) ARE PROGRAMABLE ACTIVE LOW, ACTIVE HIGH, OR DON'T CARE

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature ..... −65°C to +150°C
Supply Voltage to Ground Potential ..... −0.5V to +7.0V
Applied Output Voltage ..... −0.5V to +7.0V
Applied Input Voltage ..... −0.5V to +7.0V
Power Dissipation 1.0W

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

Operating Temperature T_A = 0°C to +70°C
V_{CC} = +5V ± 10%

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Output High Level	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = −200 μA
Output Low Level	V_{OL}	—	—	0.4	V	I_{OL} = 3.2mA
Input High Level	V_{IH}	2	—	V_{CC}	V	
Input Low Level	V_{IL}	−0.5	—	0.8	V	
Input Leakage Current	I_{LI}	—	—	10	μA	V_{IN} = V_{CC}
Output Leakage Current	I_{LO}	—	—	10	μA	V_{OUT} = V_{CC}
Operating Supply Current	I_{CC}	—	—	100	mA	Note 1
Standby Supply Current	I_{SB}	—	—	12	mA	Note 2

AC CHARACTERISTICS

		RO9864B RO9864AB		RO9864C RO9864AC		RO9864D RO9864AD			
Characteristics	Sym	Min	Max	Min	Max	Min	Max	Units	Conditions
Cycle Time	t_{CYC}	450	—	300	—	200	—	ns	
Address Access Time	t_{AA}	—	450	—	300	—	200	ns	
Output Hold After Address Change	t_{OH}	20	—	20	—	20	—	ns	
Chip Enable Access Time	t_{ACE}	—	450	—	300	—	200	ns	Note 2
Chip Select Access Time	t_{ACS}	—	75	—	75	—	75	ns	Note 3
Output Enable Access Time	t_{AOE}	—	75	—	75	—	75	ns	Note 2
Output Low Z Delay	t_{LZ}	20	—	20	—	20	—	ns	Note 4
Output High Z Delay	t_{HZ}	—	75	—	75	—	75	ns	Note 5
Power Up Time	t_{PU}	0	20	0	20	0	20	ns	Notes 2, 6
Power Down Time	t_{PD}	—	100	—	100	—	100	ns	Notes 2, 6
Capacitance**									
Input Capacitance	C_I	—	7	—	7	—	7	pf	F = 1MHz, T_A = +25°C
Output Capacitance	C_O	—	10	—	10	—	10	pf	F = 1MHz, T_A = +25°C

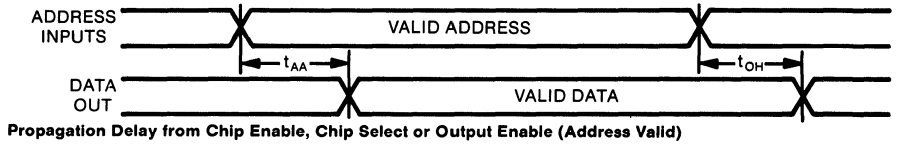
**Capacitance is periodically sampled and is not 100% tested.

NOTES:
1. Measured with device selected and outputs unloaded.
2. Applies to "A" versions only.
3. Applies to non "A" versions only.
4. Output low impedance delay (t_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going low and CS going active, whichever occurs last.
5. Output high impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going high or CS going inactive, whichever occurs first.
6. Power Up Time (t_{PU}) is not additive to Chip Enable Access Time (t_{ACE}).

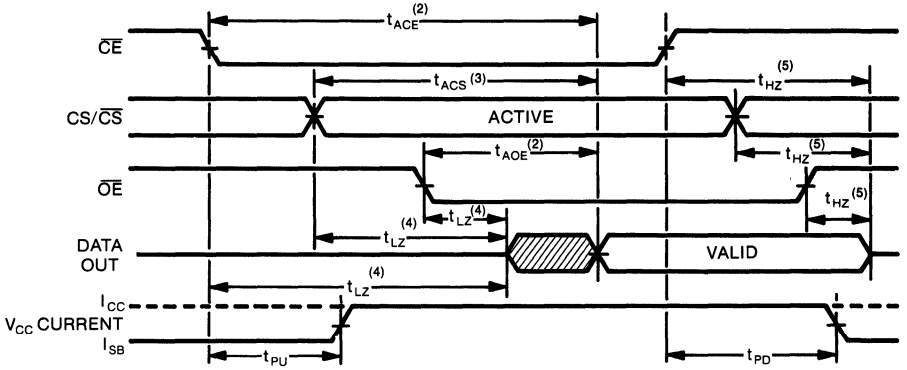
Part Number	Maximum Access Time	Operating Current	Standby Current
RO9864B	450ns	100mA	NA
RO9864C	300ns	100mA	NA
RO9864D	200ns	100mA	NA
RO9864AB	450ns	100mA	12mA
RO9864AC	300ns	100mA	12mA
RO9864AD	200ns	100mA	12mA

TIMING DIAGRAMS

Propagation Delay from Address $\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active



Propagation Delay from Chip Enable, Chip Select or Output Enable (Address Valid)



AC TEST CONDITIONS

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	20 nsec
Timing Measurement Levels: Input	1.5V
Output	0.8V and 2.0V
Output Load	See Figure 1

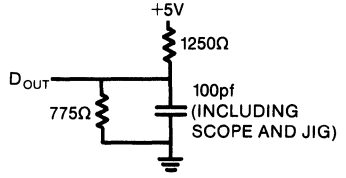


Fig. 1

READ ONLY MEMORY

131,072 Bit Static Read Only Memory

FEATURES

- 16,384 x 8 Organization
- Single +5 Volt Supply
- 450ns Max Access Time: RO9128B
- 300ns Max Access Time: RO9128C
- 200ns Max Access Time: RO9128D
- Totally Static Operation
- Three State Outputs
- All TTL Compatible Inputs/Outputs
- 28 Pin JEDEC Approved Pinout

DESCRIPTION

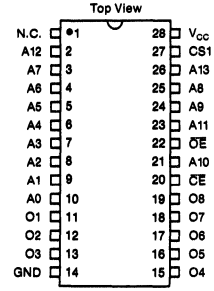
The General Instrument RO9128 is a 131,072 Bit Static Read Only Memory organized as 16,384 eight-bit words and is ideally suited for microprocessor memory applications. Fabricated with General Instrument N-Channel Silicon Gate Technology, the RO9128 provides the designer with a high performance, easy to use MOS circuit featuring operation from a single +5 Volt power supply and low power dissipation.

The RO9128 offers a power down feature controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high.

PIN CONFIGURATION

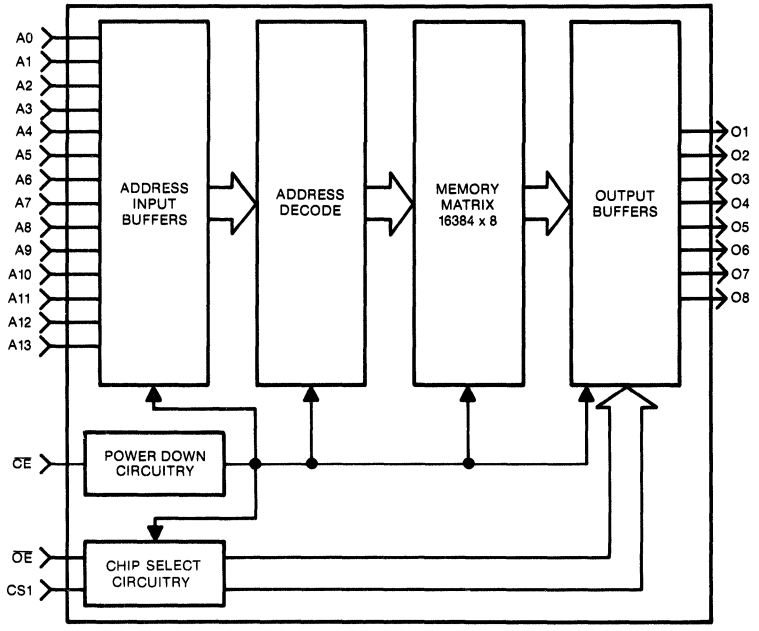
28 LEAD DUAL IN LINE

Top View



The Output Enable ($\overline{OE}$), and Chip Select (CS1) functions eliminate bus contention in multiple memory device systems.

BLOCK DIAGRAM



CHIP SELECT (CS1) IS PROGRAMABLE ACTIVE LOW, ACTIVE HIGH, OR DON'T CARE

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages (with Respect to GND) ..... −0.5V to +7.0V
Storage Temperature ..... −65°C to +150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise noted):

V_{CC} = +5V ± 10%
Operating Temperature T_A = 0°C to +70°C
Output Loading: Two TTL Loads, $C_{L\ TOTAL}$ = 100pf

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, $\overline{CE}$, $\overline{OE}$, CS1 Inputs						
Logic "1"	V_{IH}	2.0	—	V_{CC}	V	
Logic "0"	V_{IL}	0	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	$V_{IN} = V_{CC}$
Data Outputs						
Logic "1"	V_{OH}	2.4	—	V_{CC}	V	$I_{OH} = -200\mu A$
Logic "0"	V_{OL}	—	—	0.4	V	$I_{OL} = 3.2mA$
Leakage	I_{LO}	—	—	10	μA	$V_{OUT} = V_{CC}$
Power Supply Current						
I_{CC} (Active)	—	—	—	100	mA	Output Unloaded, Chip Enabled
I_{CC} (Standby)	—	—	—	12	mA	$\overline{CE}$ = 2.0V

AC CHARACTERISTICS

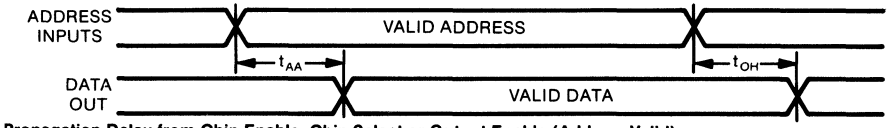
		RO9128B		RO9128C		RO9128D			
Characteristics	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Conditions**
Address Access Time	t_{ACC}	—	450	—	300	—	200	ns	
Address Hold After Address Change	t_{OH}	20	—	20	—	20	—	ns	
Chip Enable Access Time	t_{ACE}	—	450	—	300	—	200	ns	
Chip Select, Output Enable Access Time	t_{ACS}	—	100	—	100	—	75	ns	Note 1
Output Low Z Delay	t_{LZ}	20	—	20	—	20	—	ns	Note 2
Output High Z Delay	t_{HZ}	—	75	—	75	—	75	ns	Note 3
Power-Up Time	t_{PU}	0	20	0	20	0	20	ns	Note 4
Power-Down Time	t_{PO}	—	100	—	100	—	100	ns	
Capacitance**									
Input Capacitance	—	7	—	7	—	7	—	pf	F = 1MHz, T_A = +25°C
Output Capacitance	—	10	—	10	—	10	—	pf	F = 1MHz, T_A = +25°C

NOTES:
1. Access time to Valid Data (assuming data previously Enabled and addressed), measured from $\overline{OE}$ and CS1 going low, whichever occurs last.
2. Output low impedance delay (Data Invalid/Valid) is measured from $\overline{OE}$ and $\overline{CE}$ going low, or CS1 going active, whichever occurs last.
3. Output high impedance delay is measured from $\overline{OE}$ or $\overline{CE}$ going high or CS1 going Inactive whichever occurs first.
4. Power Up Time is not added to Chip Enable Access Time (t_{ACE}).

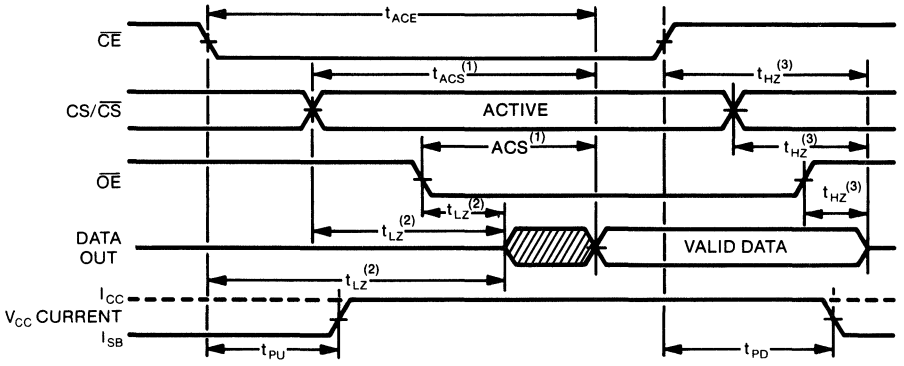
**Capacitance is periodically sampled and is not 100% tested.

TIMING DIAGRAMS

Propagation Delay from Address $\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = Active



Propagation Delay from Chip Enable, Chip Select or Output Enable (Address Valid)



AC TEST CONDITIONS

Input Pulse Levels	0.8V to 2 2V
Input Rise and Fall Times	20 nsec
Timing Measurement Levels. Input	1.5V
Output	0 8V and 2.0V
Output Load	See Figure 1

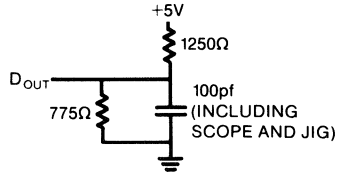


Fig. 1

262,144 Bit Static Read Only Memory

FEATURES

- 32,768 x 8 Organization
- Single +5 Volt Supply
- Maximum 300ns Access Time
- Totally Static Operation
- Three State Outputs
- All TTL Compatible Inputs/Outputs
- 28 Pin JEDEC and MOSTEK Standard Pinout

DESCRIPTION

The General Instrument RO9256 is a 262,144 Bit Static Read Only Memory organized as 32,768 by 8-bit and is ideally suited for microprocessor memory applications. Fabricated with General Instrument N-Channel Silicon Gate Technology, the RO9256 provides the designer with a high performance, easy to use MOS circuit featuring operation from a single +5 Volt power supply and low power dissipation.

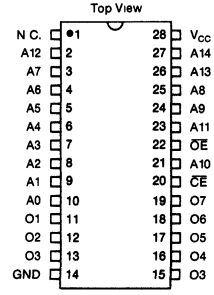
The RO9256 offers a power down feature controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high.

An additional feature of Output Enable ($\overline{OE}$) function eliminates bus contention in multiple bus microprocessor systems.

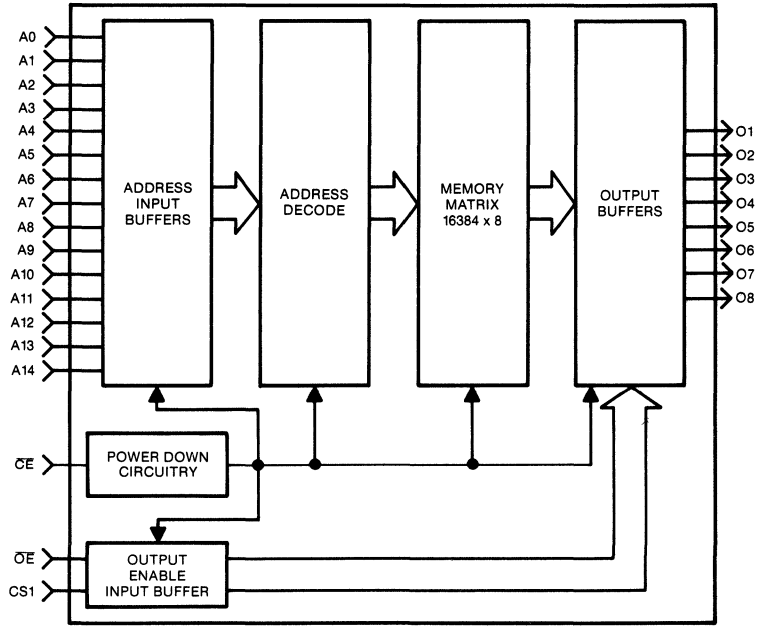
PIN CONFIGURATION

28 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



20K Cartridge ROM

FEATURES

- Mask Programable Storage Providing 2048 x 10 Bit Words
- 16 Bit On-Chip Address Latch
- Memory Map Circuitry to Place the 2K ROM Page Within a 65K Memory Area
- 16 Bit Tri-State Bus with Higher 6 Bits Driven to Zero During Read Operations

CIRCUIT REQUIREMENTS

The RO-3-9504 operates as the program memory for systems using a CP1610 microprocessor. It is configured as 2048 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

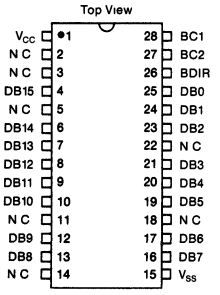
DESCRIPTION

From initialization, the RO-3-9504 waits for the first address code i.e., BAR. For this address code and all subsequent address sequences, the 9504 reads the 16-bit external bus and latches the value into its address register.

The 9504 contains a programable memory map location for its own 2K page, and if a valid address is detected, the particular address location will transfer its contents to the chip output buffers. If the control code following the address cycle was a READ, the 9504 will output the 10 bits of addressed data and drive a logic zero on the top six bits of the bus.

PIN CONFIGURATION

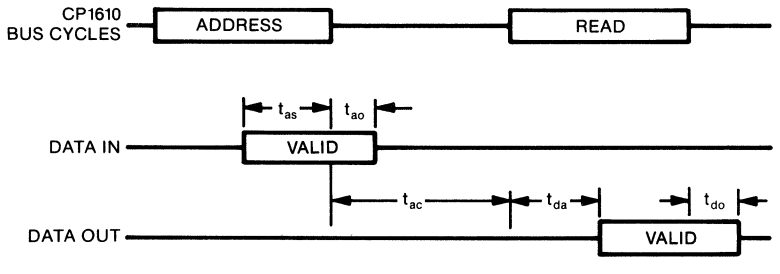
28 LEAD DUAL IN LINE



INPUT CONTROL SIGNALS

BDIR	BC1	BC2	Equivalent Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = High Impedance
0	0	1	IAB	No Action
0	1	0	ADAR	Address Data to Address Register, D0-D15 = High Impedance
0	1	1	DTB (READ)	Data To Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	No Action
1	1	0	DW	No Action
1	1	1	INTAK	INTerrupt AcKnowledge

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to 100°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with Respect to V_{SS} ..... −0.2V to +9.0V

Standard Conditions (unless otherwise stated):

T_A = 0°C to +55°C
V_{CC} = +4.85V − +5.15V
V_{SS} = 0.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Max	Units	Conditions
Inputs					
Input Logic Low	V_{IL}	0	0.7	V	
Input Logic High	V_{IH}	2.4	V_{CC}	V	
Input Leakage	V_{IL}	—	5	μA	V_{IN} = 0V to V_{CC}
Capacitance	—	—	10	pf	V_{IN} = 0V
CPU BUS Outputs					
Output Logic Low	V_{OL}	0	0.5	V	I_{OL} = 1.5mA +150pf
Output Logic High	V_{OH}	2.4	V_{CC}	V	I_{OH} = −200μA
Supply Current					
V_{CC} Supply	I_{CC}	—	120	mA	25°C

AC CHARACTERISTICS

Characteristics	Sym	Min	Max	Units	Conditions
Inputs					
Address Set Up	t_{as}	400	—	ns	
Address Overlap	t_{ao}	65	—	ns	
CPU BUS Outputs					
Turn ON Delay	t_{da}	—	350	ns	
Turn OFF Delay	t_{do}	85	—	ns	
Access Time	t_{ac}	—	1.5	μs	

READ ONLY MEMORY

40K Cartridge ROM

FEATURES

- Mask Programable Storage Providing 4096 x 10 Bit Words
- 16 Bit On-Chip Address Latch
- Control Decoder
- Programable Memory Map Circuitry to Place 4K ROM Page Within 65K Word Memory Space Located on 4K Page Boundaries

REQUIREMENTS

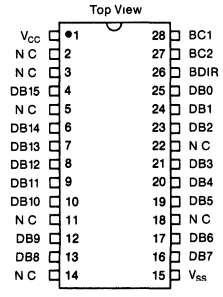
The RO9508 operates as the program memory for systems using a CP1600 series microprocessor. It is configured as 4096 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

DESCRIPTION

The RO9508 contains a programable memory map location for its own 4K page and if a valid address is detected, the particular addressed location will transfer its contents to the chip output buffers. If the control code following the address cycle was a Read, the RO9508 will output the 10 bits of addressed data and also drive a logic zero on the top 6 bits of the bus.

PIN CONFIGURATION

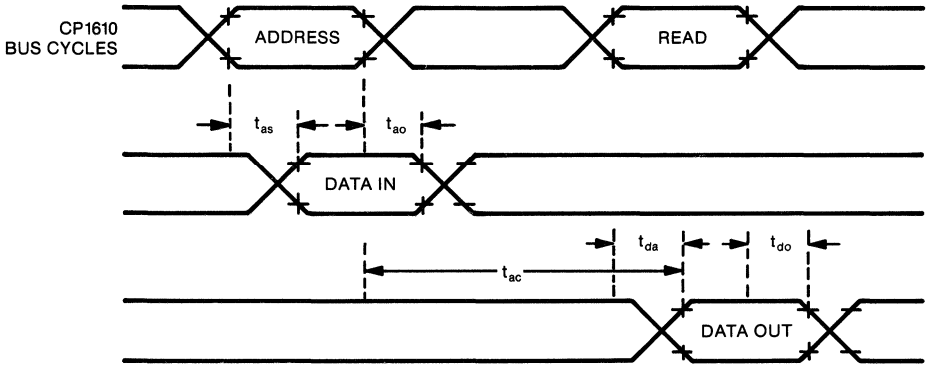
28 LEAD DUAL IN LINE



BUS CONTROL SIGNALS

BDIR	BC2	BC1	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = High Impedance
0	0	1	ADAR	Address Data to Address Register, D0-D15 = High Impedance
0	1	0	IAB	No Action
0	1	1	DTB	Data To Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DW	No Action
1	1	0	DWS	No Action
1	1	1	INTAK	INTerrupt AcKnowledge

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +100°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with Respect to V_{SS} ..... −0.2V to +9.0V

Standard Conditions (unless otherwise noted):

Ambient Temperature 0°C to +55°C
V_{CC} = +4.85V to +5.15V
V_{SS} = 0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Inputs						
Input Logic Low	V_{IL}	0	—	0.7	V	
Input Logic High	V_{IH}	2.4	—	V_{CC}	V	
Input Leakage	V_{IL}	—	—	5	μA	V_{IN} = 0V to V_{CC}
CPU Bus Outputs						
Output Logic Low	V_{OL}	0	—	0.5	V	I_{OL} = 1.5mA
Output Logic High	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 80μA
Supply Current						
V_{CC} Supply	I_{CC}	—	—	120	mA	V_{CC} = 5.15V @ 25°C

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Inputs						
Address Set Up	t_{AS}	300	—	—	ns	
Address Overlap	t_{AO}	—	—	65	ns	
CPU Bus Outputs						
Turn ON Delay	t_{DA}	—	—	350	ns	
Turn OFF Delay	t_{DO}	85	—	—	ns	
Access Time	t_{AC}	—	—	1.5	μs	

80K Cartridge ROM

FEATURES

- Mask Programable Storage Providing 8192 x 10 Bit Words
- 16 Bit On-Chip Address Latch
- Control Decoder
- Programable Memory Map Circuitry to Place 8K ROM Page Within 65K Word Memory Space Located on Two Independent 4K Boundaries

CIRCUIT REQUIREMENTS

The RO9580 operates as the program memory for systems using a CP1600 series microprocessor.

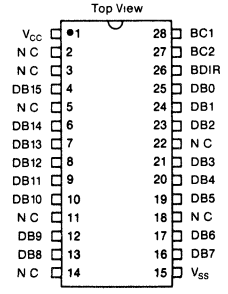
It is configured as 8192 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

DESCRIPTION

The RO9580 contains a programable memory map location for its own 8K page and if a valid address is detected, the particular addressed location will transfer its contents to the chip output buffers. If the control code following the address cycle was a Read, the RO9580 will output the 10 bits of addressed data and also drive a logic zero on the top 6 bits of the bus.

PIN CONFIGURATION

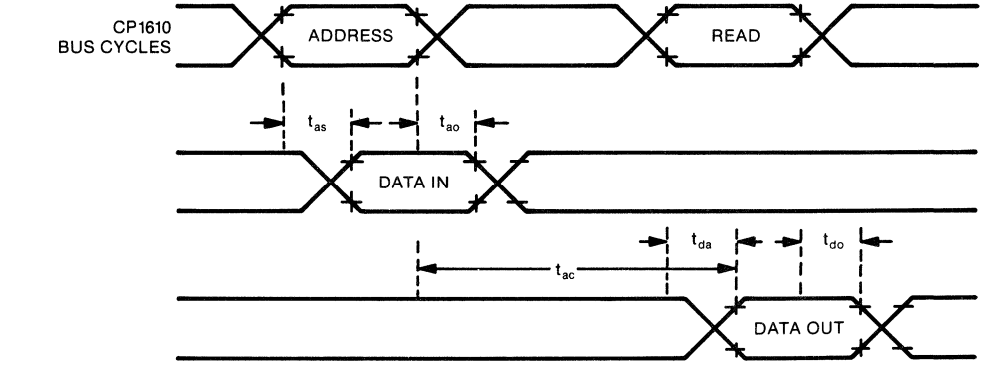
28 LEAD DUAL IN LINE



BUS CONTROL SIGNALS

BDIR	BC2	BC1	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = High Impedance
0	0	1	ADAR	Address Data to Address Register, D0-D15 = High Impedance
0	1	0	IAB	No Action
0	1	1	DTB	Data To Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DW	No Action
1	1	0	DWS	No Action
1	1	1	INTAK	INTerrupt AcKnowledge

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +100°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +12V
V_{CC} with Respect to V_{SS} ..... −0.2V to +12V

Standard Conditions (unless otherwise noted):

Ambient Temperature: −40°C to +85°C
V_{CC} = +4.50V to +5.50V,
V_{SS} = 0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Inputs						
Input Logic Low	V_{IL}	0	—	0.8	V	
Input Logic High	V_{OH}	2	—	V_{CC}	V	
Input Leakage	V_{IL}	—	—	5	μA	V_{IN} = 0V to V_{CC}
CPU Bus Outputs						
Output Logic Low	V_{OL}	0	—	0.4	V	I_{OL} = 1.6mA
Output Logic High	V_{OH}	2 4	—	V_{CC}	V	I_{OH} = 100μA
Supply Current						
V_{CC} Supply	I_{CC}	—	—	75	mA	

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Inputs						
Address Set Up	t_{AS}	300	—	—	ns	
Address Overlap	t_{AO}	50	—	65	ns	
CPU Bus Outputs						
Turn ON Delay	t_{DA}	—	—	300	ns	
Turn OFF Delay	t_{DO}	80	—	250	ns	
Access Time	t_{AC}	—	—	1 5	μs	

160K Cartridge ROM

FEATURES

- Mask Programable Storage Providing 16,384 x 10 Bit Words
- 16 Bit On-Chip Address Latch
- Control Decoder
- Programable Memory Map Circuitry to Place 16K ROM Page Within 65K Word Memory Space Located on Four Independent 4K Boundaries

REQUIREMENTS

The RO9160 operates as the program memory for systems using a CP1600 series microprocessor.

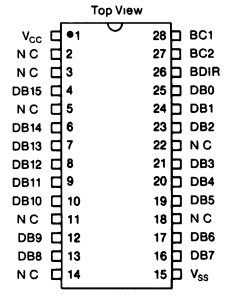
It is configured as 16K x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

DESCRIPTION

The RO9160 contains a programable memory map location for its own 16K page and if a valid address is detected, the particular addressed location will transfer its contents to the chip output buffers. If the control code following the address cycle was a Read, the RO9160 will output the 10 bits of addressed data and also drive a logic zero on the top 6 bits of the bus.

PIN CONFIGURATION

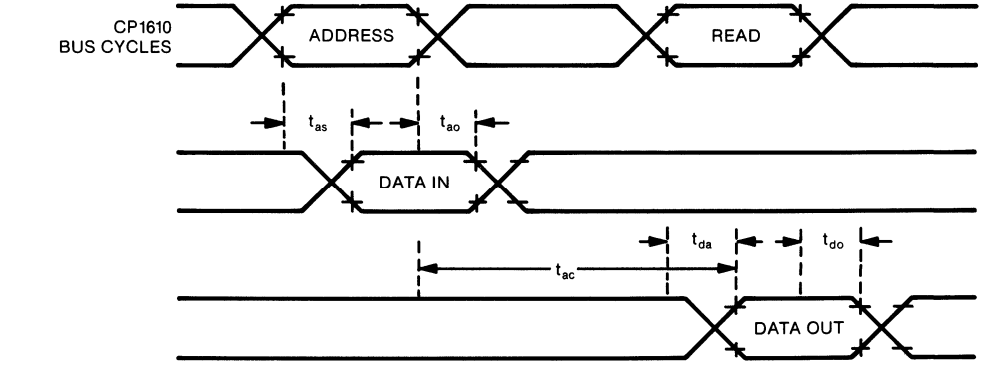
28 LEAD DUAL IN LINE



BUS CONTROL SIGNALS

BDIR	BC2	BC1	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = High Impedance
0	0	1	ADAR	Address Data to Address Register, D0-D15 = High Impedance
0	1	0	IAB	No Action
0	1	1	DTB	Data To Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DW	No Action
1	1	0	DWS	No Action
1	1	1	INTAK	INTerrupt AcKnowledge

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +100°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +12V
V_{CC} with Respect to V_{SS} ..... −0.2V to +12V

Standard Conditions (unless otherwise noted):

Ambient Temperature: −40°C to +85°C
V_{CC} = +4.50V to +5.50V
V_{SS} = 0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Inputs						
Input Logic Low	V_{IL}	0	—	0.8	V	
Input Logic High	V_{IH}	2	—	V_{CC}	V	
Input Leakage	V_{IL}	—	—	5	μA	V_{IN} = 0V to V_{CC}
CPU Bus Outputs						
Output Logic Low	V_{OL}	0	—	0.4	V	I_{OL} = 1.6mA
Output Logic High	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 100μA
Supply Current						
V_{CC} Supply	I_{CC}	—	—	75	mA	

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Inputs						
Address Set Up	t_{AS}	300	—	—	ns	
Address Overlap	t_{AO}	50	—	65	ns	
CPU Bus Outputs						
Turn ON Delay	t_{DA}	—	—	300	ns	
Turn OFF Delay	t_{DO}	80	—	250	ns	
Access Time	t_{AC}	—	—	1.5	μs	

GENERAL INSTRUMENT

Keyboard Encoder

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
CAPACITIVE KEYBOARD ENCODER	4,592 bits organized as 112 keys x 4 modes x 10 bits, plus 112 bits for internal programing of function keys.	AY-3-4592	2-42

READ ONLY MEMORY

Capacitive Keyboard Encoder

FEATURES

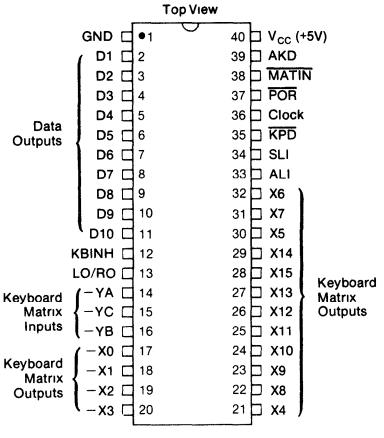
- 128 Key Keyboard Encoder: 112 Fully Decoded Keys, 16 Discrete Function Keys
- 112 Keys With 4 Modes, 10 Bit Output
- Key Validation Logic Protects Against Bounce
- N-Key Roll Over or 2-Key Roll Over
- Internal ROM Allows Any Keys to Control SHIFT CTRL, SHIFT LOCK and ALPHA LOCK
- ALPHA LOCK and SHIFT LOCK Indicator Lines
- Any Key Down (AKD) Strobe
- Single +5 Volt Power Supply
- Programable Coding of Standard and Special Function Keys
- Zener Diode Protection on All I/O Pins
- Low Power Consumption, Less Than 2 MW per Key
- Usable with Capacitive, Magnetic, Inductive, Hall Effect, or Mechanical Keyboard Switches
- Inputs and Outputs TTL and CMOS Compatible
- Internal Oscillator

DESCRIPTION

The General Instrument AY-3-4592 is a unique dual pulse scanning encoder and keyboard controller for 112 keys in four modes and 16 programable discrete function keys. ROM programing permits any keys to control the shift control and lock functions The AY-3-4592 can be used with capacitive, inductive (magnetic) or switch closure type switches since it works on pulse detection.

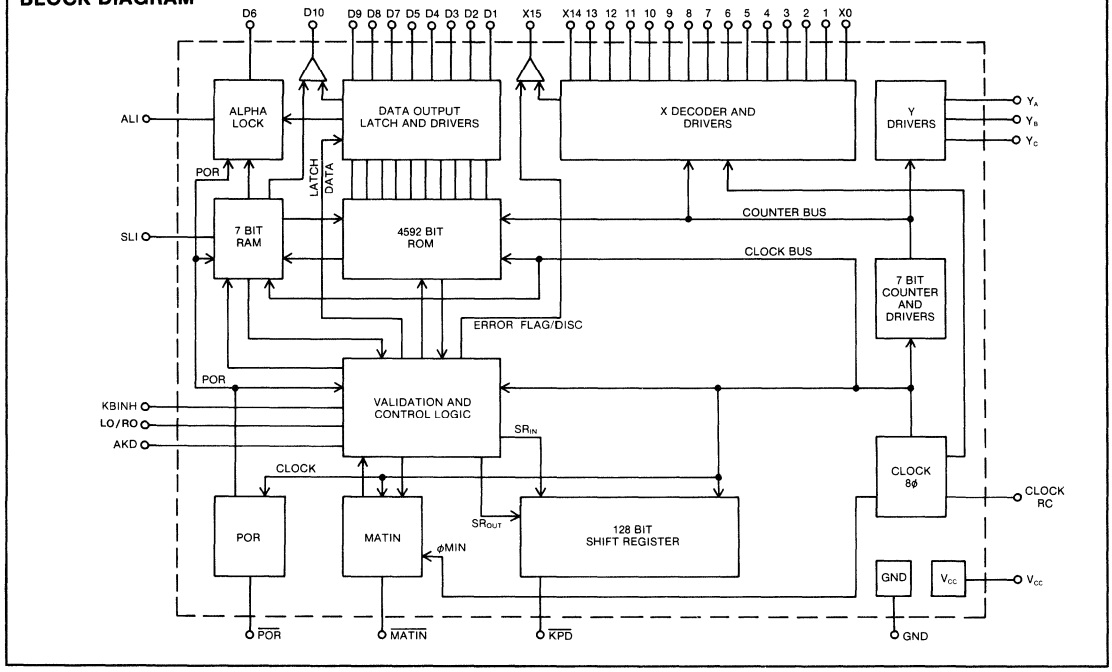
PIN CONFIGURATION

40 LEAD DUAL IN LINE



The AY-3-4592 is fabricated with General Instrument N-Channel MOS technology on a single chip containing a 4592 bit ROM, a 128 bit shift register and an internal oscillator.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Symbol	Function
1	Ground	GND	Ground Pin
2-10	Data Out	D1-D9	Data Outputs, D1 through D9
11	Data Out	D10	Data Output D10. See AY-3-4592 options for complete description
12	Key Inhibit	KBINH	Logic "1" on KBINH will inhibit the processing of Key closures and prevent new output codes. See AY-3-4592 options for other custom options.
13	Lockout/rollover	LO/RO	High for 2 Key Rollover operation, low for N Key Rollover operation. This input is a high impedance Schmitt trigger with thresholds of approximately ¼ (low) and ¾ (high) of V_{CC}. This allows easy interfacing with very slow RC circuits for such functions as "repeat delay". LO/RO is internally "anded" with AKD/STB; if either is low, N Key rollover is automatically selected.
14-16	Y-Address	YA, YB, YC	Y Address lines select one of eight Y inputs through external multiplexer. Scan sequence is Y7 to Y0
17-27, 30-32	X Outputs	X0-X13, X5-X7	X output drivers for Matrix scanning. Scan sequence is X15 to X0. Each driver generates 8 pairs of pulses each scanning cycle.
28, 29	X15, 14	X15, X14	X15 is programed as a "discrete output" key in the standard part. Optionally it may be programed as an error flag or as a Matrix drive line. See AY-3-4592 options. Unlike X0-X13, neither X14 nor X15 have associated ROM output codes. These lines are used to enable separate discrete keys to be debounced using an addressable latch as illustrated in figure 2.
33	Alpha Lock Indicator	ALI	ALI will indicate if op code XX101 is selected. (See operation codes). In the standard device there is no other function. If alpha lock is selected as an option, op code XX101 will result in bit 6 being replaced by bit 9 when a key is depressed.
34	Shift Lock Indicator	SLI	SLI will indicate if op code XX011 is selected (see operation codes). In the standard device this op code will also select the shift lock function.
35	Key Pressed	$\overline{KPD}$	$\overline{KPD}$ is used to shift the threshold of the external sense amplifier in order to provide hysteresis to improve noise immunity. In addition $\overline{KPD}$ may be inverted to provide the data input to the 8 bit latches for decoding X14 and X15. When a key closure is detected $\overline{KPD}$ is generated causing the 8 bit latch output to go high. See figure 2.
36	CLOCK	CLK	Resistor/capacitor tie point for the internal oscillator. Nominal frequencies and scan times are shown below:
37	Reset	$\overline{POR}$	Reset clears all internal registers and flip flops. Suggested circuit for power on reset is illustrated in Figure 1.
38	Matrix Input	$\overline{MATIN}$	Input from external multiplexer. Senses signal from X-Y scan of depressed key.
39	Any Key Down Strobe	AKD	AKD is low when no key is depressed. When a key is depresed AKD goes high. If, while one key is held, a second key is depressed, AKD will go low for 2 clock cycles.
40	Power	V_{CC}	Power supply +5V input

	C = 150pf		C = 220pf		C = 500pf	
R	Freq	Scan time	Freq	Scan time	Freq	Scan time
5K	1 3 MHz	1 5 msec	1 2 MHz	1 7 msec	71 MHz	2 8 msec
10K	8 MHz	2 3 msec	.8 MHz	2 7 msec	45 MHz	4 3 msec
25K	4 MHz	4 8 msec	3 MHz	6 0 msec	20 MHz	10 0 msec

OPERATION

Keys are connected in a 16 x 8 matrix. Scanning of the matrix is performed by the encoder in conjunction with an external, multiplexer. The encoder provides a 3 bit binary address (YA, YB, YC) used to scan each of eight possible sense lines (Y-lines). The drive lines (X-lines) are each pulsed low by the encoder. If a key is closed, the pulse is coupled from the drive to the sense lines, amplified, and sent to the encoder. When used to encode reactive switches, a detection circuit is necessary between the output of the multiplexer and the $\overline{\text{MATIN}}$ input to the encoder. In this manner, each matrix cross-point is interrogated in turn. Each matrix cross-point is given a unique binary code that is determined by the internal scan counters. This code is used to address a ROM which generates the output codes (such as ASCII or other customer defined codes). The output of the ROM is entered into an output holding register when the key is determined to be a valid key closure. Only the cross-points on X0 through X13 can have output codes: X14 and X15 can be used for scanning discrete keys.

An internal oscillator controls the matrix scanning rate. The minimum scanning time is 1.7 ms, at a 1.2 MHz clock. This allows a burst typing speed equivalent to over 250 words/min. When a key is depressed, a matrix address from an X driver and Y input line representing that key is loaded into a 7 bit latch. On the second keyboard scan, the matrix address and the stored address are compared. If the two addresses match, the ROM 10 bit word at that address is loaded into the data holding register. This data remains valid until the next key is depressed. The internal error flag is set, if this option was utilized, whenever there is a mismatch between 7 bit addresses.

Two negative pulses must be detected during the $\overline{\text{MATIN}}$ timing window for the depression to be recognized.

Keyboard Selection

The AY-3-4592 keyboard encoder can be used with a wide variety of available keyboards. An external multiplexing circuit and one external sense amplifier can be tailored to the user's specific requirements. As shown in Figure 1, the sense amplifier detects changes in voltage caused by variations in the switch impedance as a key is depressed and released. Given the key switch impedances for depressed and released states, the values of Rx and Rh can be chosen to guarantee switch closure detection and noise margins. Rx is chosen to match the capacitor or reactor time constants. For example, given a variable capacitance keyboard switch with C1 = 100pf, and C2 = 10pf for depressed and released positions respectively, with a 1.5MHz oscillator and Rx = 10 Kohm, a depressed key would make a 4.7 volt pulse while a raised key would produce a 2.6 volt pulse. The potentiometer would then be set for best noise immunity with minimum pulse width, 90ns for all keys. The hysteresis resistor, Rh, is chosen at roughly ten times the value of Rx to provide increased noise immunity for detected key depressions.

Operation Codes

Depending on the internal programing of the AY-3-4592, keys may have one of three different functions. Keys on matrix line X0 through X13 have, in addition to the output code bits, a function flag bit (FFB). If the FFB is programed as a zero, the key produces a data output when depressed.

When FFB is a one, the key is a "function" key for which bits 1-5 determine the function. These bits are referred to as the op code and are used to provide special functions such as shift, shift lock, alpha lock, etc. Bits 6-10 are not used.

Op codes may be programed to provide data outputs as well as change the mode of operation Data when outputted is not latched as are normal coded outputs.

Bits 1-3 indicate what operation the key will perform; per table 1.

Bit 4 programed as one indicates a down-coded key, for which the 10 data bits programed in the shift mode level of ROM are outputted when the key is depressed.

Bit 5 programed as one indicates an up-coded key for which the 10 data bits programed in the control mode level of ROM are outputted when the key is released.

Neither bit 4 nor 5 will have any effect on the operational control of bits 10-3.

Table 1

Op-Code 5	4	3	2	1	Function
X	X	0	0	0	Function key (with up/down codes)*
X	X	0	0	1	Right Shift Key
X	X	0	1	0	Left Shift Key
X	X	0	1	1	Shift Lock Key or Discrete Key (output SLI)
X	X	1	0	0	Control Key
X	X	1	0	1	Alpha Lock Key or Discrete Key (output ALI)
X	0	1	1	0	Error Reset Key or discrete key (output X15)
X	X	1	1	1	Discrete Key (output D10)

*If the op-code is 00000 the key has no internal function but $\overline{\text{KPD}}$ will go low when it is processed.

OPTIONS

Pin or Function	Option
X15	X15 may be programed as 1) an X-output to provide a second set of 8 discrete lines 2) a discrete output which indicates when a function key with op code XX110 is depressed 3) an Error Flag Indicator (EFI). See Error Flag In the AY-3-4592 STD X15 is a discrete output
Error Flag	When this option is selected, the AY-3-4592 has the capability of detecting multiple key depressions during the same scan cycle. When selected, the error flag may be programed to generate KBINH and or appear at the X15 output. The error flag may be reset by three methods. If the automatic reset is selected/the flag will be reset when the error causing Key is released. Op-code XX110 may be programed on a function key to reset the error flag. If pin 12 is programed for KBINH error flag will be reset by pulsing pin 12 high. The reset will occur on the negative edge of the KBINH signal; the pulse must be at least 16 clock cycles. Error flag causes KBINH and is automatically reset.
Alpha Lock	When programed for Alpha lock, the function key with op-code XX101 will cause the bit 6 output to be replaced by bit 9. Bit 9 is not altered. Alpha lock is normally used to force printing of upper case characters irrespective of the shift function. Op Code XX101 will also cause an output on ALI (pin 33). When Alpha lock is not programed, op code XX101 will result in an output on ALI (pin 33). Op code XX101 may be programed for momentary action, or latched push-on, push-off alternating action. ALI may be programed for normally low or high output. Op code XX101 is momentary action. ALI is normally low. The AY-3-4592 STD is not programed for Alpha lock, although there will be an output on ALI.
Shift Lock	When programed for shift lock, the function key with op-code XX011 will cause normal electronic shift action. Op code XX011 will also cause an output on SLI (pin 34). If shift lock is not programed, op code XX011 will simply cause an output on SLI. SLI may be programed for normally low or high output. The AY-3-4592 STD is programed for shift lock operation with SLI normally low.
KBINH	KBINH, Keyboard Inhibit, may be programed to be caused by Pin 12 high, by the error flag, or both. In addition, function keys with up or down codes may be programed, as a group, to be inhibited by KBINH. This is the KCI Out option. When pin 12 is programed to cause KBINH, a high input on pin 12 will inhibit processing of common keys. If a key is depressed while the KBINH signal is present, output and output strobe will be generated when KBINH is released. The AY-3-4592 STD has KBINH actuated by pin 12 high, and by the error flag. The KCI In option is used, that is, the function key operation is independent of KBINH.
D10	D10, pin 11, may be programed as the output for the memory bit 10 or as a discrete output. As a discrete output, pin 10 is switched from its normal state (programable as high or low) by the function key with op-code XX111. The AY-3-4592 STD is programed for D10 as a discrete key, normally low.
Key Type	Keys may be either normally open or normally closed. The AY-3-4592 STD is designed for normally open keys.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} ..... -0.3 Volts to +7.0 Volts
Maximum voltage with respect to V_{CC} ..... +0.3 Volts
Storage Temperature ..... 65°C to +150°C
Operating Temperature ..... 0 to 70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

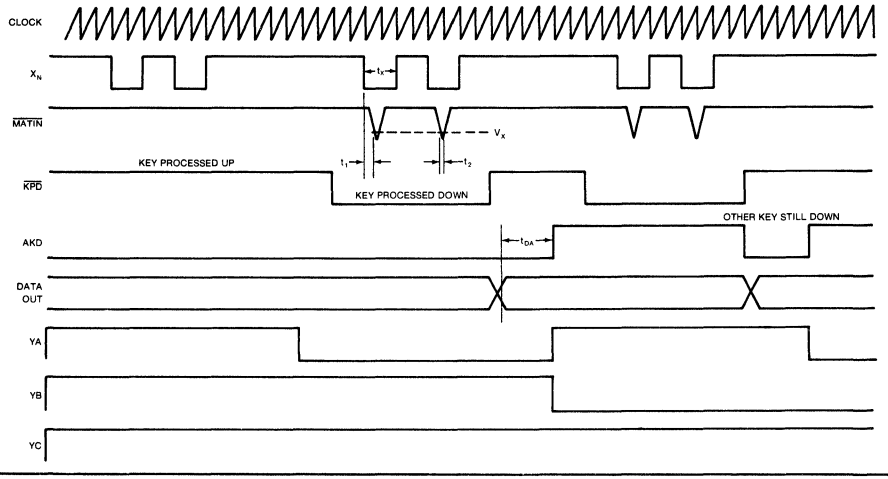
Standard Conditions (unless otherwise noted)

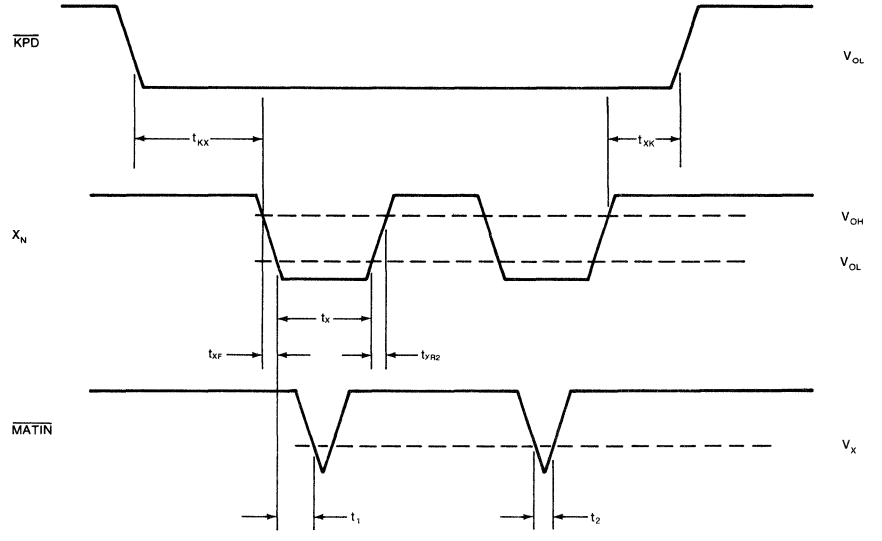
V_{CC} = 5.0V ±5%
T_A = 0° to 70°C

Characteristic	Symbol	Min.	Typ.**	Max.	Unit	Condition
Data Output "1" Voltage	V_{OH}	3.5	-	-	V	I_{OH} = 50μA, 25pf
Data Output "0" Voltage	V_{OL}	-	-	0.5	V	I_{OL} = 1.6mA
All Inputs "1" Voltage	V_{IH}	2.2	-	-	V	except $\overline{POR}$, 2KRO
All Inputs "0" Voltage	V_{IL}	-	-	0.8	V	except $\overline{POR}$, 2KRO
All Inputs Leakage	I_{IH}	-	-	10	μA	V_{in} = 5V
X Output "1" Voltage	X_{OH}	3.5	-	-	V	I_{OH} = 50μA, 100pf
X Output "0" Voltage	X_{OL}	-	-	0.5	V	I_{OL} = 1.6mA
AKd Output Voltage	V_A	-	-	0.6	V	I_{OL} = 3.2mA
$\overline{MATIN}$ Input Voltage	V_X	-	-	0.4	V	
$\overline{POR}$, 2KRO high threshold	V_{SH}	-	1.3	-	V	Schmitt trigger
$\overline{POR}$, 2KRO low threshold	V_{SL}	-	3.7	-	V	Schmitt trigger
Power Supply Current	I_{CC}	-	35	60	mA	Vcc = 5.3V
Clock Frequency	ϕ	200	-	1200	kHz	
Matrix Delay	t_1	-	-	250	ns	
Input pulse width	t_2	90	-	-	ns	
X Output pulse width	t_x	1.7	-	-	μs	
X Output fall time	t_{XF}	-	-	150	ns	V_{OH} = 4.3V, V_{OL} = 0.4V
X Output rise time	t_{XR1}	-	-	150	ns	V_{OH} = 2.4V, V_{OL} = 0.4V
X Output rise time	t_{XR2}	-	-	500	ns	V_{OH} = 3.5V, V_{OL} = 0.4V
X Output rise time	t_{XR3}	-	-	1500	ns	V_{OH} = 4.3V, V_{OL} = 0.4V
$\overline{KPD}$-X Output set time	T_{KX}	500	-	-	ns	
X Output-$\overline{KPD}$ hold time	t_{XK}	100	-	-	ns	
Data out to AKD time	t_{OA}	1.7	-	-	μs	

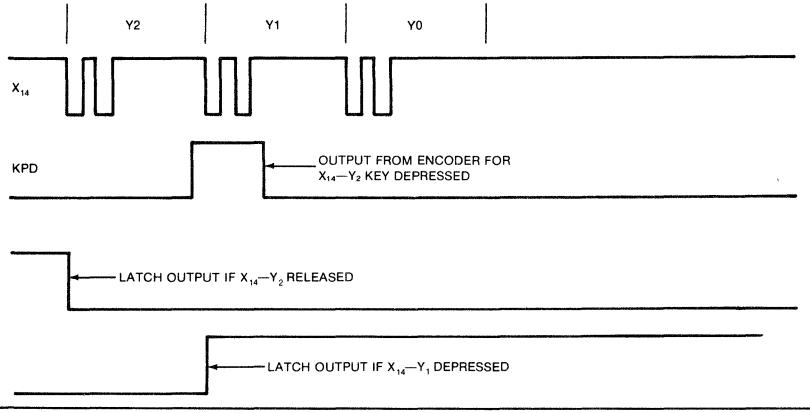
**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS





Discrete Function Key



CODE CHART / AY-3-4592-STD

XXY	F	NORMAL			SHIFT			CONTROL			SHIFT/CONTROL		
	B	HEX	BINARY		HEX	BINARY		HEX	BINARY		HEX	BINARY	
000	1	001	0000000001	Right Shift	3FF	1111111111		3FF	1111111111		3FF	1111111111	
001	1	002	0000000010	Left Shift	3FF	1111111111		3FF	1111111111		3FF	1111111111	
002	1	003	0000000011	Shift Lock	3FF	1111111111		3FF	1111111111		3FF	1111111111	
003	1	004	0000000100	Control	3FF	1111111111		3FF	1111111111		3FF	1111111111	
004	1	005	0000000101	ALI	3FF	1111111111		3FF	1111111111		3FF	1111111111	
005	1	006	0000000110	X15	3FF	1111111111		3FF	1111111111		3FF	1111111111	
006	1	007	0000000111	D10	3FF	1111111111		3FF	1111111111		3FF	1111111111	
007	0	0CE	0011001110	1	0DE	0011011110	!	0CE	0011001110	!	0DE	0011011110	!
010	0	1E4	0111100100	ESC	1E4	0111100100	ESC	1E4	0111100100	ESC	1E4	0111100100	ES
011	0	0CD	0011001101	2	1BF	0110111111	@	0CD	0011001101	2	1FF	0111111111	NUL
012	0	0CD	0011001101	2	0DD	0011011101	"	0CD	0011001101	2	0DD	0011011101	"
013	0	1B8	0110001000	W	1A8	0110101000	W	1E8	0111101000	ETB	1E8	0111101000	ETB
014	0	1BE	0110001110	9	1AE	0110101110	Q	1EE	0111101110	DC1	1EE	0111101110	DC1
015	0	18C	0110001100	S	1AC	0110101100	S	1EC	0111101100	DC3	1EC	0111101100	DC3
016	0	19E	0110011110	a	18E	0110111110	A	1FE	0111111110	SOH	1FE	0111111110	SOH
017	0	185	0110000101	Z	1A5	0110100101	Z	1E5	0111100101	SUB	1E5	0111100101	SUB
020	0	17F	0101111111	NUL	17F	0101111111	NUL	17F	0101111111	NUL	17F	0101111111	NUL
021	0	0CB	0011001011	4	0DB	0011011011	$	0CB	0011001011	4	0DB	0011011011	$
022	0	0CC	0011001100	3	0DC	0011011100	#	0CC	0011001100	3	0DC	0011011100	#
023	0	1BD	0110001101	r	1AD	0110101101	R	1ED	0111101101	DC2	1ED	0111101101	DC2
024	0	19A	0110011010	e	18A	0110111010	E	1FA	0111111010	ENQ	1FA	0111111010	ENQ
025	0	198	0110011011	d	188	0110111011	D	1F8	0111111011	EOT	1F8	0111111011	EOT
026	0	187	0110000111	x	1A7	0110100111	X	1E7	0111100111	ETB	1E7	0111100111	ETB
027	0	19C	0110011100	c	1BC	0110111100	C	1FC	0111111100	ETX	1FC	0111111100	ETX
030	0	17E	0101111110	SOH	17E	0101111110	SOH	17E	0101111110	SOH	17E	0101111110	SOH
031	0	17D	0101111101	STX	17D	0101111101	STX	17D	0101111101	STX	17D	0101111101	STX
032	0	0CA	0011001010	5	0DA	0011011010	%	0CA	0011001010	5	0DA	0011011010	%
033	0	18B	0110001011	t	1A8	0110101011	T	1EB	0111101011	DC4	1EB	0111101011	DC4
034	0	199	0110011001	f	1B9	0110111001	F	1F9	0111111001	ACK	1F9	0111111001	ACK
035	0	198	0110011000	g	1B8	0110111000	G	1F8	0111111000	BEL	1F8	0111111000	BEL
036	0	189	0110001001	v	1A9	0110101001	V	1E9	0111101001	SYN	1E9	0111101001	SYN
037	0	19D	0110011101	b	1BD	0110111101	B	1FD	0111111101	STX	1FD	0111111101	STX
040	0	17C	0101111100	ETX	17C	0101111100	ETX	17C	0101111100	ETX	17C	0101111100	ETX
041	0	0C8	0011001000	7	0D9	0011011001	¿	0C8	0011001000	7	0D9	0011011001	¿
042	0	0C9	0011001001	6	0D9	0011011001	¿	0C9	0011001001	6	0D9	0011011001	¿
043	0	186	0110000110	y	1A6	0110100110	Y	1E6	0111100110	EM	1E6	0111100110	EM
044	0	197	0110010111	h	1B7	0110110111	H	1F7	0111110111	BS	1F7	0111110111	BS
045	0	191	0110010001	n	1B1	0110110001	N	1F1	0111110001	SO	1F1	0111110001	SO
046	0	0C9	0011001001	6	0C3	0011000011	<	0C9	0011001001	6	0C3	0011000011	<
047	0	0DF	0011011111	SP	0DF	0011011111	SP	0DF	0011011111	SP	0DF	0011011111	SP
050	0	17B	0101111011	EOT	17B	0101111011	EOT	17B	0101111011	EOT	17B	0101111011	EOT
051	0	0C7	0011000111	8	0D5	0011010101	*	0C7	0011000111	8	0D5	0011010101	*
052	0	0C8	0011001000	7	0D8	0011011000	'	0C8	0011001000	7	0D8	0011011000	
053	0	18A	0110001010	u	1AA	0110101010	u	1EA	0111101010	NAK	1EA	0111101010	NAK
054	0	195	0110010101	J	1B5	0110110101	J	1F5	0111110101	ENQ	1F5	0111110101	ENQ
055	0	194	0110010100	k	1B4	0110110100	K	1F4	0111110100	VT	1F4	0111110100	VT
056	0	192	0110010010	m	1B2	0110110010	M	1F2	0111110010	CR	1F2	0111110010	CR
057	0	0D3	0011010011	.	0C3	0011000011	<	0D3	0011010011		0C3	0011000011	<
060	0	17A	0101111010	ENQ	17A	0101111010	ENQ	17A	0101111010	ENQ	17A	0101111010	ENQ
061	0	0C6	0011000110	9	0D7	0011010111	(	0C6	0011000110	9	0D7	0011010111	(
062	0	0C7	0011000111	8	0D7	0011010111	(	0C7	0011000111	8	0D7	0011010111	(
063	0	196	0110010110	i	1B6	0110110110	I	1F6	0111110110	HT	1F6	0111110110	HT
064	0	190	0110010000	o	1B0	0110110000	O	1F0	0111110000	SI	1F0	0111110000	SI
065	0	194	0110010100	K	1A4	0110100100	[	1F4	0111110100	VT	1E4	0111100100	ESC
066	0	193	0110010011	l	1B3	0110110011	L	1F3	0111110011	FF	1F3	0111110011	FF
067	0	192	0110010010	m	1A2	0110100010	]	1F2	0111110010	CR	1E2	0111100010	GS
070	0	179	0101111001	ACK	179	0101111001	ACK	179	0101111001	ACK	179	0101111001	ACK
071	0	0CF	0011001111	ø	0D6	0011010110	)	0CF	0011001111	ø	0D6	0011010110	)
072	0	0C6	0011000110	9	0D6	0011010110	)	0C6	0011000110	9	0D6	0011010110	)
073	0	178	0101111000	BEL	178	0101111000	BEL	178	0101111000	BEL	178	0101111000	BEL

CODE CHART / AY-3-4592-STD

XXY	F B	NORMAL HEX	NORMAL BINARY		SHIFT HEX	SHIFT BINARY		CONTROL HEX	CONTROL BINARY		SHIFT/CONTROL HEX	SHIFT/CONTROL BINARY	
074	0	18F	01100011111	P	1AF	01101011111	P	1EF	01111101111	DLE	1EF	01111101111	DLE
075	0	0C4	0011000100	:	0C5	0011000101	:	0C4	0011000100	;	0C5	0011000101	:
076	0	193	0110010011	L	1A3	0110100011	\	1F3	0111110011	FF	1E3	0111100011	FS
077	0	0D1	0011010001	.	0C1	0011000001	>	0D1	0011010001	.	0C1	0011000001	>
080	0	0D2	0011010010	–	1A0	0110100000	–	0D2	0011010010	–	1A0	0110100000	–
081	0	191	0110010001	n	1A1	0110100001	^	1F1	0111110001	SI	1E1	0111100001	RS
082	0	18F	0110001111	P	1BF	0110111111	@	1EF	0111101111	DLE	1FF	0111111111	NUL
083	0	1A4	0110100100	[	1A2	0110100010	]	1E4	0111100100	ESC	1E2	0111100010	GS
084	0	0D8	0011011000	'	0DD	0011011101	"	0D8	0011011000	'	0DD	0011011101	"
085	0	0C4	0011000100	,	0D4	0011010100	+	0C4	0011000100	;	0D4	0011010100	+
086	0	0D0	0011010000	/	0C0	0011000000	?	0D0	0011010000	/	0C0	0011000000	?
087	0	177	0101110111	BS	177	0101110111	BS	177	0101110111	BS	177	0101110111	BS
090	0	0C2	0011000010	=	0D4	0011010100	+	0C2	0011000010	=	0D4	0011010100	+
091	0	0C5	0011000101		0D5	0011010101	*	0C5	0011000101		0D5	0011010101	*
092	0	176	0101110110	HT	176	0101110110	HT	176	0101110110	HT	176	0101110110	HT
093	0	1A3	0110100011	\	083	0010000011	!	1E3	0111100011	FS	1E3	0111100011	FS
094	0	175	0101110101	LF	175	0101110101	LF	175	0101110101	LF	175	0101110101	LF
095	0	1A4	0110100100	[	084	0010000100	{	1E4	0111100100	ESC	1E4	0111100100	ESC
096	0	1F2	0111110010	CR	1F2	0111110010	CR	1F2	0111110010	CR	1F2	0111110010	CR
097	0	1A2	0110100010	]	082	0010000010	}	1E2	0111100010	GS	1E2	0111100010	GS
100	0	080	0010000000	DEL	080	0010000000	DEL	080	0010000000	DEL	080	0010000000	DEL
101	0	174	0101110100	VT	174	0101110100	VT	174	0101110100	VT	174	0101110100	VT
102	0	0D2	0011010010	_	1A0	0110100000	—	1E0	0111100000	US	1E0	0111100000	US
103	0	173	0101110011	FS	173	0101110011	FS	173	0101110011	FS	173	0101110011	FS
104	0	1F5	0111110101	LF	1F5	0111110101	LF	1F5	0111110101	LF	1F5	0111110101	LF
105	0	1BF	0110111111	@	1A3	0110100011	\	1FF	0111111111	NUL	1FF	0111111111	NUL
106	0	1A1	0110100001	^	081	0010000001	~	1E1	0111100001	RS	1E1	0111100001	RS
107	0	1A0	0110100000	—	0^2	0011000010	=	1A0	0110100000	—	0C2	0011000010	=
110	0	172	0101110010	CR	172	0101110010	CR	172	0101110010	CR	172	0101110010	CR
111	0	1F6	0111110110	HT	1F6	0111110110	HT	1F6	0111110110	HT	1F6	0111110110	HT
112	0	0D2	0011010010	-	0C2	0011000010	=	0D2	0011010010	–	0C2	0011000010	=
113	0	171	0101110001	SO	171	0101110001	SO	171	0101110001	SO	171	0101110001	SO
114	0	190	0110010000	o	1A0	0110100000	–	1F0	0111110000	SI	1E0	0111100000	US
115	0	1A4	0110100100	[	1A2	0110100010	]	1A4	0110100100	[	1A2	0110100010	]
116	0	1F7	0111110111	BS	1F7	0111110111	BS	1F7	0111110111	BS	1F7	0111110111	BS
117	0	160	0101100000	US	160	0101100000	US	160	0101100000	US	160	0101100000	US
120	0	170	0101110000	SI	170	0101110000	SI	170	0101110000	SI	170	0101110000	SI
121	0	0C8	0011001000	7	0C8	0011001000	7	0C8	0011001000	7	0C8	0011001000	7
122	0	1F4	0111110100	VT	1F4	0111110100	VT	1F4	0111110100	VT	1F4	0111110100	VT
123	0	16F	0101101111	DLE	16F	0101101111	DLE	16F	0101101111	DLE	16F	0101101111	DLE
124	0	0CB	0011001011	4	0CB	0011001011	4	0CB	0011001011	4	0CB	0011001011	4
125	0	0D3	0011010011	,	0D3	0011010011	,	0D8	0011011000	,	0D3	0011010011	,
126	0	0CE	0011001110	1	0CE	0011001110	1	0CE	0011001110	I	0CE	0011001110	I
127	0	0CF	0011001111	ø	0CF	0011001111	ø	0CF	0011001111	ø	0CF	0011001111	0
130	0	16E	0101101110	DC1	16E	0101101110	DC1	16E	0101101110	DC1	16E	0101101110	DC1
131	0	0C6	0011000110	9	0C6	0011000110	9	0C6	0011000110	9	0C6	0011000110	9
132	0	0C7	0011000111	8	0C7	0011000111	8	0C7	0011000111	8	0C7	0011000111	8
133	0	0CA	0011001010	5	0CA	0011001010	5	0CA	0011001010	5	0CA	0011001010	5
134	0	0C9	0011001001	6	0C9	0011001001	6	0C9	0011001001	6	0C9	0011001001	6
135	0	0CD	0011001101	2	0CD	0011001101	2	0CD	0011001101	2	0CD	0011001101	2
136	0	0CC	0011001100	3	0CC	0011001100	3	0CC	0011001100	3	0CC	0011001100	3
137	0	0D1	0011010001		0D1	0011010001		0D1	0011010001		0D1	0011010001	

OPTIONS ARE Error Flag — Programmed
X15 — Discrete output, normally low
KBINH — Set by high on pin 12 or error flag Function keys not inhibited by KBINH
Error Flag — Reset by releasing error-causing key
Shift Lock — Operational SLI normally low
Alpha Lock — Inhibited ALI normally low, set by OP code XX101
D10 — Discrete output, normally low
Key Type — Normally open

NOTE Bit 9 — Programmed to allow alpha lock implementation using external logic
Bit 8 — Programmed low for "mono mode" keys, for which the output is the same in all modes
Bits 1-7 — "Inverted" ASCII data bits

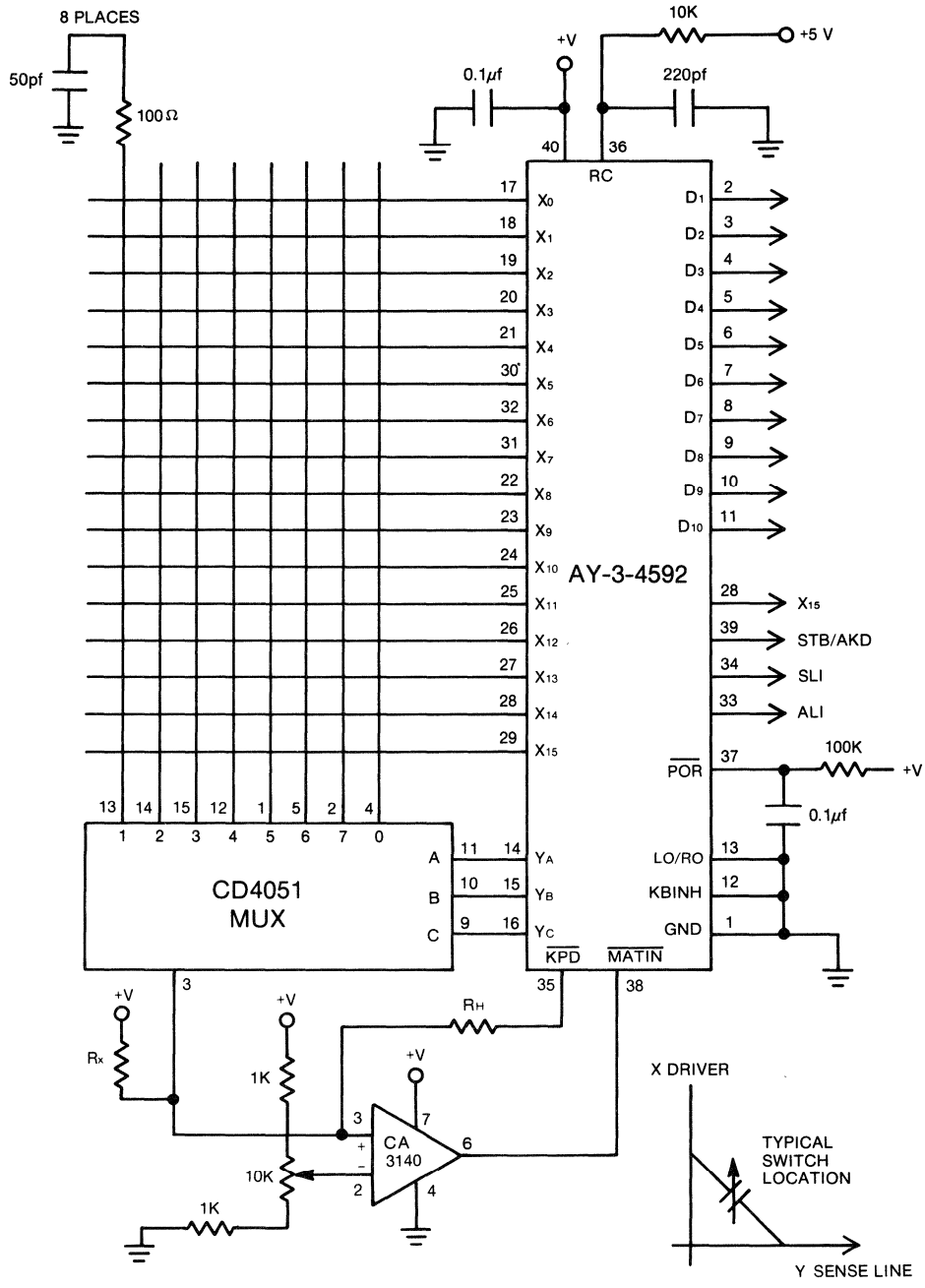


Fig. 1 SAMPLE KEYBOARD DESIGN ROM CODED KEYS

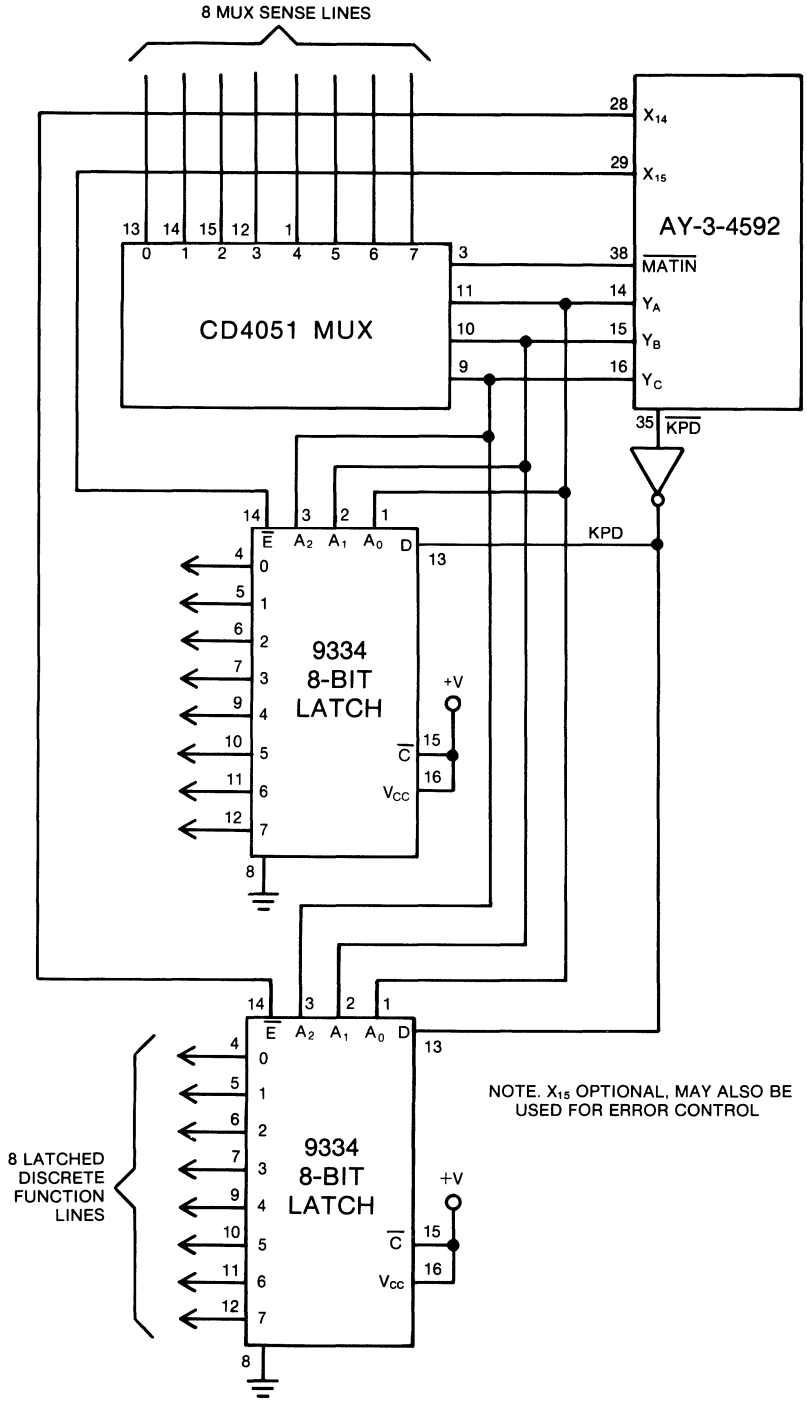


Fig. 2 SAMPLE KEYBOARD DESIGN DISCRETE FUNCTION KEYS

GENERAL INSTRUMENT

Character Generators

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
CHARACTER GENERATOR	2,560 bits organized as 64-5 x 8 characters	RO-3-2513	2-54
	16,384 bits organized as 2048-8 bit words	RO-3-9316CGII	2-59

Character Generator

FEATURES

- 64 x 8 x 5 Organization — Ideal for Systems Requiring a Row Scan 5 x 7 Dot Matrix Character Generator
- Single +5 Volt Supply
- TTL Compatible — All Inputs and Outputs
- Static Operation — No Clocks Required
- 450ns Maximum Access Time
- 175mW Maximum Power
- Three-State Outputs — Under the Control of an Output Inhibit Input to Simplify Memory Expansion
- Standard ASCII (RO-3-2513/CGR-001) or Totally Automated Custom Programing Available
- Zener Protected Inputs
- Glass Passivation Protection

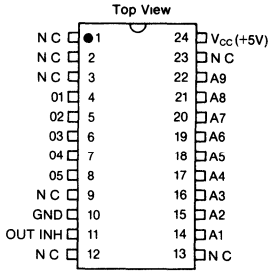
DESCRIPTION

The General Instrument RO-3-2513 is a 2560 bit Read-Only Memory organized as 512 five bit words and is ideally suited for use as a Character Generator. Fabricated in the General Instrument advanced GIANT II N-Channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-2513 can store, for high speed raster scan CRT displays, a full 64 characters in a standard 5 x 7 dot matrix format.

The RO-3-2513 is available pre-programed with ASCII encoded 5 x 7 characters (General Instrument part no. RO-3-2513/CGR-0001) a direct replacement in pin connection, operation, and character font for the Signetics 2513/CM2140. The RO-3-2513 is also available reprogramed with lower case ASCII encoded 5 x 7 characters (General Instrument part no. RO-3-2513/CGR-005), a direct replacement for the Signetics 2513/CM3021

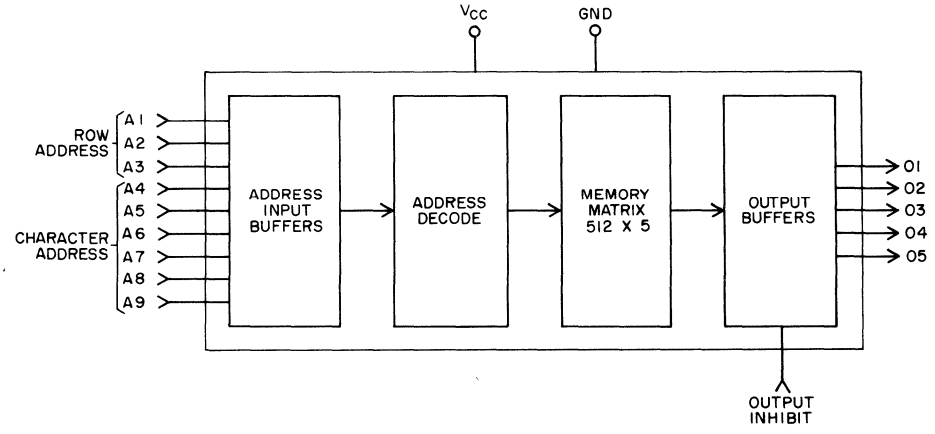
PIN CONFIGURATION

24 LEAD DUAL IN LINE



A separate publication, RO-3-2513 Custom Coding Information, available from General Instrument Sales Offices, describes the punched card and truth table format for custom programing of the RO-3-2513 memory.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) ..... −0.3 to +0.0V
Storage Temperature ..... −65° C to +150° C
Operating Temperature (T_A) ..... 0° C to +70° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

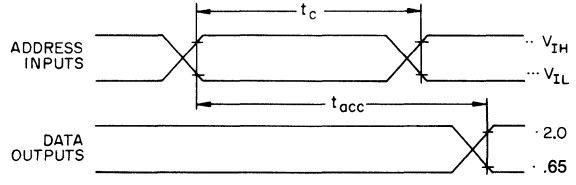
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0° C to +70° C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 50pf

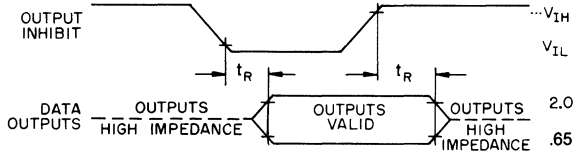
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.5	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC}	—	—	25	35	mA	Outputs open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pf	F = 1MHz
Data Outputs						
Access Time	t_{ACC}	75	250	450	ns	
Inhibit Response Time	t_R	—	150	240	ns	
Capacitance	C_O	—	8	10	pf	F = 1MHz

**Typical values are at +25° C and nominal voltages

TIMING DIAGRAMS



A. ACCESS TIME (ADDRESS TO OUTPUT-OUTPUT INHIBIT AT LOGIC '0')



B. INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

RO-3-2513-001 STANDARD PATTERN CHARACTER FORMAT (Upper Case ASCII)

The RO-3-2513/CGR-001 is a pre-programed version of the RO-3-2513 series with ASCII encoding and the character font shown below. A logic "1" represents an input or output voltage nominally equal to Vcc (+5V) and a logic "0" represents a voltage nominally equal to GND (0V).

An example demonstrating the correspondence of device outputs and addressing sequence to the 5 x 7 dot matrix font is shown below:

CHARACTER ADDRESS

RO-3-2513/CGR-001 Address Bit	A9	A8	A7	A6	A5	A4
ASCII Bit	6	5	4	3	2	1
ASCII upper case "S" Character	0	1	0	0	1	1

ROW ADDRESS

A_3	A_2	A_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS

O_5	O_4	O_3	O_2	O_1
0	0	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	0	0	0	1
0	1	1	1	0

RO-3-2513/CGR-001 CHARACTER ADDRESS A_6 A_5 A_4	A_9 A_8 A_7 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0								
0 0 1								
0 1 0								
0 1 1								
1 0 0								
1 0 1								
1 1 0								
1 1 1								

RO-3-2513-005 STANDARD PATTERN CHARACTER FORMAT (Upper Case ASCII)

The RO-3-2513/CGR-005 is a pre-programed version of the RO-3-2513 series with ASCII encoding and the character font shown below. A logic "1" represents an input or output voltage nominally equal to V_{CC} (+5V) and a logic "0" represents a voltage nominally equal to GND (0V).

An example demonstrating the correspondence of device outputs and addressing sequence to the 5 x 7 dot matrix font is shown below:

CHARACTER ADDRESS

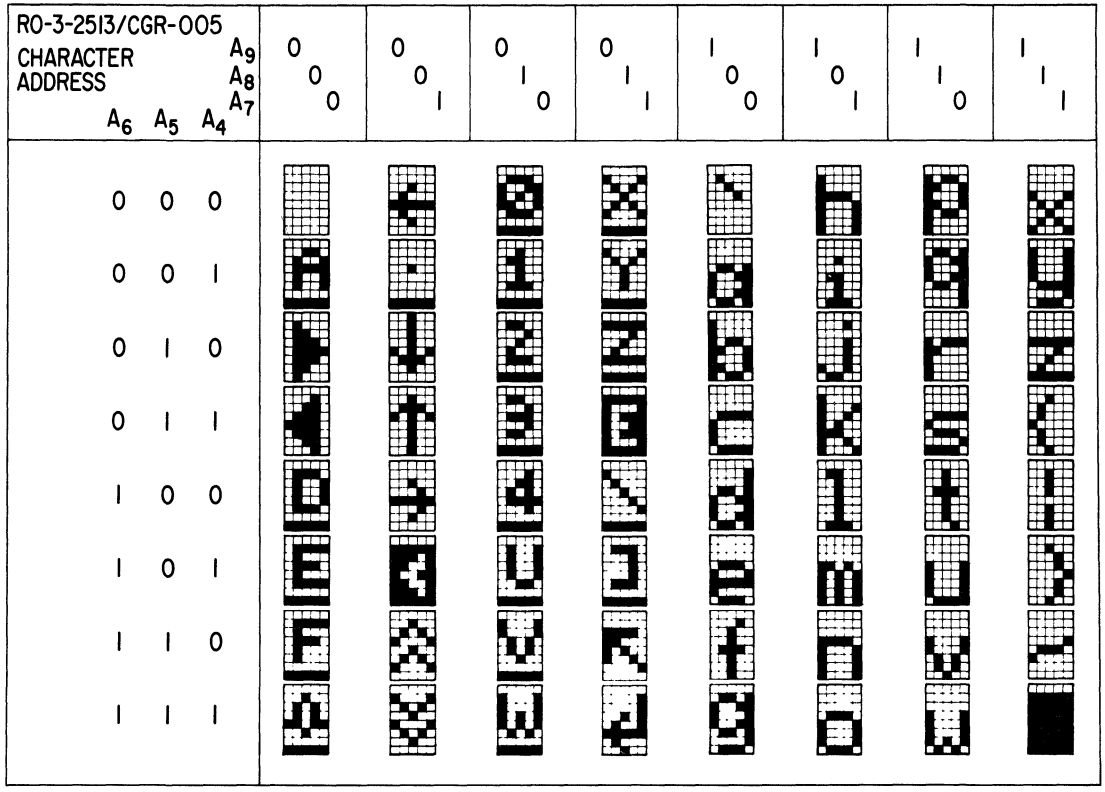
RO-3-2513/CGR-005 Address Bit	A9	A8	A7	A6	A5	A4
ASCII Bit	6	5	4	3	2	1
ASCII lower case 's' Character	1	1	0	0	1	1

ROW ADDRESS

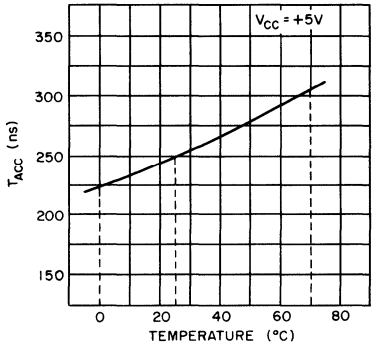
A3	A2	A1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS

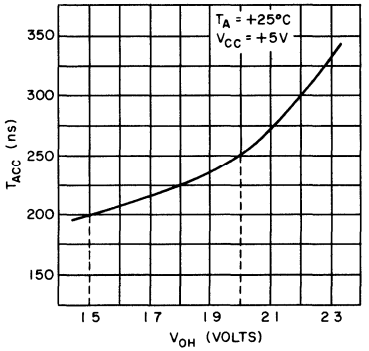
05	04	03	02	01
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	1	1	1	1
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	1	1	1	0



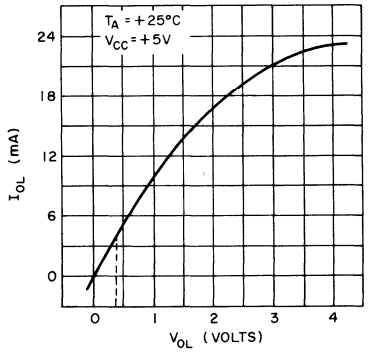
TYPICAL CHARACTERISTIC CURVES



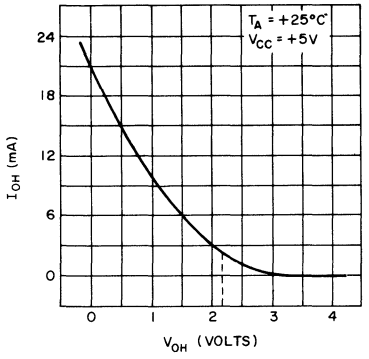
ACCESS TIME vs. TEMPERATURE



ACCESS TIME vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

Character Generator

FEATURES

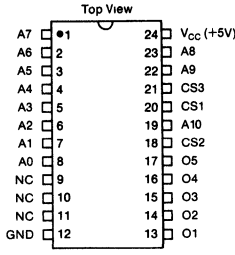
- 128 Character Row Scan Including 96 Standard ASCII Characters
- 5 x 7 Dot Matrix Character Generator
- Single +5 Volt Supply
- TTL Compatible — All Inputs and Outputs
- Static Operation — No Clocks Required
- 450ns Maximum Access Time
- Three-Stage Outputs for Bus Interface
- EPROM 2716 Pin Compatible

DESCRIPTION

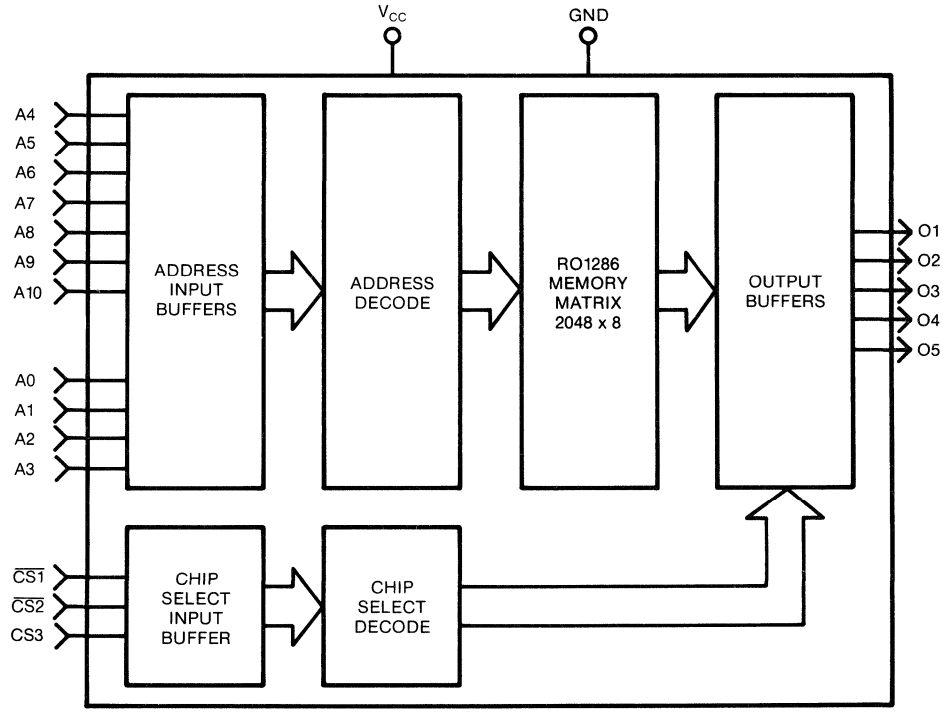
The General Instrument RO1286 is a 16,384 Bit Static Read-Only Memory organized as 2048 8-bit words and is ideally suited for use as a Character Generator. Fabricated in the General Instrument N-Channel Ion Implant process to enable operation from a single +5 Volt power supply, the RO1286 can store for high speed raster scan CRT displays, a full 128 characters in a standard 5 x 7 dot matrix format.

PIN CONFIGURATION

24 PIN DUAL IN LINE



BLOCK DIAGRAM



DESCRIPTION

The chip is selected by applying the proper logic levels to the 3-chip select pins (PIN 20, 18, and 21). A 7-bit binary word must be present at the address inputs, A4-A10 of the character generator, to select a character (one out of the 128 programed characters). The dot matrix of selected characters is generated by cycling line count address input A0-A3 through the line counts necessary to generate the characters. A dot is generated when an output is a "1".

CHIP SELECT

CS1	CS2	CS3
0	0	1

CHARACTER ADDRESS

A10	A9	A8	A7	A6	A5	A4
1	0	0	1	0	0	0

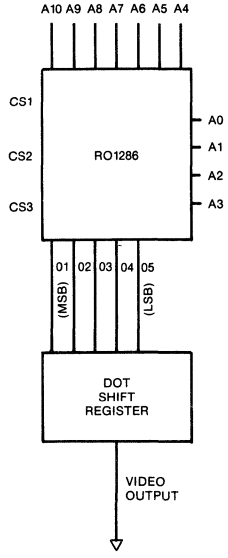
LINE COUNT

A3	A2	A1	A0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0

DOT MATRIX

01	02	03	04	05
1	0	0	0	1
1	0	0	0	1
1	0	0	0	1
1	1	1	1	1
1	0	0	0	1
1	0	0	0	1
1	0	0	0	1
0	0	0	0	0
0	0	0	0	0

Example of Generating the Character 'H':



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and Input Voltages (with Respect to GND) ..... −0.3V to +8.0V
Storage Temperature ..... −65°C to +150°C
Operating Temperature (T_A) ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise noted):

V_{CC} = +5V ±5%
Operating Temperature T_A = 0°C to +70°C
Output Loading: One TTL Load, $C_{L\ TOTAL}$ = 100pf

Data labeled "typical" is presented for design guidance only and is not guaranteed.

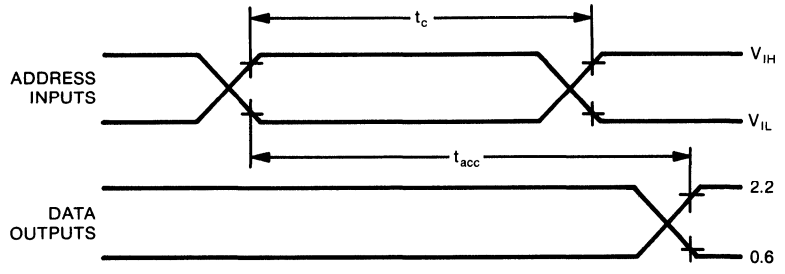
DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, CHIP SELECT Inputs						
Logic "1"	V_{IH}	2	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
RO-3-9316B-CC1	I_{CC}	—	65	115	mA	Outputs Open

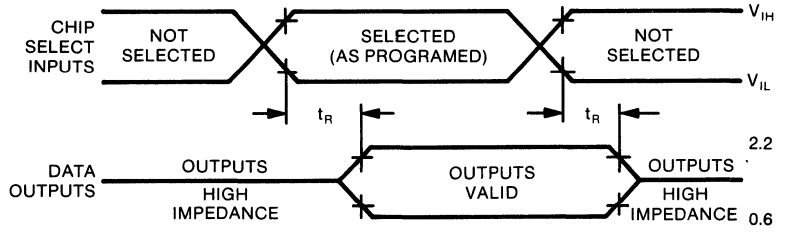
AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address, CHIP SELECT Inputs						
Cycle Time	t_C	400	—	—	ns	
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance						
Input Capacitance	C_I	—	5	8	pf	F = 1MHz
Output Capacitance	C_O	—	8	10	pf	F = 1MHz

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)



CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

RO1286 Character set in Hexadecimal Representation:

Character	Hex No.	Character	Hex No.	Character	Hex No.	Character	Hex No.
—	00	SP	20	@	40	‘	60
A	01	!	21	A	41	a	61
B	02	”	22	B	42	b	62
C	03	#	23	C	43	c	63
D	04	$	24	D	44	d	64
E	05	%	25	E	45	e	65
F	06	&	26	F	46	f	66
G	07	’	27	G	47	g	67
H	08	(	28	H	48	h	68
I	09	)	29	I	49	ı	69
J	0A	*	2A	J	4A	j	6A
K	0B	+	2B	K	4B	k	6B
L	0C	,	2C	L	4C	l	6C
M	0D	-	2D	M	4D	m	6D
N	0E	.	2E	N	4E	n	6E
O	0F	/	2F	O	4F	o	6F
P	10	0	30	P	50	p	70
Q	11	1	31	Q	51	q	71
R	12	2	32	R	52	r	72
S	13	3	33	S	53	s	73
T	14	4	34	T	54	t	74
U	15	5	35	U	55	u	75
V	16	6	36	V	56	v	76
W	17	7	37	W	57	w	77
X	18	8	38	X	58	x	78
Y	19	9	39	Y	59	y	79
Z	1A	:	3A	Z	5A	z	7A
↑	1B	;	3B	[	5B	{	7B
↓	1C	<	3C	\	5C	¦	7C
←	1D	=	3D	]	5D	}	7D
→	1E	>	3E	^	5E	~	7E
£	1F	?	3F	—	5F	■	7F

RO1286 CHARACTER ADDRESS

A7 A6 A5 A4 / A10 A9 A8	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
000	_	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
001	P	Q	R	S	T	U	V	W	X	Y	Z	↑	↓	←	→	£
010		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
011	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
100	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
100	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
110	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
111	p	q	r	s	t	u	v	w	x	y	z	{	!	}	~	■

GENERAL INSTRUMENT

Speech ROMs

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
SERIAL SPEECH ROM	16,384 bits organized 2048 x 8	SPR016	2-64
	32,768 bits organized 4096 x 8	SPR032	2-70
	131,072 bits organized 16K x 8	SPR128	2-73

16,384 Bit Serial Read Only Memory

FEATURES

- 2048 x 8 Bit ROM Organization
- Serial In/Parallel Out Shift Register
- Single Supply Voltage +5V
- Interfaced to SP0256
- Totally Automatic Custom Programing

DESCRIPTION

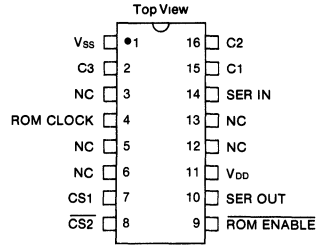
The SPR016 is a serial Read Only Memory with 2048 x 8 bits of ROM. The data is addressed by an internal program counter (PC). The device also contains a serial in/parallel out shift register, which is used to assemble an address to be parallel loaded into the PC.

The device operates with a single supply (nominally +5V) which may be powered down when the system is inactive. When the SPR016 is interfaced to the SP0256 Speech Processor, the ROM enable input is used to avoid bus conflict on the serial out pin during the SPR016 power up.

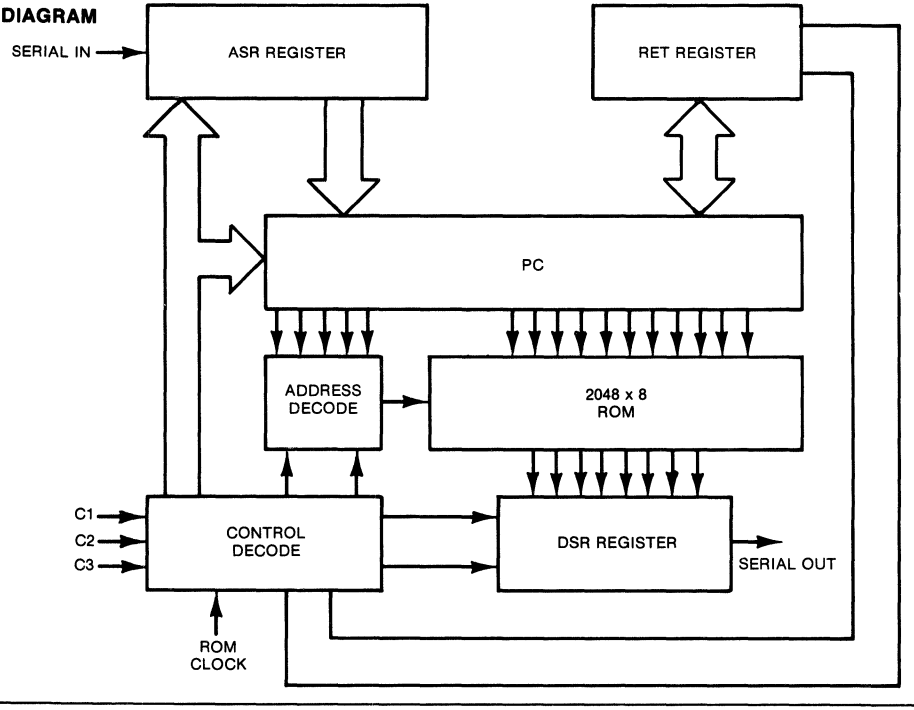
The SPR016 is constructed on a single monolithic chip utilizing the General Instrument low voltage N-Channel Ion Implant technology.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN ASSIGNMENTS (PRELIMINARY)

Pin Number	Name	Function
9	$\overline{\text{ROM ENABLE}}$	Active low chip select used in system to eliminate bus conflict at system start-up. When brought high, $\overline{\text{ROM ENABLE}}$ Tri-States Serial Out.
14	SERIAL IN	Serial Input used to load 16 bit address into device.
10	SERIAL OUT	Output pin used to shift out data byte.
7	CS1	Active high chip select. Will Tri-State Serial output when low.
8	$\overline{\text{CS2}}$	Active low chip select. Will Tri-State Serial output when high.
4	ROM CLOCK	1.56MHz clock input from SP0256 speech processor.
1	V_{SS}	Ground pin.
2 16 15	C3 C2 C1	Control pins decoded to determine device function.
11	V_{DD}	Positive supply pin (+4.6V to +7.0V).

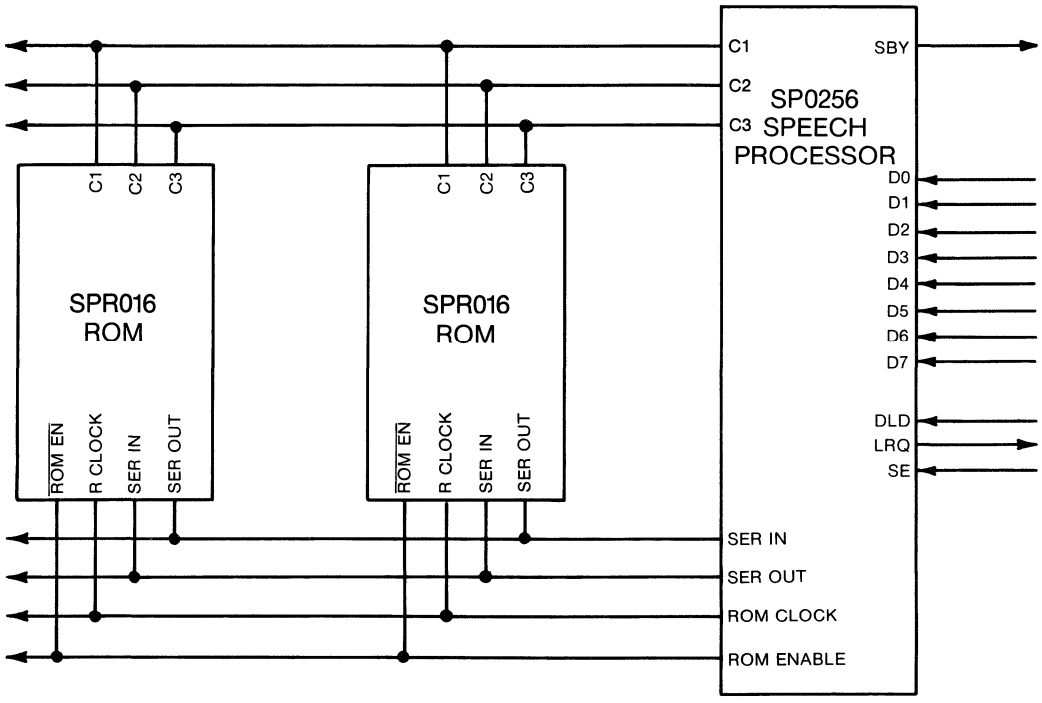


Fig. 1 INTERFACE OF SPR016 ROM TO SP0256 SPEECH PROCESSOR

TABLE 1 SPR016 CONTROL STATES

C1	C2	C3	Name	Function
0	0	0	**NOP**	No action taken
0	0	1	**ASR Load**	Accepts data from the serial input, synchronous to the externally supplied ROM clock. This data is shifted into the ASR holding register in preparation for loading into the PC. Although ASR is 16 bits long, it is not necessary to load all 16 bits of address sequentially in one ASR load.
0	1	0	**PC Load**	Loads the contents of the ASR register into the PC.
0	1	1	**DSR Load**	Loads the 8 bits of data pointed to by the present value of the least significant 11 bits of the PC into the data output shift register (DSR). At the completion of the DSR load the PC is incremented.
1	0	0	**DSR Shift Out**	Shifts out the contents of DSR to the serial out pin, synchronous to the ROM clock.
1	0	1	**RET Register Load**	Loads the return register (RET) with the current value of the PC
1	1	0	**Return**	Loads the PC with the contents of the RET register.
1	1	1	**NOP**	No Action Taken

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} ..... −.3 to +12V
Storage Temperature ..... −25°C to +125°C
Lead Temperature (Soldering) 10 Sec ..... +333°C

*Exceeding these ratings could cause permanent damage to this device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{DD} = +4.6V to +7.0V
Operating Temperature = 0°C to +70°C

Supply Current

I_{DD} = 25mA V_{DD} = 7.0V ROM clock frequency typically 1.56MHz
V_{SS} = 0.0V T_A = 0°C

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Inputs						
$\overline{\text{ROM ENABLE}}$, SERIAL IN, CS1, $\overline{\text{CS2}}$, C1, C2, C3						
ROM Clock						
Logic "0"	V_{IL}	0	—	0.6	V	
Logic "1"	V_{IH}	2.4	—	V_{DD}	V	
Capacitance	C_{IN}	—	—	10	pf	
Leakage	I_{LC}	—	—	10	μA	$V_{PIN} = V_{DD}$ Volts, all others grounded
Outputs						
SERIAL OUT						
Logic "0"	V_{OL}	0	—	0.6	V	I_L = 1.6mA
Logic "1"	V_{OH}	2.5	—	V_{DD}	V	I_L = −50μA
Leakage	I_{LO}	—	—	10	μA	Output Tristated

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
ROM Clock Freq.	F	1.555	1.56	1.565	MHz	48% to 52% Duty Cycle Positive
Output Enable Delay Time from $\overline{\text{RE}}$, CS1, $\overline{\text{CS2}}$	t_{OE}	—	—	120	ns	Independent of ROM Clock
Output Disable Delay Time from CS1, $\overline{\text{RE}}$, $\overline{\text{CS2}}$	t_{OD}	—	—	120	ns	
Serial In Set Up Time	t_{SPIN}	120	—	—	ns	
Control Bus Set Up Time	t_{CIN}	180	—	—	ns	
Serial Output Access Time	t_{ACC}	—	—	360	ns	
Address Select Access Time	t_{AS}	—	—	8T + 120	ns	Note 1
Address Deselect Access Time	t_{AD}	—	—	8T + 120	ns	Note 1

NOTE:
1. T is the cycle time, in nanoseconds of the ROM clock input

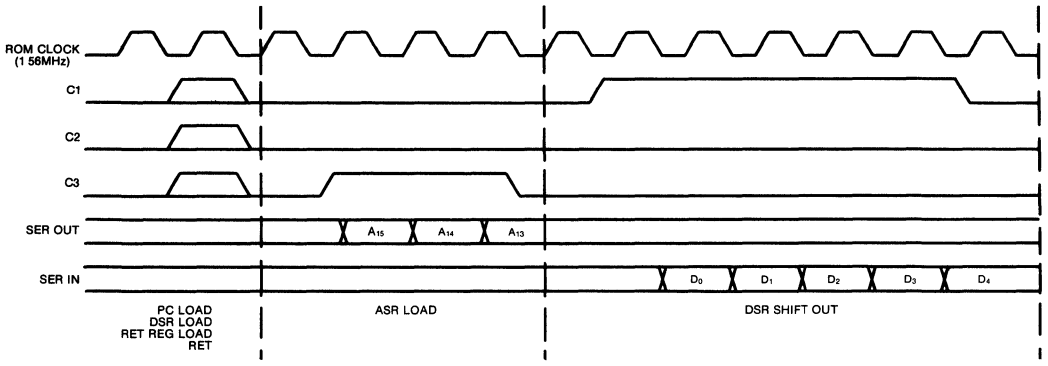
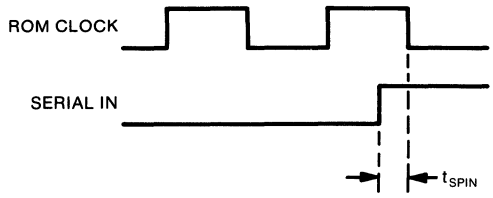
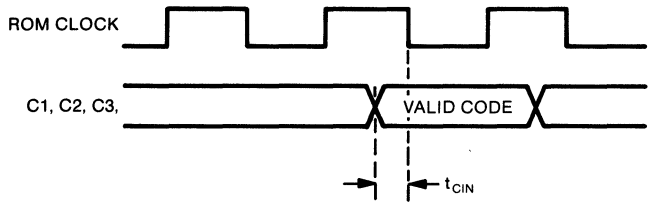


Fig. 2 SPR016 INTERFACE TIMING

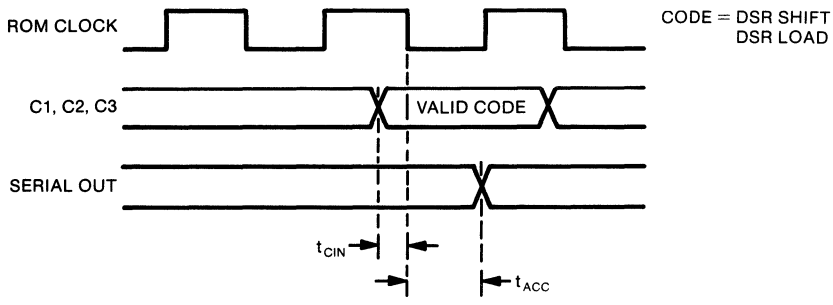
SERIAL IN SETUP TIME



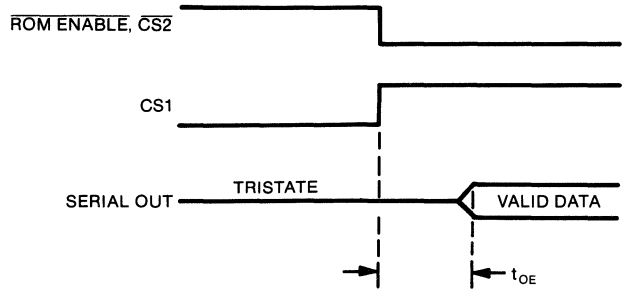
CONTROL BUS SETUP TIME



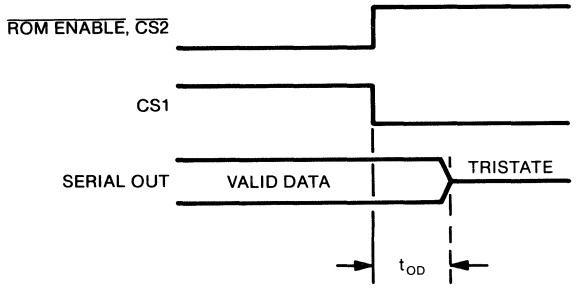
SERIAL OUT ACCESS TIME



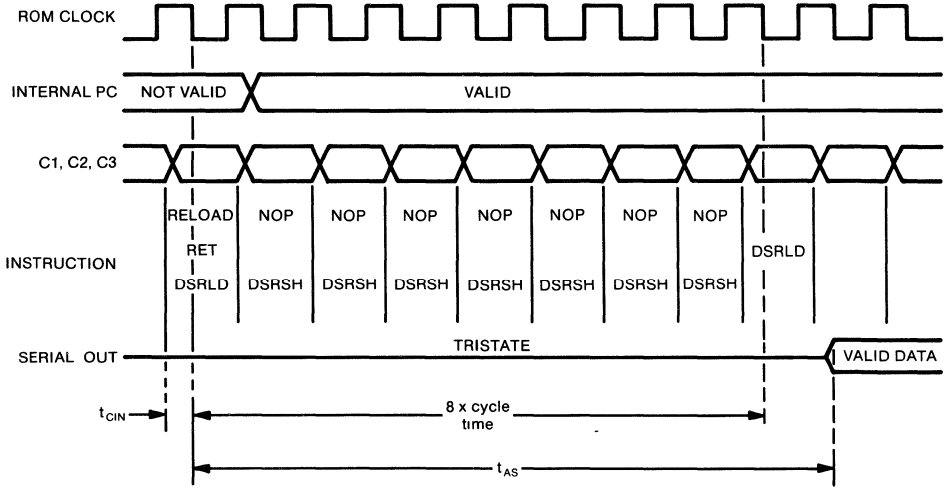
OUTPUT ENABLE RELAY TIME



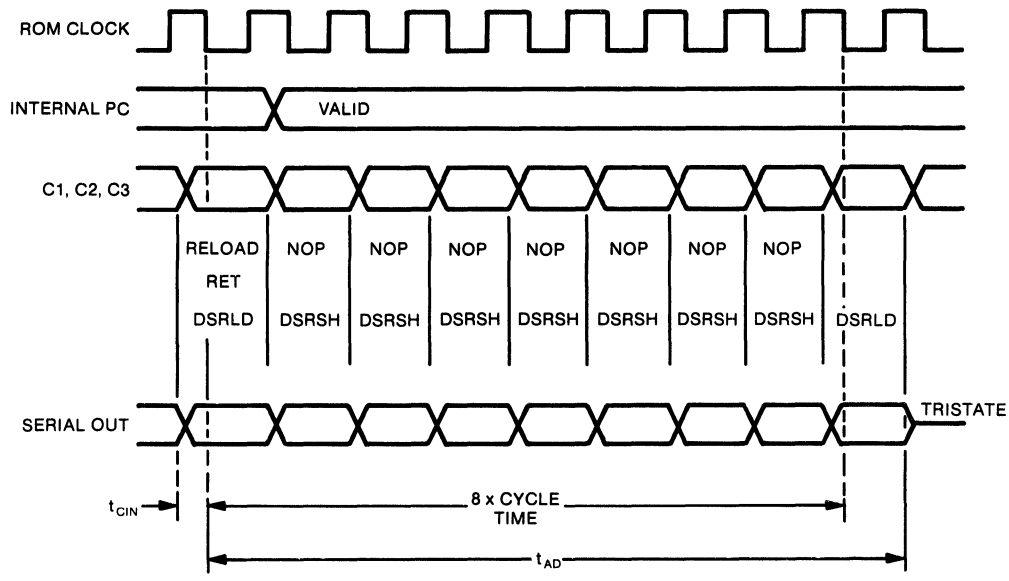
OUTPUT DISABLE RELAY TIME



ADDRESS SELECT ACCESS TIME



ADDRESS DE-SELECT TIME



32,768 Bit Serial Read Only Memory

FEATURES

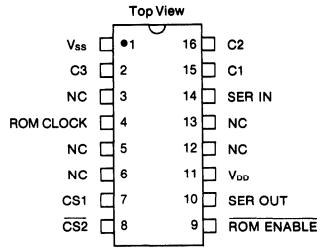
- 4096 x 8 Bit Organization
- Single +5 Volt Supply
- Tri-State Outputs
- Totally Automated Custom Programing
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

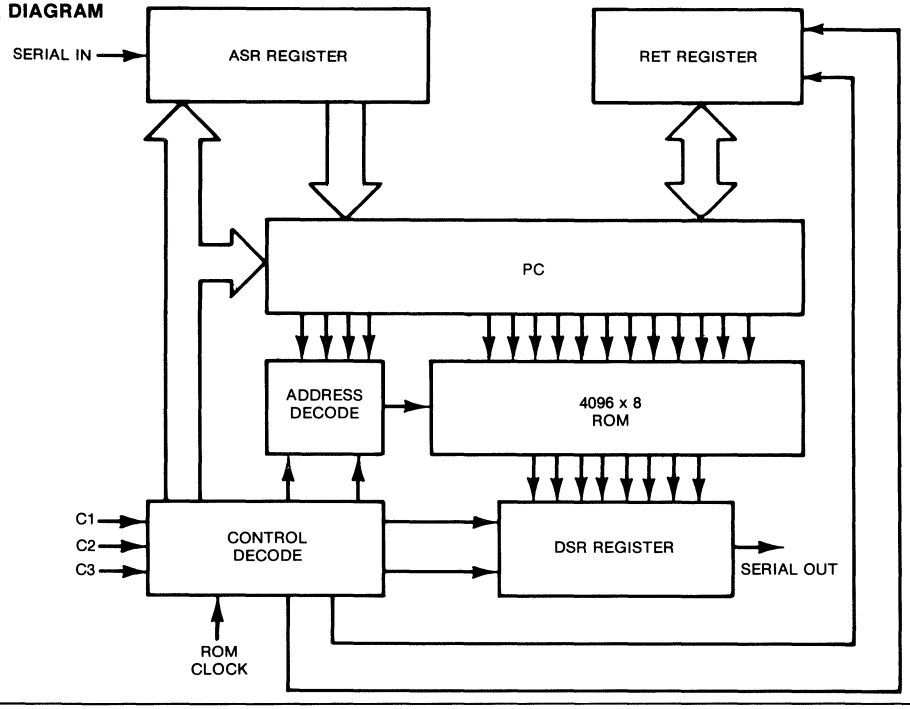
The General Instrument SPR032 is a 32,768 Bit Serial Read Only Memory organized as 4096 eight-bit words and is ideally suited for interfacing with the SP0256 Speech Processor Fabricated in the General Instrument advanced N-Channel Ion-Implant process to enable operation from a single +5 Volt power supply, up to 10 SPR032s can be interfaced to the SP0256 without buffering.

PIN CONFIGURATION

16 PIN DUAL IN LINE



BLOCK DIAGRAM



PIN ASSIGNMENTS (PRELIMINARY)

Pin Number	Name	Function
9	$\overline{\text{ROM ENABLE}}$	Active low chip select used in system to eliminate bus conflict at system start-up. When brought high, $\overline{\text{ROM Enable}}$ Tri-States Serial Out (Pin 3).
14	SERIAL IN	Serial Input used to load 16 bit address into device.
10	SERIAL OUT	Output pin used to shift out data byte.
7	CS1	Active high chip select. Will Tri-State Serial output when low.
8	$\overline{\text{CS2}}$	Active low chip select. Will Tri-State Serial output when high.
4	ROM CLOCK	1.56MHz clock input from SP0256 speech processor.
1	V_{SS}	Ground pin.
2	C3	Control pins decoded to determine device function.
16	C2	
15	C1	
11	V_{DD}	Positive supply pin (+4.6V to +7.0V).

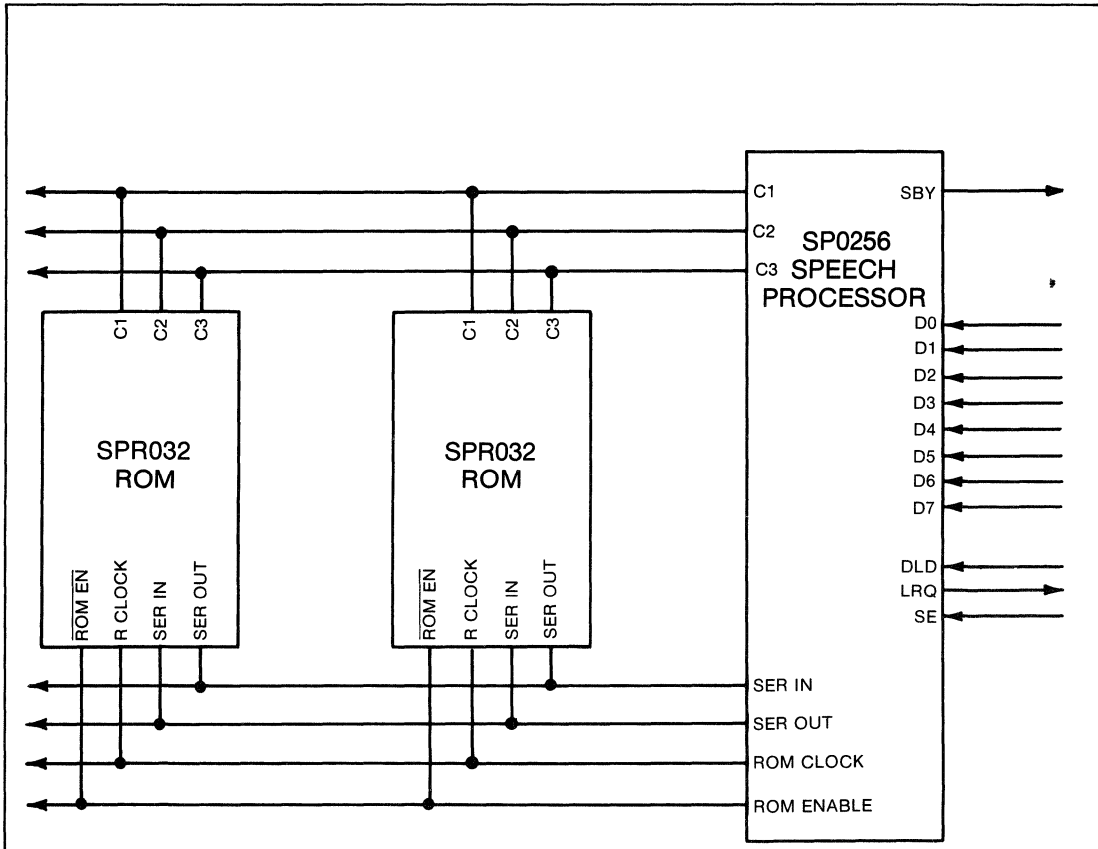


Fig. 1 INTERFACE OF SPR032 ROM TO SP0256 SPEECH PROCESSOR

TABLE 1 SPR032 CONTROL STATES

C1	C2	C3	FUNCTION	
0	0	0	**NOP**	No action taken.
0	0	1	**ASR Load**	Accepts data from the serial input, synchronous to the externally supplied ROM clock. This data is shifted into the ASR holding register in preparation for loading into the PC. Although ASR is 16 bits long, it is not necessary to load all 16 bits of address sequentially in one ASR load.
0	1	0	**PC Load**	Loads the contents of the ASR register into the PC.
0	1	1	**DSR Load**	Loads the 8 bits of data pointed to by the present value of the least significant 11 bits of the PC into the data output shift register (DSR). At the completion of the DSR load the PC is incremented.
1	0	0	**DSR Shift Out**	Shifts out the contents of DSR to the serial out pin, synchronous to the ROM clock.
1	0	1	**RET. Register Load**	Loads the return register (RET) with the current value of the P.C.
1	1	0	**Return**	Loads the PC with the contents of the RET register.
1	1	1	**NOP**	No action taken.

ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{DD} ..... −.3 to +12V
Storage Temperature ..... −25° C to +125° C
Lead Temperature (soldering) 10 Sec ..... +333° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated)

V_{DD} = +4.6V to +7.0V
Operating Temperature = 0° C to +70° C

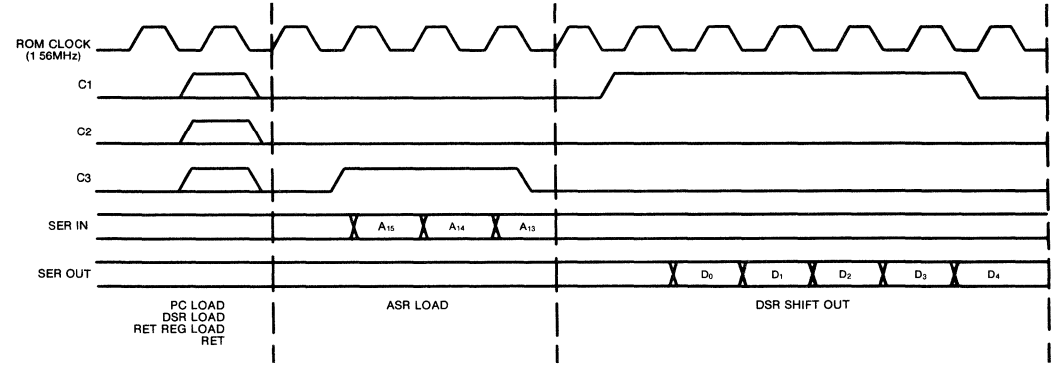
Supply Current

I_{DD} = 25mA V_{DD} = 7.0V V_{SS} = 0.0V ROM clock frequency typically 1.56MHz T_A = 0° C

DC CHARACTERISTICS

Characteristics	Sym	Min	Max	Units	Conditions
Inputs					
$\overline{\text{ROM ENABLE}}$, SERIAL IN, CS1, $\overline{\text{CS2}}$, C1, C2, C3					
ROM Clock					
Logic 0	V_{IL}	0	0.6	V	
Logic 1	V_{IH}	2 4	V_{DD}	V	
Capacitance	C_{IN}	—	10	pf	
Leakage	I_{LC}	—	10	μA	V Pin = V_{DD} Volts, all others grounded
Outputs					
SERIAL OUT					
Logic 0	V_{OL}	0	0.6	V	I_L = 1.6mA
Logic 1	V_{OH}	2.5	V_{DD}	V	I_L = −50μA
Leakage	I_{LO}	—	10	μA	Output Tristated

TIMING DIAGRAM



SPR032 INTERFACE

131,072 Bit Serial Read Only Memory

FEATURES

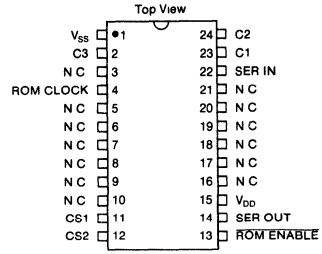
- 16K x 8 Organization
- Single +5 Volt Supply
- Tri-State Serial Output
- Totally Automated Custom Programing
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

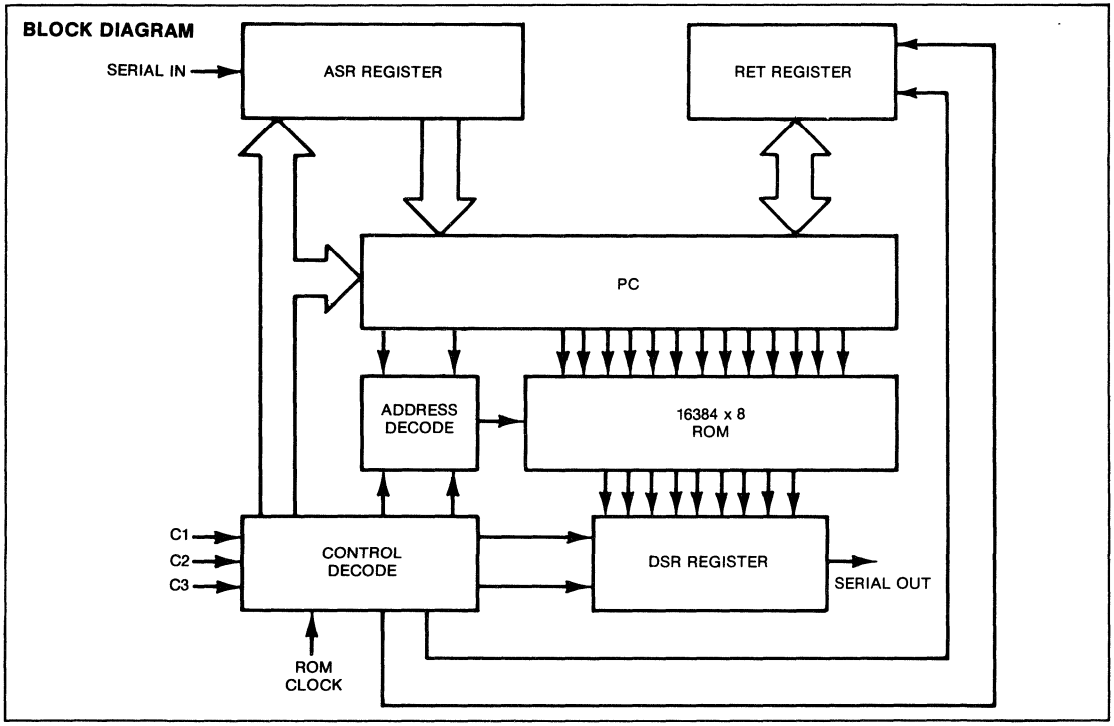
The General Instrument SPR128 is a 131,072 Bit Serial Read Only Memory organized as 16,384 eight-bit words and is ideally suited for interfacing with the SP0256 Speech Processor. Fabricated in the General Instrument advanced N-Channel Ion Implant process to enable operation from a single +5 Volt power supply, up to 4 SPR128s can be interfaced to the SP0256 without buffering.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN ASSIGNMENTS

Pin Number	Name	Function
	$\overline{\text{ROM ENABLE}}$	Active low chip select used in system to eliminate bus conflict at system start-up. When brought high, $\overline{\text{ROM ENABLE}}$ Tri-States Serial Out.
	SERIAL IN	Serial Input used to load 16 bit address into device.
	SERIAL OUT	Output pin used to shift out data byte.
	CS1	Active high chip select. Will Tri-State Serial output when low.
	$\overline{\text{CS2}}$	Active low chip select. Will Tri-State Serial output when high.
	ROM CLOCK	1.56MHz clock input from SP0256 speech processor.
	V_{SS}	Ground pin.
	C3 C2 C1	Control pins decoded to determine device function
	V_{DD}	Positive supply pin (+4.6V to +7.0V)

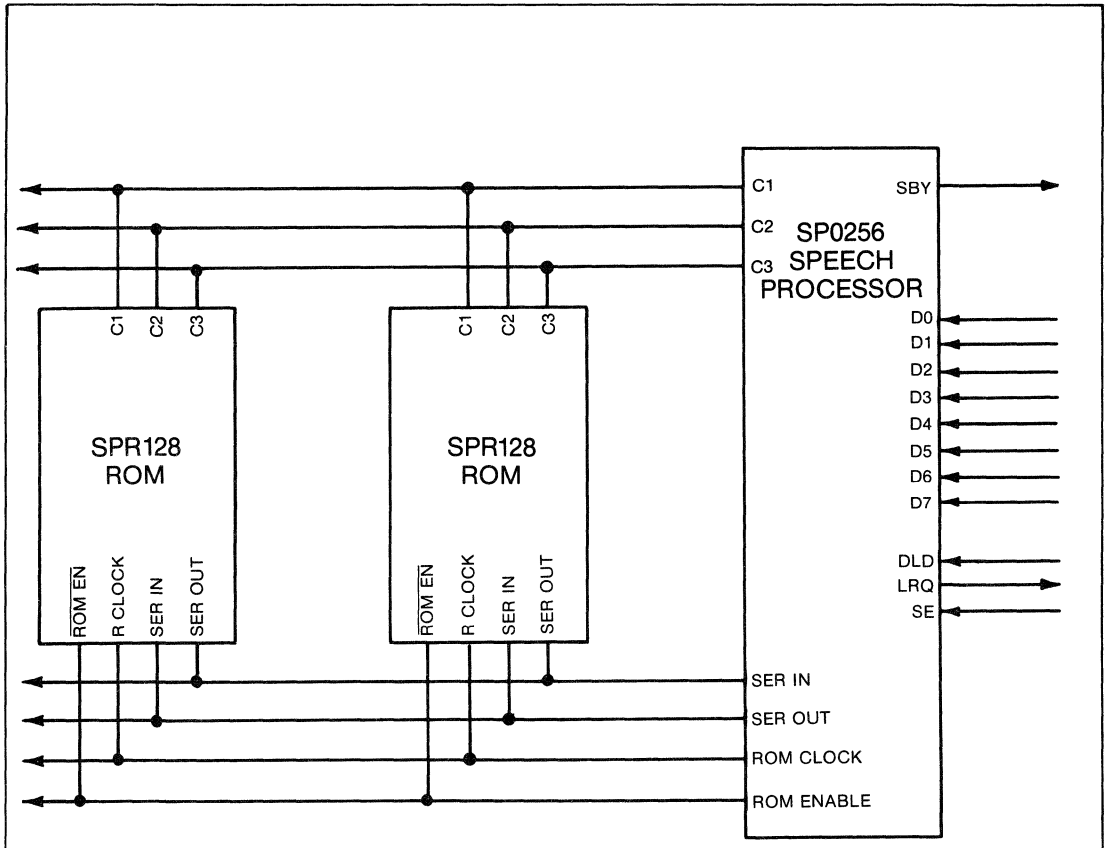


Fig. 1 INTERFACE OF SPR128 ROM TO SP0256 SPEECH PROCESSOR

TABLE 1 SPR128 CONTROL STATES

C1	C2	C3	Function	
0	0	0	**NOP**	No action taken.
0	0	1	**ASR Load**	Accepts data from the serial input, synchronous to the externally supplied ROM clock. This data is shifted into the ASR holding register in preparation for loading into the PC. Although ASR is 16 bits long, it is not necessary to load all 16 bits of address sequentially in one ASR load.
0	1	0	**PC Load**	Loads the contents of the ASR register into the PC.
0	1	1	**DSR Load**	Loads the 8 bits of data pointed to by the present value of the least significant 14 bits of the PC into the data output shift register (DSR). At the completion of the DSR load the PC is incremented.
1	0	0	**DSR Shift-Out**	Shifts out the contents of DSR to the serial out pin, synchronous to the ROM clock.
1	0	1	**RET Register Load**	Loads the return register (RET) with the current value of the PC.
1	1	0	**Return**	Loads the PC with the contents of the RET register.
1	1	1	**NOP**	No action taken

ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{DD} ..... −.3 to +12V
Storage Temperature ..... −25° to +125°C
Lead Temperature (soldering) 10 Sec ..... +333°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated)

V_{DD} = +4.6V to +7.0V
Operating Temperature = 0°C to +70°C

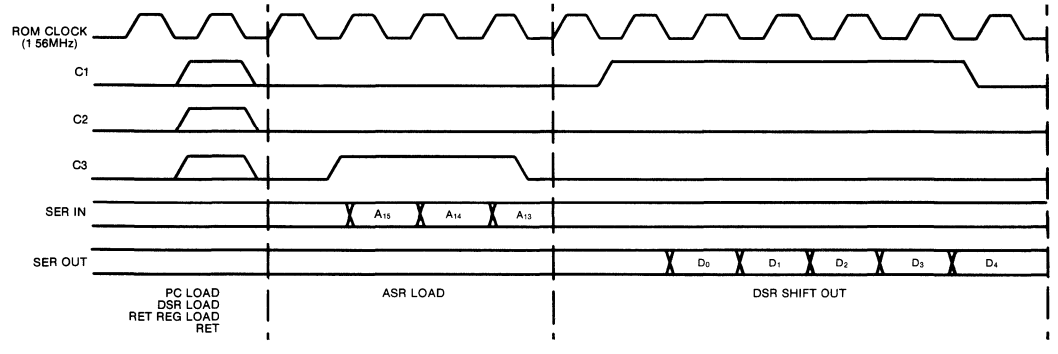
Supply Current

I_{DD} = 25mA V_{DD} = 7.0V ROM clock frequency typically 1 56MHz
V_{SS} = 0.0V T_A = 0°C

DC CHARACTERISTICS

Characteristics	Sym	Min	Max	Units	Conditions
Inputs					
ROM ENABLE, SERIAL IN, CS1, CS2, C1, C2, C3 ROM Clock					
Logic 0	V_{IL}	0	0.6	V	
Logic 1	V_{IH}	2.4	V_{DD}	V	
Capacitance	C_{IN}	—	10	pf	
Leakage	C_{IN}	—	10	μA	V Pin = V_{DD} Volts, all others grounded
Outputs					
SERIAL OUT					
Logic 0	V_{OL}	0	0.6	V	I_L = 1.6mA
Logic 1	V_{OH}	2 5	V_{DD}	V	I_L = −50μA
Leakage	I_{LO}	—	10	μA	Output Tristated

TIMING DIAGRAM



SPR128 INTERFACE

Electrically Alterable Non-Volatile Memory 3

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
		Electrically Alterable Non-Volatile Memory	
82 BIT EAROM	82 bits organized 82 x 1	ER0082	3-5
700 BIT SERIAL EAROM	700 bits organized 50 x 14	ER1451	3-8
1400 BIT SERIAL EAROM	1400 bits organized 100 x 14	ER1400	3-11
512 BIT EAROM	512 bits organized 32 x 16	ER2051	3-14
		ER2051IR	3-14
		ER2051HR	3-14
512 BIT EAROM	512 bits organized 64 x 8	ER2055	3-17
		ER2055IR	3-17
		ER2055HR	3-17
1K N-CHANNEL EEPROM	1K bits organized 128 x 8	ER5901	3-20
		ER5901IR	3-20
		ER5901HR	3-20
4096 BIT EAROM	4096 bits organized 1024 x 4	ER3400	3-22
		ER3400I/IR	3-22
		ER3400HR	3-22
8192 BIT EAROM	8192 bits organized 2048 x 4	ER2810IR	3-28
		ER2810HR	3-28
16K N-CHANNEL EEPROM	16K bits organized 2048 x 8	ER5716	3-32
		ER5716IR	3-32
		ER5716HR	3-32
WORD ALTERABLE 16K BIT EEPROM	Electrically word alterable 16K bits organized 2048 x 8, 5V operation in read mode.	ER5816	3-36
		ER5816IR	3-36
		ER5816HR	3-36
WORD ALTERABLE 16K BIT EEPROM	Electrically word alterable 16K bits organized 2048 x 8, 5V operation in all modes.	ER5916	3-41
		ER5916IR	3-41
		ER5916HR	3-41
		Non-Volatile Static RAM	
4K N-CHANNEL NON-VOLATILE STATIC RAM	4K bits organized 512 x 8	ER5304	3-48

GENERAL INSTRUMENT

Electrically Alterable Non-Volatile Memory

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
82 BIT EAROM	82 bits organized 82 x 1	ER0082	3-5
700 BIT SERIAL EAROM	700 bits organized 50 x 14	ER1451	3-8
1400 BIT SERIAL EAROM	1400 bits organized 100 x 14	ER1400	3-11
512 BIT EAROM	512 bits organized 32 x 16	ER2051	3-14
		ER2051IR	3-14
		ER2051HR	3-14
512 BIT EAROM	512 bits organized 64 x 8	ER2055	3-17
		ER2055IR	3-17
		ER2055HR	3-17
1K N-CHANNEL EEPROM	1K bits organized 128 x 8	ER5901	3-20
		ER5901IR	3-20
		ER5901HR	3-20
4096 BIT EAROM	4096 bits organized 1024 x 4	ER3400	3-22
		ER3400I/IR	3-22
		ER3400HR	3-22
8192 BIT EAROM	8192 bits organized 2048 x 4	ER2810IR	3-28
		ER2810HR	3-28
16K N-CHANNEL EEPROM	16K bits organized 2048 x 8	ER5716	3-32
		ER5716IR	3-32
		ER5716HR	3-32
WORD ALTERABLE 16K BIT EEPROM	Electrically word alterable 16K bits organized 2048 x 8, 5V operation in read mode.	ER5816	3-36
		ER5816IR	3-36
		ER5816HR	3-36
WORD ALTERABLE 16K BIT EEPROM	Electrically word alterable 16K bits organized 2048 x 8, 5V operation in all modes.	ER5916	3-41
		ER5916IR	3-41
		ER5916HR	3-41

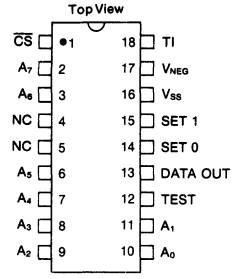
82 Bit Electrically Alterable Read Only Memory

FEATURES

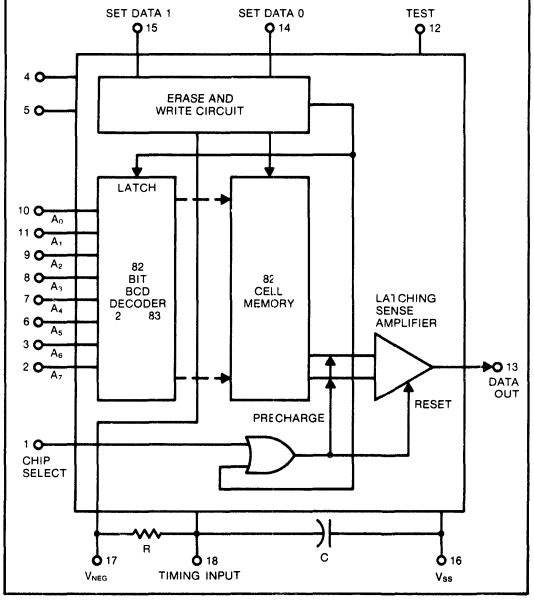
- 82 x 1 bit organization
- Addressing by two 4-bit BCD digits
- +5, −30V power supplies
- Set inputs have debounce circuits
- Bit erasable
- 100 μsec Read Access Time
- Minimum Data Retention, 7 years unpowered, 2 years powered
- P-Channel output transistor, open drain, pull down resistor
- Control, Address and Data Inputs TTL or CMOS compatible
- Ideally suited for T V. receiver channel selection

PIN CONFIGURATION

18 LEAD DUAL IN-LINE



BLOCK DIAGRAM



DESCRIPTION

The ER0082 is a 82 x 1 bit electrically alterable read only memory. This device can be used as part of a television receiver tuner control system. The memory is programmed by the user to maintain a record of channels the user wishes to be tuned, and is non-volatile in that the information stored within is not affected by the condition of or the sequencing of power supplied to the chip.

OPERATION

Memory Address

The address is provided by two positive logic binary coded decimal (BCD) digits, LSD (A_0-A_3) and MSD (A_4-A_7) (least and most significant digits), i e. 8 bits which supply the address of a bit in the memory. There is an address in memory associated with each of the BCD numbers 2 through 83. Addresses outside the range of 2 to 83 at the LSD and MSD inputs do not cause any modification of the stored bits or change in the output data

Example. Address 83 = 10000011 (A_7 . A_0)

Address 2 = 00000010 (A_7 ..A_0)

Address changes must occur only during $\overline{CS}$ high and must be stable at least 20μs before $\overline{CS}$ goes low.

Memory Read

The negative transition of $\overline{CS}$ (from a "1" level to a "0" level) initiates a memory read cycle, except when the transition occurs during a memory alteration cycle, in which case the transition is ignored A read cycle will cause the DATA OUT pin to indicate the state of the memory bit read The DATA OUT pin will retain the state until either $\overline{CS}$ goes to "1" or a memory alteration cycle is initiated. DATA OUT will show the contents of the address 100μs after $\overline{CS}$ starts falling When $\overline{CS}$ is high the DATA OUT pin is low. The DATA OUT pin is internally pulled up to the positive supply, V_{SS} and for a "0" output the DATA OUT pin floats with an external pull-down (10KΩ) to ground.

Memory Alteration

A memory alteration cycle is initiated only when the SET DATA "0" or the SET DATA "1" input, but not both, has been continuously at "0" for the specified debounce time. This allows an input to be entered via a contact closure to ground using switches. These inputs are connected to V_{SS} via internal pull-ups During the alteration cycle the address is held latched within the LSI. Changes in the address and SET DATA inputs are ignored, and the DATA OUT pin is held at "0" Only one memory bit may be erased or written during any single memory alteration cycle The alteration cycle, once initiated, must go to completion. Upon completion of an alteration cycle or the fall of $\overline{CS}$ whichever occurs last, the memory bit corresponding to the current input address will be read and output on the DATA OUT terminal. A memory read of a bit altered due to SET DATA "0" input will cause the DATA OUT pin to be "0" Similarly, a read of a bit altered due to a SET DATA "1" input will cause the DATA OUT pin to be "1". The SET DATA inputs have internal circuits to provide delays for interfacing to mechanical switches or relays. Each successful debounce of a SET DATA input will initiate only one memory alteration cycle. Another alteration cycle will not occur until both

SET DATA inputs have remained continuously at a "1" level for the specified release time and only one of the SET DATA inputs has again been successfully debounced. After an alteration cycle is complete, a read cycle may not be initiated by CS until 3 cycles of the clock on the "Timing" input pin have occurred (about 12.5ms for a nominal 200Hz frequency).

Timing

This is an input provided for external components used for a timing reference. A resistor (680K) and a capacitor (.01μF) may be connected to this input to provide a 200Hz nominal clock frequency A lower capacitor or resistor value will provide a higher frequency The timer will run only during a read cycle, alteration cycles, or while timing a debounce or release. Increasing the clock frequency will shorten these times. The frequency can vary from 50Hz min to 500Hz max. and may be measured on the timing pin

PIN FUNCTIONS

NAME	FUNCTIONS
A_0-A_7	Address bus used to select 1 of 82 addresses
$\overline{CS}$	Chip select. An active low signal which enables or disables the data out pin.
Data Out	DATA OUT is a single bit indicating the state of the addressed memory cell.
Set Data 0 Set Data 1	These are inputs by which the user can modify the memory contents.
TI	Provides a timing reference for internal timing cycles
TEST	A TEST pin which provides a connection to V_m, an internal voltage used for evaluating chip memory performance In normal operation this pin should be left unconnected.
V_{SS}	Substrate Supply. Nominally +5V.
V_{NEG}	Power supply input Nominally −30V

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All input and outputs (except V_{NEG}) with respect to V_{SS} . . −20V to +0.3V
V_{NEG} with respect to V_{SS} . . . . . −40V
Storage temperature (No Data Retention) . . . . . −65° C to +150° C
Storage temperature (with Data Retention)
Operating . . . . . 0° C to +70° C
Unpowered . . . . . −40° C to +85° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

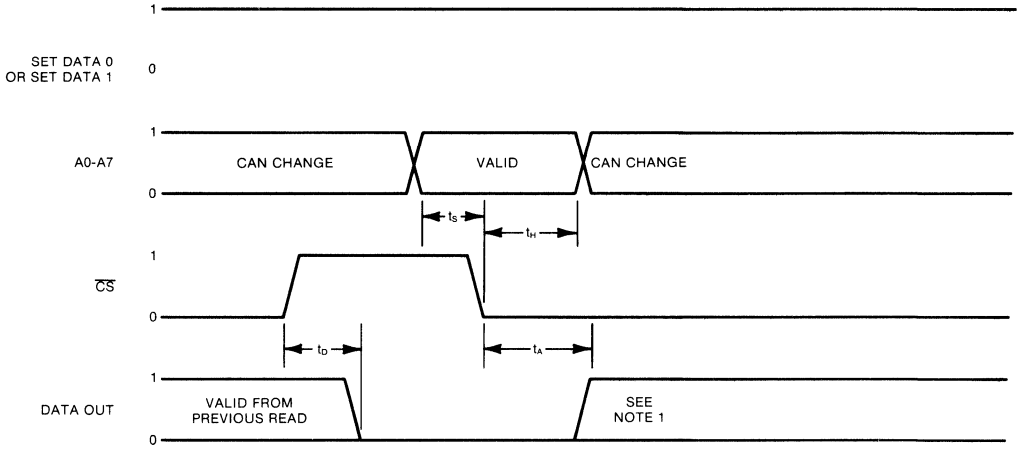
Standard Conditions (unless otherwise noted)

V_{SS} = +4.5V to +8 0V
$V_{SS} - V_{NEG}$ = −32V to −38V
Operating Temperature T_A = 0° C to 70° C

Characteristic	Sym	Min	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic "1"	V_{IH}	V_{SS} −2 0	V_{SS} +.3	V	
Input Logic "0"	V_{IL}	V_{SS} −10	V_{SS} −4.1	V	
Input Leakage	I_L	—	10	μA	
Output Logic "1"	V_{OH}	—	V_{SS} −.5	V	@ 0.5mA
Power Supply	I_{SS}	4	20	mA	
Power Dissipation	P_{SS}	130	700	mW	
AC CHARACTERISTICS					
Read Cycle Time	—	130	—	μs	
Read Access Time	t_A	—	100	μs	from fall of $\overline{CS}$
Memory Alteration Time	—	200	—	ms	
Time between Memory Alteration Cycles	t_C	12.5	—	ms	
Debounce Time for Changing Memory	t_B	12.5	37.5	ms	
Address Setup Time	t_S	20	—	μs	
Address Hold Time	t_H	100	—	μs	
Reset Time	t_D	2	30	μs	from rise of $\overline{CS}$
Input Rise & Fall Times	—	.03	30	ms	on all inputs
EAROM CHARACTERISTICS					
Data Retention, Power Off (Storage)	—	7	—	Years	−40° C to +85° C
Data Retention, Power On	—	2	—	Years	0° C to +70° C
Read Cycles Per Cell	—	10^7	—	—	no loss of data
Erase/Write Cycles per Cell	—	10^3	—	cycles	10 year retention
Erase/Write Cycles per Cell	—	10^4	—	cycles	1 year retention

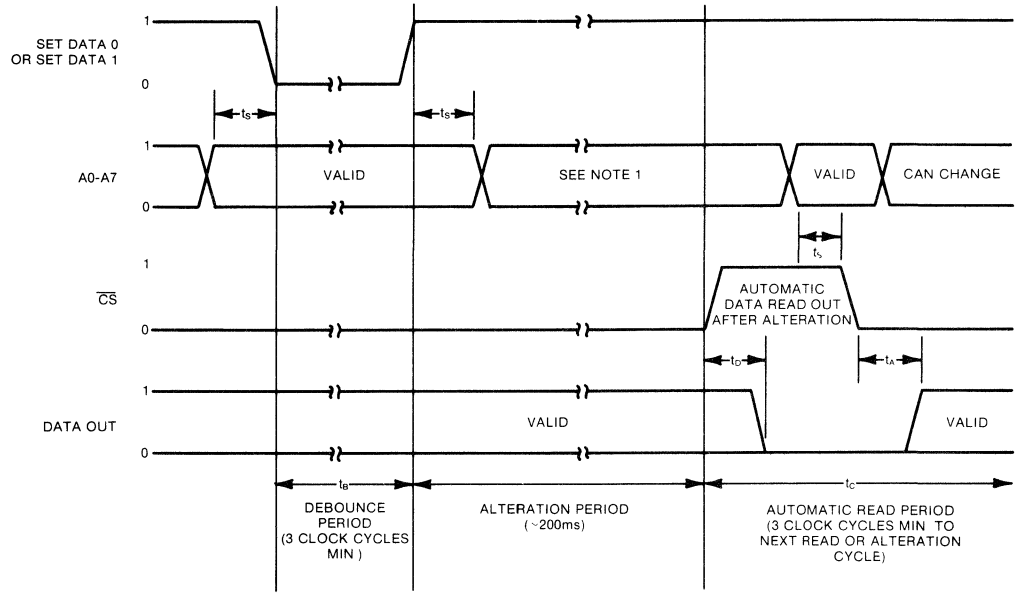
TIMING DIAGRAMS

READ OPERATION



NOTE 1 Data will be valid until the next positive $\overline{CS}$ transition or until initiation of an alteration cycle

DATA ALTERATION



NOTE 1 Address may change here, but should not change if verification of correct alteration is required

700 Bit Serial Electrically Alterable Read Only Memory

FEATURES

- 50 word x 14 bit organization
- Addressing by two consecutive one-of-ten codes
- Word alterable
- 10 year data storage
- TTL compatible signal levels
- Write/erase time 10ms

DESCRIPTION

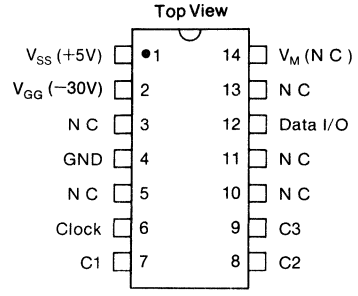
The ER1451 is a serial input/output 700 bit electrically erasable and reprogrammable ROM, organized as 50 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus. Its operation is similar to the ER1400 in all respects, except that it has only half the memory capacity The address, in the form of two consecutive one-of-ten codes, is shifted in with the first ten bits indicating the MSD Address 49 is the highest valid address For this reason during the first five clock cycles of an ACCEPT ADDRESS function the data input is ignored

Mode selection is by a 3 bit code applied to C1, C2 and C3

Before writing, a selected location must be preconditioned by an Erase operation. Data is then stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 700 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

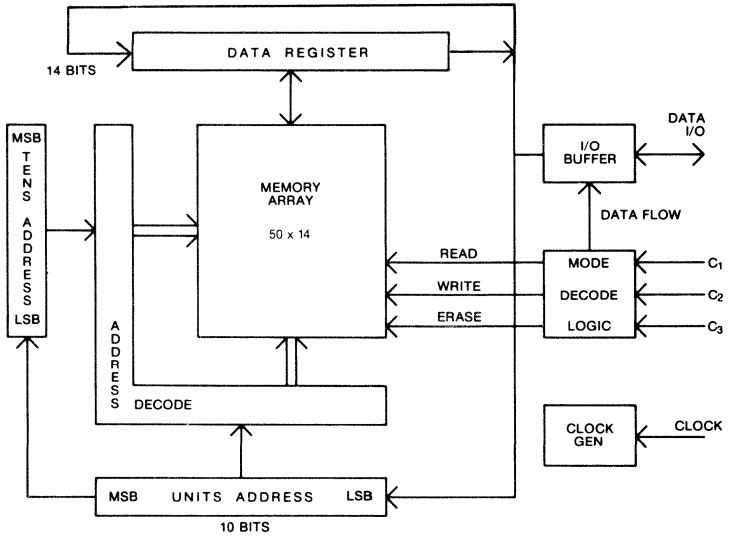
PIN CONFIGURATION

14 LEAD DUAL IN LINE



N.C. = No external connection for normal usage

BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively When outputting data it has TTL drive capability, while in all other modes it is left floating.
V_M	Used for testing purposes only Must be left unconnected for normal operation
V_{SS}	Chip substrate Normally connected to +5V
V_{GG}	DC supply Normally connected to −30 Volt supply
Clock	Timing reference Required for all operations May be left at logic one when device is in standby
C1, C2, C3	Mode control pins Their operation is as follows

C1	C2	C3	Function
1	1	1	Standby—The output buffer is left floating If the clock is maintained, the contents of the Address and Data Registers will remain unchanged
1	0	0	Accept Address—Data presented at the I/O pin is shifted into the Address Register with each clock pulse Addressing is by two consecutive one-of-ten codes
0	1	1	Read—The address word is read from memory into the data register.
0	1	0	Shift Data Out—The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse
1	0	1	Erase—The word stored at the addressed location is erased to all zeroes.
0	0	0	Accept Data—The data register accepts serial data presented at the I/O pin The Address Register remains unchanged
0	0	1	Write—The word contained in the Data Register is written into the location designated by the Address Register
1	1	0	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (except V_{GG}) with respect to V_{SS} . . −20V to +0 3V
V_{GG} with respect to V_{SS} . . . . . −40V
Storage temperature (No Data Retention) . . . . . −65° C to +150° C
Storage temperature (with Data Retention)
Operating . . . . . −25° C to +75° C
Unpowered . . . . . −65° C to +80° C

*Exceeding these ratings could cause permanent damage to the device This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

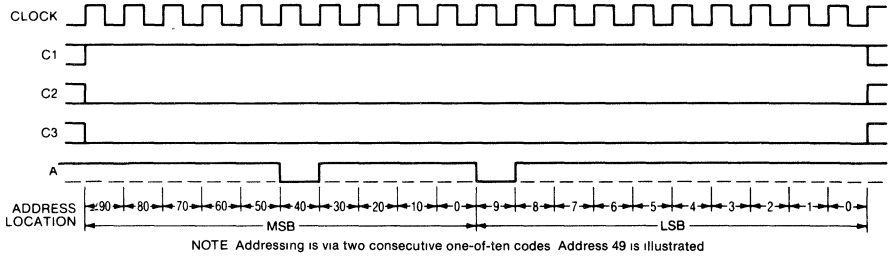
V_{SS} = +5 Volts ± 5% GND = 0 Volts
V_{GG} = −30 Volts ± 5%
Operating Temperature T_A = 0° C to +70° C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input Logic "0"	V_{IL}	V_{SS}−15 0	—	+0 8	Volts	
Input Logic "1"	V_{IH}	V_{SS}−1.5	—	V_{SS}+0 3	Volts	
Input Leakage	I_L	—	—	10	μA	V_{IN} = −10V
Output Logic "0"	V_{OL}	—	—	+0 4	Volts	I_{OL} = 3 2mA
Output Logic "1"	V_{OH}	V_{SS}−1.5	—	V_{SS}	Volts	I_{OH} = 3.2mA
Power Consumption	P_{GG}	—	—	300	mW	
Power Supply Current	I_{GG}	—	—	8 0	mA	
	I_{SS}	—	—	8.0	mA	
AC CHARACTERISTICS						
Clock Frequency	fϕ	10 0	14 0	17 0	kHz	
Clock Duty Cycle	Dϕ	35	50	65	%	
Write Time	tw	10.0	15 0	24 0	ms	
Erase Time	te	10 0	15 0	24 0	ms	
Rise, Fall Time	tr, tf	—	—	1.0	μs	
Control, Data Set Up Time	t_{CS}	1	—	—	μs	
Control, Data Hold Time	t_{CH}	0	—	—	μs	
Propagation Delay	t_{PW}	—	—	20 0	μs	Load: 2 TTL gates + 100pf
Non-Volatile Data Storage	T_S	10	—	—	Years	See Note 1.
Number of Erase/Write Cycles	N_W	—	—	10^4	—	Per word. See Note 2.
Number of Read Accesses Between Writes	N_{RA}	10^9	—	—	—	Per word

**Typical values are at +25° C and nominal voltages

NOTES 1 T_S is for powered or unpowered storage
2 N_W (=10^4) is a maximum for data retention times greater than 10 years. Beyond 10^4 reprogramming cycles, there is a gradual, logarithmic reduction in retention time with 1 year being a typical value after 10^5 cycles.

TIMING DIAGRAMS



NOTE Addressing is via two consecutive one-of-ten codes Address 49 is illustrated

Fig.1 ACCEPT ADDRESS

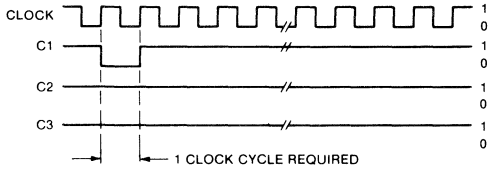
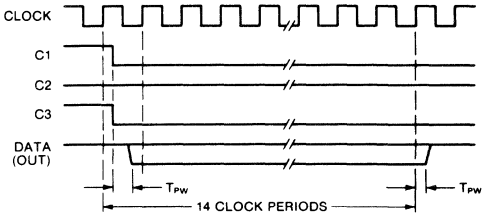


Fig.2 READ



T_{PW} measured initially from control line transition to data out then measured from the positive clock edges to data changes Timing measurements made at V_{SS} −2 and 0 8 Volt points

Fig.3 SHIFT DATA OUT

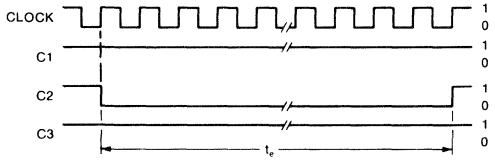


Fig.4 ERASE

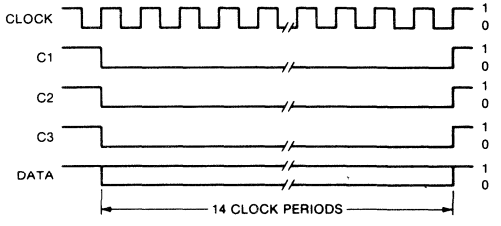


Fig.5 ACCEPT DATA

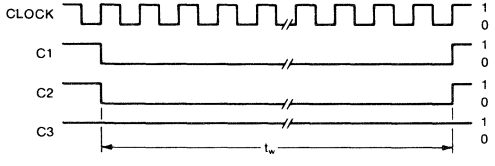


Fig.6 WRITE

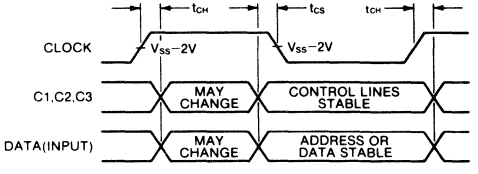


Fig.7 INPUT TIMING

1400 Bit Serial Electrically Alterable Read Only Memory

FEATURES

- 100 word x 14 bit organization
- Addressing by two consecutive one-of-ten codes
- Single −35 Volt supply
- Word alterable
- 10 year data storage
- MOS compatible signal levels
- Write/erase time. 10ms

DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

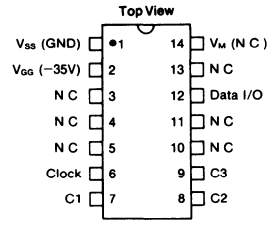
Mode selection is by a 3 bit code applied to C1, C2 and C3.

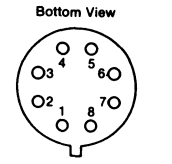
Before writing, a selected location must be preconditioned by an Erase operation Data is then stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATIONS

Standard package
14 LEAD DUAL IN LINE

Special Order Package
8 LEAD TO-8 (ER1400T)

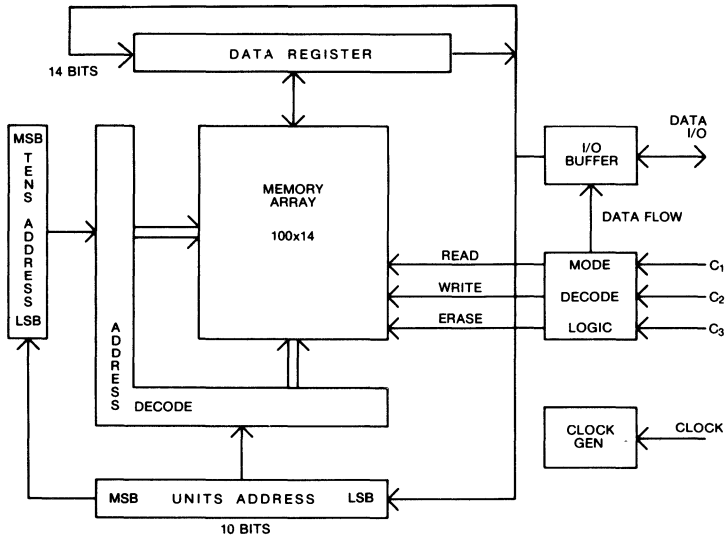




1 Data I/O
2 VM (N C)
3 VSS (GND)
4 VGG (−35V)
5 Clock
6 C1
7 C2
8 C3

N C = No external connection for normal usage

BLOCK DIAGRAM



ELEC. ALTERABLE NON-VOLATILE MEMORY

PIN FUNCTIONS

Name	Function
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. When outputting data it has MOS drive capability, while in all other modes it is left floating.
V_M	Used for testing purposes only. Must be left unconnected for normal operation.
V_{SS}	Chip substrate. Normally connected to ground.
V_{GG}	DC supply. Normally connected to V_{SS} −35 Volt supply.
Clock	Timing reference. Required for all operations. May be left at logic zero when device is in standby.
C1,C2,C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby—the output buffer is left floating. If the clock is maintained, the contents of the Address and Data Registers will remain unchanged.
0	1	1	Accept Address—Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.
1	0	0	Read—The address word is read from memory into the data register.
1	0	1	Shift Data Out—The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase—The word stored at the addressed location is erased to all ones.
1	1	1	Accept Data—The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
1	1	0	Write—The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (except V_{GG}) with respect to V_{SS} . . −20V to +0.3V
V_{GG} with respect to V_{SS} . . . . . −40V
Storage temperature (No Data Retention) . . . . . −65°C to +150°C
Storage temperature (with Data Retention)
Operating . . . . . −25°C to +75°C
Unpowered . . . . . −65°C to +80°C

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

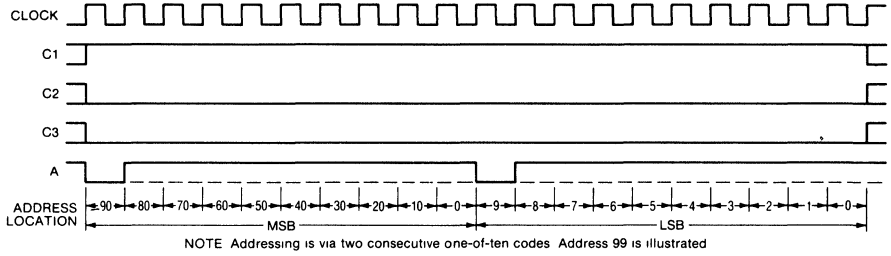
Standard Conditions (unless otherwise noted):

V_{SS} = GND
V_{GG} = −35V ±8%
Operating Temperature T_A = 0°C to +70°C

Characteristics	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input logic "1"	V_{IL}	V_{SS}−15 0	—	V_{SS}−8 0	Volts	
Input logic "0"	V_{IH}	V_{SS}−1 0	—	V_{SS}+0.3	Volts	
Input leakage	I_L	—	—	10	μA	V_{IN} = −15V
Output logic "1"	V_{OL}	—	—	V_{SS}−12 0	Volts	Load = 1.5 Meg, 100pF
Output logic "0"	V_{OH}	V_{SS}−1 0	—	V_{SS}+0 3	Volts	I_{SOURCE} = 200μA
Power consumption	P_{GG}	—	—	300	mW	
Power supply current	I_{GG}	—	—	8 0	mA	
AC CHARACTERISTICS						
Clock Frequency	fϕ	10.0	14.0	17.0	kHz	
Clock duty cycle	Dϕ	35	50	65	%	
Write time	tw	10 0	15.0	24.0	ms	
Erase time	te	10.0	15.0	24.0	ms	
Rise, fall time	tr, tf	—	—	1 0	μs	
Control, Data set up time	t_{CS}	1	—	—	μs	
Control, Data hold time	t_{CH}	0	—	—	μs	
Propagation delay	tpw	—	—	20 0	μs	Load − 1 Meg. 100pF
Non-volatile data storage	T_S	10	—	—	Years	See Note 1.
Number of erase/write cycles	N_W	—	—	10^4	—	Per word. See Note 2.
Number of read accesses between writes	N_{RA}	10^9	—	—	—	Per word

** Typical values are at +25°C and nominal voltages
NOTE 1: T_S is for powered or unpowered storage
NOTE 2: N_W (=10^4) is a maximum for data retention times greater than 10 years. Beyond 10^4 reprogramming cycles, there is a gradual, logarithmic reduction in retention time with 1 year being a typical value after 10^5 cycles.

TIMING DIAGRAMS



NOTE Addressing is via two consecutive one-of-ten codes Address 99 is illustrated

Fig.1 ACCEPT ADDRESS

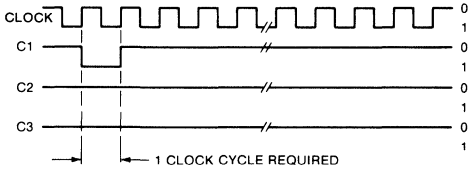
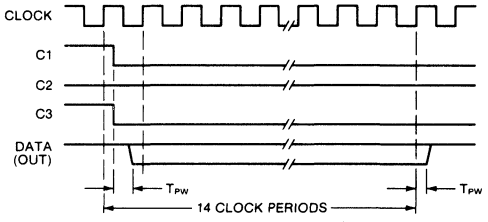


Fig.2 READ



TPW measured initially from control line transition to data out, then measured from the positive clock edges to data changes Timing measurements are made at VSS −2 and −10 volt points

Fig.3 SHIFT DATA OUT

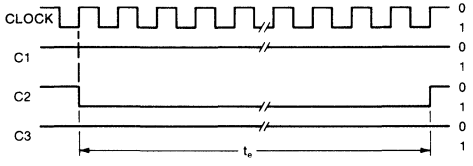


Fig.4 ERASE

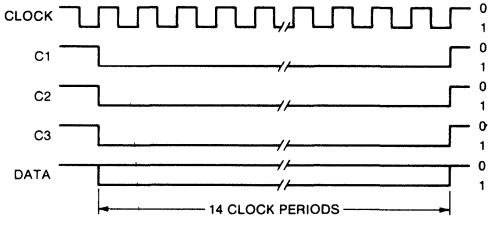


Fig.5 ACCEPT DATA

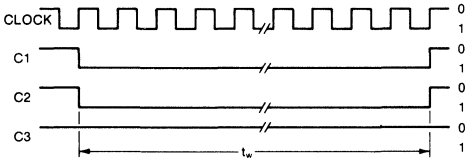


Fig.6 WRITE

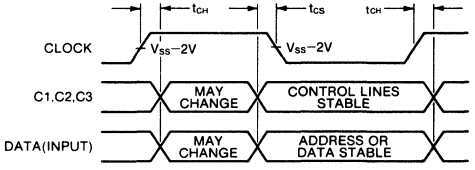


Fig.7 INPUT TIMING

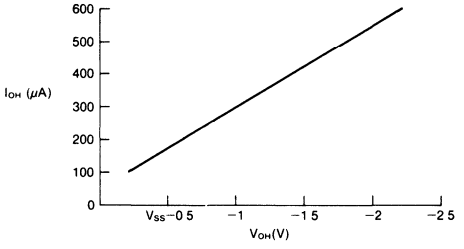


Fig.8 TYPICAL OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

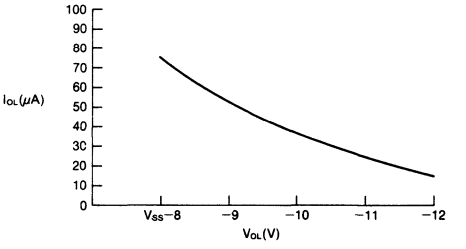


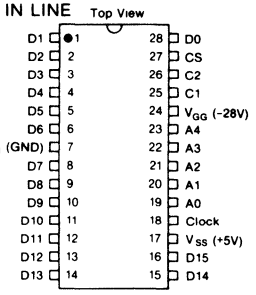
Fig.9 TYPICAL OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

512 Bit Electrically Alterable Read Only Memory

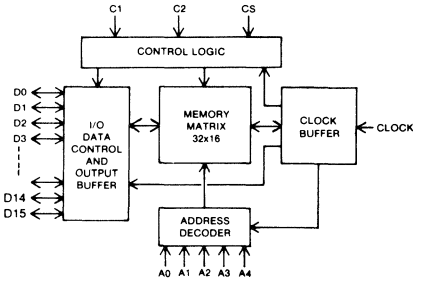
- 32 word x 16 bit organization
- 5 bit binary addressing
- +5, −28 V power supplies
- Word Alterable
- 10 year data storage for ER2051 (at +70°C)
- 1 year data storage for ER2051 IR (at +85°C) and ER2051 HR (at +125°C)
- TTL compatibility with pull-up resistors on inputs
- Tri-state outputs
- Read Time: 1μs (ER2051), 2μs (ER2051 IR and ER2051 HR)
- Write/Erase Time. 50ms (ER2051), 100ms (ER2051 HR)
- No Voltage switching required
- Chip select
- Two extended temperature ranges
  −40°C to +85°C (Industrial) Part # ER2051 IR
  −55°C to +125°C (Hi-Rel) Part # ER2051 HR

PIN CONFIGURATION

28 LEAD DUAL IN LINE Top View



BLOCK DIAGRAM



DESCRIPTION

The ER2051, ER2051 IR and ER2051 HR are fully decoded 32 x 16 electrically erasable and reprogrammable ROMs Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

The EAROM may be operated with the V_{SS} power supply between +5V and +10Volts, as long as the $V_{SS}-V_{GG}$ always equals 33 Volts Thus, V_{SS} can be +5Volts for TTL compatibility or up to +10Volts for CMOS compatibility, if V_{GG} is appropriately adjusted.

The ER2051 IR and ER2051 HR are screened to Mil Std 883B/ method 5004 1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual They are available in 28 lead ceramic dual in line packages.

OPERATION

Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which causes a positive shift in the threshold of both transistors), data is written into one of the transistors making its threshold more negative. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written."

It is important to note two things. first, that an erase is required before a wire to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

The ER2051, ER2051 IR and ER2051 HR EAROMs use dynamic, edge triggered circuits internally. This requires either a mode change, a clock or a transition of the chip select between successive operations Thus successive operations in the same mode must be separated by transitions of one of these four lines. Clock pulses are not normally required during erase or write operations, but are needed for successive operations if the chip select is held high, i e , applications where one EAROM is used

PIN FUNCTIONS

A_0-A_4	5-Bit Word Address
D_0-D_{15}	Data input and output pins
CS	Chip Select Chip selected at logic "1" When chip select is at logic "0", outputs are open circuit, read, write and erase are disabled Power is reduced
C1, C2	Mode Control Inputs C1 C2 0 1 Erase Mode stored data is erased at addressed location 1 Don't Care Read Mode addressed data read after clock pulse Output data retained at output pins until chip deselected or control lines switched 0 0 Write Mode input data written at addressed location Clock not required
CLK	Clock input Pulse to logic "1" for read operation
V_{SS}	Substrate supply Normally at +5 volts
V_{GI}	Ground Input
V_{GG}	Power Supply Input Normally at −28 volts

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All input and outputs (with respect to V_{SS}) ..... −35V to +0.3V
Storage temperature ..... −65°C to +150°C
Soldering temperature of leads (10 seconds)..... +300°C

*Exceeding these ratings could cause permanent damage to the device This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Data labeled "typical" is presented for design guidance only and is not guaranteed.

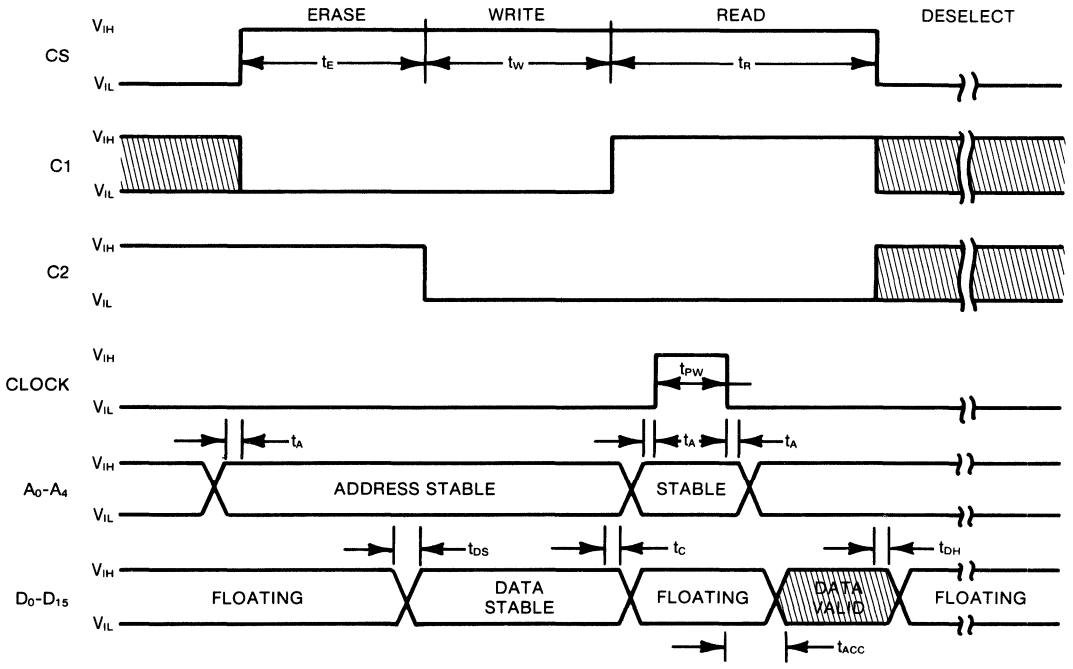
Standard Conditions (for TTL compatibility)

V_{SS} = +5V ±5%
V_{GG} = −28V ±5%
v_{GI} = GND
Operating Temperature T_A = 0°C to +70°C for ER2051
T_A = −40°C to +85°C for ER2051 IR
T_A = −55°C to +125°C for ER2051 HR
Output Load = 100pf, 1 TTL load

		ER2051			ER2051 IR/ER2051 HR				
Characteristics	**Sym**	**Min.**	**Typ.****	**Max.**	**Min.**	**Typ.****	**Max.**	**Units**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1 5	—	V_{SS} +0 3	V_{SS} −1 5	—	V_{SS} +0 3	V	
Input Logic "0"	V_{IL}	V_{SS} −15	—	0 8	V_{SS} −10	—	0 6	V	
Output Logic "1"	V_{OH}	V_{SS} −1 5	—	—	V_{SS} −1 5	—	—	V	I_{OH} = 100μA
Output Logic "0"	V_{OL}	—	—	0 6	—	—	0 6	V	I_{OL} = 1.6mA for V_{SS} = 5V
Input Leakage	I_L	—	2	10	—	2	10	μA	V_{IN} = V_{SS} −15
Output Leakage	I_O	—	2	10	—	2	10	μA	Chip deselected
Power Supply Current									
Read	I_{GG}	—	—	14	—	—	18	mA	I_{GG} returned through V_{SS}
Write	I_{GG}	—	—	11	—	—	15	mA	
Erase	I_{GG}	—	—	11	—	—	15	mA	
Deselected	I_{GG}	—	—	9	—	—	12	mA	
AC CHARACTERISTICS									
Access Time	t_{ACC}	—	—	1.0	—	—	2.0	μs	
Clock Pulse width	t_{PW}	2 0	—	20 0	2 0	—	20 0	μs	
Erase Cycle Time	t_E	50	—	200 0	100	—	200 0	ms	
Write Cycle Time	t_W	50	—	200 0	100	—	200 0	ms	
Read Cycle Time	t_R	3 5	—	24 0	4.5	—	25	μs	
Address to Clock Time	t_A	50	—	—	50	—	—	ns	
Data Set Up Time	t_{DS}	50	—	—	50	—	—	ns	
Data Hold Time	t_{DH}	50	—	—	50	—	—	ns	
Control to Address & Data Change	t_C	0	—	—	0	—	—	ns	
Number of Reads/Word Refresh	N_{RA}	10''	—	—	10''	—	—		
Number of Erase/Write Cycles	N_W	10^6	—	—	10^5	—	—	—	
Input Capacitance, all pins	C_{10}	—	8	15	—	8	15	pF	
Unpowered Data Storage Time	t_S	10	—	—	1	—	—	Years	at max temperature
Power Dissipation Read Cycle	P_D	—	450	500	—	450	500	mW	at 25°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	500	mW	at 125°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	600	mW	at −55°C V_{SS} = +5, V_{GG} = −29
Pulse Rise, fall time	t_{R1} t_F	10	—	100	10	—	100	ns	

**Typical values are at +25°C and nominal voltages

TIMING DIAGRAM



512 Bit Electrically Alterable Read Only Memory

FEATURES

- 64 word x 8 bit organization
- 6 bit binary addressing
- +5, −28V power supplies
- Word Alterable
- 10 year data storage for ER2055 (at +70°C)
- 1 year data storage for ER2055 IR (at +85°C) and ER2055 HR (at +125°C)
- TTL compatible with pull-up resistors on inputs
- Tri-state outputs
- Read Time: 2μs (ER2055), 4μs (ER2055 IR and ER2055 HR)
- Write/Erase Time: 50ms (ER2055), 100ms (ER2055 HR)
- No voltage switching required
- 2 chip selects
- Two extended temperature ranges:
  −40°C to +85°C (Industrial) Part # ER2055 IR
  −55°C to +125°C (Hi-Rel) Part # ER2055 HR

DESCRIPTION

The ER2055 is a fully decoded 64 x 8 electrically erasable and reprogrammable ROM. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

OPERATION

Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which causes a positive shift in the threshold of both transistors), data is written into one of the transistors making its threshold more negative. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written".

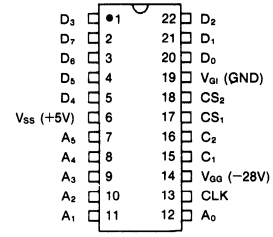
The ER2055 EAROM may be operated with V_{SS} between +5 and +10 volts for either TTL or CMOS compatibility. The negative power supply, V_{GG}, should be adjusted so that the difference between V_{SS} and V_{GG} is always 33 volts.

It is important to note two things: first, that an erase is required before a write to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

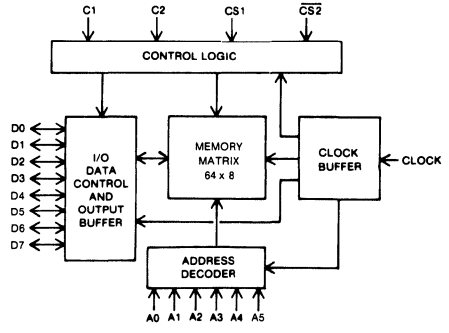
PIN CONFIGURATION

22 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



The ER2055 EAROM uses dynamic edge triggered circuits internally. This requires either a mode change, a clock or a transition of the chip selects between successive operations. Thus successive operations in the same mode must be separated by transition of one of these four lines. Clock pulses are not normally required during erase or write operations, but are needed for successive operations if the chip is continuously selected, i.e., applications where one EAROM is used.

The ER2055IR and ER2055HR are screened to Mil Std. 883B/ method 5004. 1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. They are available in 28 lead ceramic dual in-line packages.

PIN FUNCTIONS

A_0-A_5	6-Bit Word Address		
D_0-D_7	Data input and output pins		
CS1, $\overline{CS2}$	Chip Selects Chip selected at logic "1" on CS1 and logic "0" on $\overline{CS2}$. When chip is not selected, outputs are open circuit, read, write and erase are disabled. Power is reduced.		
C1, C2	Mode Control Inputs		
	C1	C2	
	0	1	Erase Mode stored data is erased at addressed location
	1	Don't Care	Read Mode. addressed data read after clock pulse Output data retained at output pins until chip deselected or control lines switched.
	0	0	Write Mode: input data written at addressed location Clock not required
CLK	Clock Input Pulse to logic "1" for read operation		
V_{SS}	Substrate supply. Normally at +5 volts		
V_{GI}	Ground Input.		
V_{GG}	Power Supply Input. Normally at −28 volts.		

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to V_{SS}) ..... −35V to +0 3V
Storage temperature ..... −65° C to +150° C
Soldering temperature of leads (10 seconds) ..... +300° C

Standard Conditions (for TTL Compatibility)

V_{SS} = +5V ±5%
V_{GG} = −28V ±5%
V_{GI} = GND
Operating Temperature T_A = 0° C to +70° C for ER2055
T_A = −40° C to +85° C for ER2055IR
T_A = −55° C to +125° C for ER2055HR
Output Load = 100pF, 1 TTL load

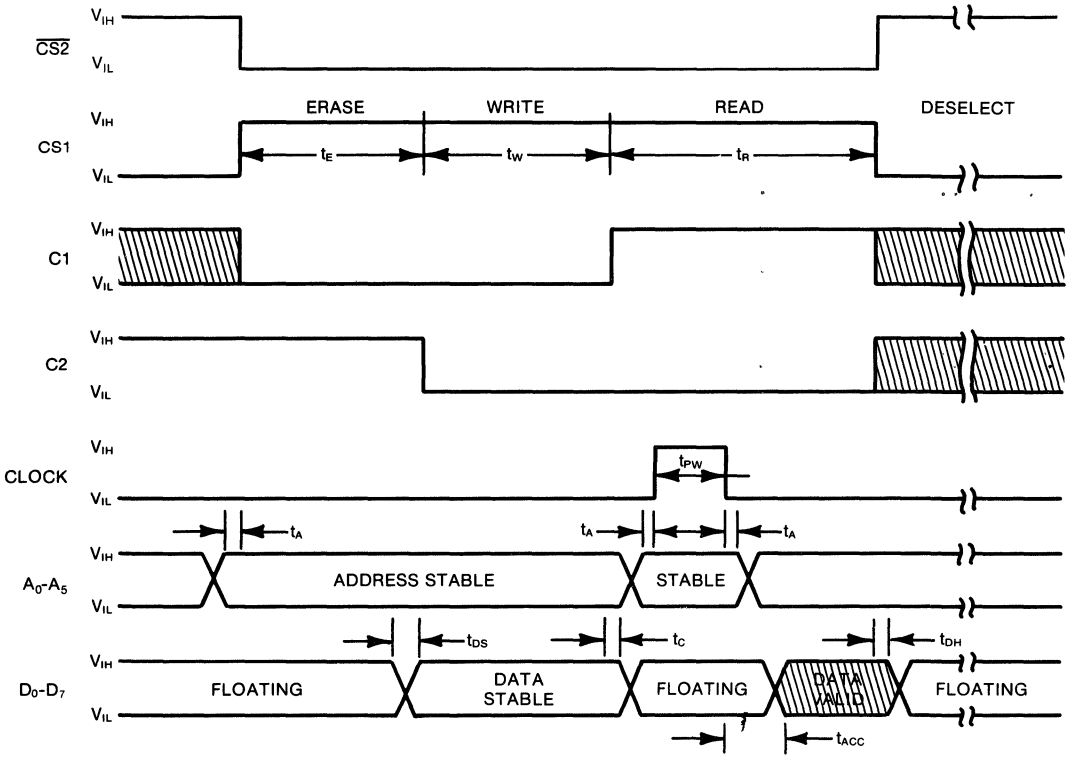
*Exceeding these ratings could cause permanent damage to the device This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

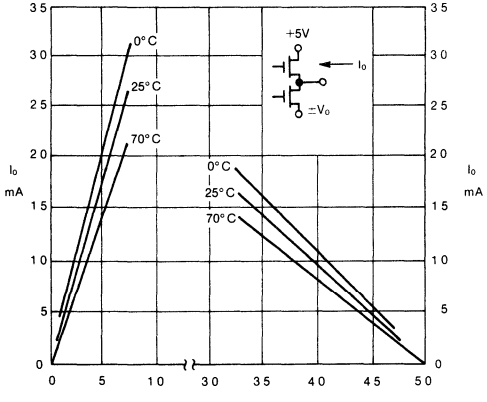
		ER2055			ER2055 IR/ER2055 HR				
Characteristics	**Sym**	**Min.**	**Typ.****	**Max.**	**Min.**	**Typ.****	**Max.**	**Units**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1.5	—	V_{SS} +0.3	V_{SS} −1.5	—	V_{SS} +0.3	V	
Input Logic "0"	V_{IL}	V_{SS} −15	—	0.8	V_{SS} −10	—	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} −1.5	—	—	V_{SS} −1.5	—	—	V	I_{OH} = 100μA
Output Logic "0"	V_{OL}	—	—	0.6	—	—	0.6	V	I_{OL} = 1.6mA for V_{SS} = 5V
Input Leakage	I_L	—	2	10	—	2	10	μA	V_{IN} = V_{SS} −15
Output Leakage	I_O	—	2	10	—	2	10	μA	Chip deselected
Power Supply Current									
Read	I_{GG}	—	8	10	—	8	18	mA	I_{SS} approx. I_{GG}
Write	I_{GG}	—	6	7	—	6	9	mA	I_{SS} approx. I_{GG}
Erase	I_{GG}	—	4	7	—	6	8	mA	I_{SS} approx. I_{GG}
Deselected	I_{GG}	—	4	7	—	4	6	mA	I_{SS} approx. I_{GG}
AC CHARACTERISTICS									
Access Time	t_{ACC}	—	—	2.0	—	—	4.0	μs	
Clock Pulse width	t_{PW}	2 0	—	20.0	2.0	—	20.0	μs	
Erase Cycle Time	t_E	50	—	200.0	100	—	200.0	ms	
Write Cycle Time	t_W	50	—	200.0	100	—	200.0	ms	
Read Cycle Time	t_R	5.0	—	24.0	6.0	—	25.0	μs	
Address to Clock Time	t_A	50	—	—	50	—	—	ns	
Data Set Up Time	t_{DS}	50	—	—	50	—	—	ns	
Data Hold Time	t_{DH}	50	—	—	50	—	—	ns	
Control to Address & Data Change	t_C	0	—	—	0	—	—	ns	
Number of Reads/Word Refresh	N_{RA}	10^{11}	—	—	10^{11}	—	—		
Number of Erase/Write Cycles	N_W	10^6	—	—	10^5	—	—	—	
Input Capacitance, all pins	C_{IO}	—	6	10	—	6	10	pF	
Unpowered Data Storage Time	t_S	10	—	—	1	—	—	Years	at max. temperature
Power Dissipation Read Cycle	P_D	—	450	500	—	450	500	mW	at 25° C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	500	mW	at 125° C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	600	mW	at −55° C V_{SS} = +5, V_{GG} = −29
Pulse Rise, fall time	t_{R1} t_F	10	—	100	10	—	100	ns	

**Typical values are at +25° C and nominal voltages.

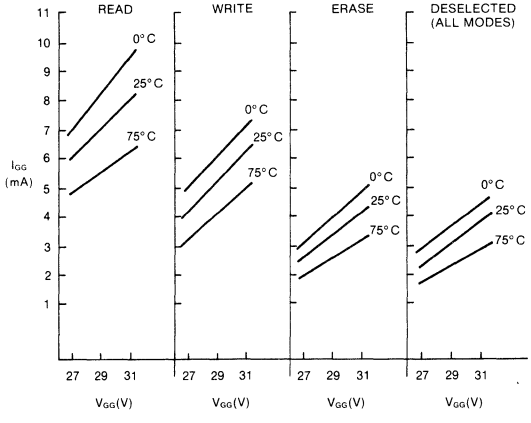
TIMING DIAGRAM



TYPICAL OUTPUT CHARACTERISTICS



TYPICAL SUPPLY CURRENT VS POWER SUPPLY VOLTAGE



1K N-Channel EEPROM

FEATURES

- 128 x 8 bit organization, fully decoded
- SNOS si-gate technology
- Single +5V power supply
- 100ns access time
- TTL compatible
- Word alterable
- Reprogramming time-user determined
- Automatic erase/write cycle

DESCRIPTION

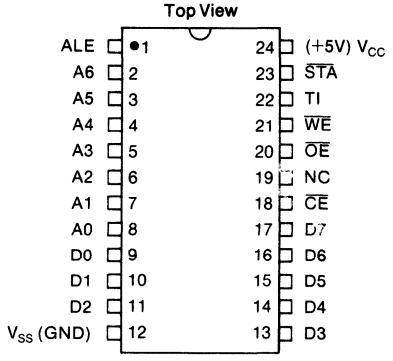
The ER5901 is intended for microcomputer applications which require a small non-volatile memory capable of fast operation with a minimum of processor intervention. The fast access time, coupled with the ability to multiplex the address and data lines, through the Address Latch Enable (ALE) and $\overline{WE}$ inputs, will make it readily adaptable for use in most systems.

A single pulse on the $\overline{WE}$ input will cause the device to perform a complete erase/write cycle without any further processor intervention. The duration of this reprogramming cycle can be determined by means of an external RC time constant connected to the TI input. During the reprogramming cycle a busy status is made available on the status line $\overline{STA}$.

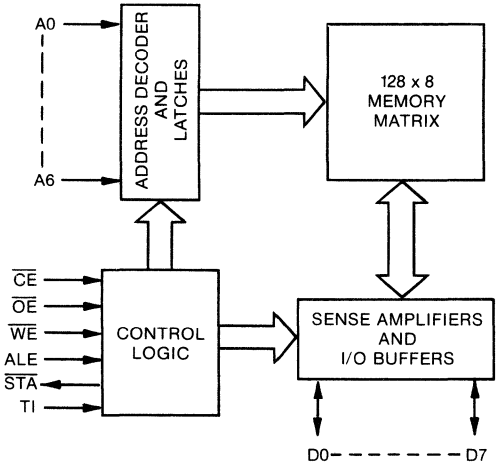
The combining of all these features on a single device has been achieved through innovative circuit design and N-channel Si-gate technology.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELEC. ALTERABLE NON-VOLATILE MEMORY

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to Ground ..... +6V to −0.3V
Storage temperature (unpowered and without data retention) ..... −65°C to +150°C
Soldering temperature of leads (10 secs.) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

V_{SS} = GND
V_{CC} = +5V ±5% Volts
Operating Temperature Ranges T_A: 0°C to + 70°C (Commercial)
−40°C to +85°C (Industrial)
−55°C to +125°C (Military)

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Logic "1"	V_{IH}	2 0	—	V_{CC}+0 3	V	
Input Logic "0"	V_{IL}	−0.1	—	+0.8	V	
Output Logic "1"	V_{OH}	2 4	—	V_{CC}	V	I_{OH} = −400μA
Output Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Input Leakage Current	I_{IL}	—	—	**	μA	V_{IN} = 5.25V
Output Leakage Current	I_{OL}	—	—	**	μA	V_{OUT} = 5 25V
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	—	35	54	mA	V_{CC} = +5.5V
Chip Deselected	I_{CC}	—	12	18	mA	V_{CC}= +5.5V
Power Dissipation						
Chip Selected	P_D	—	195	300	mW	V_{CC} = +5 5V
Chip Deselected	P_D	—	66	100	mW	V_{CC} = +5 5V

** To be announced at a later date.

NOTE: 1. T_A = −40°C to + 85°C, V_{CC} = 5±5% Volts, unless otherwise specified.

PIN FUNCTIONS

Name	Function
A0-A6	7 bit binary word address.
D0-D7	8 bit data I/O
V_{CC}	Power supply +5V ± 5%
GND	Chip Ground connection
$\overline{CE}$	Chip Enable input — used for chip selection
$\overline{OE}$	Output Enable input — gates data to output pins during Read.
$\overline{WE}$	Write Enable input — enables a reprogramming cycle, input data latched on a positive edge.
ALE	Address Latch Enable input — address inputs latched on negative edge May be tied to $\overline{WE}$ when separate address and data lines are used
$\overline{STA}$	Status output pin — low when chip is in reprogramming mode and cannot be accessed.
TI	Timing input — defines clock frequency for reprogramming, May be RC or other external clock

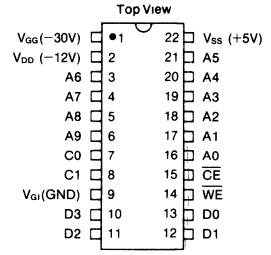
4096 Bit Electrically Alterable Read Only Memory

FEATURES

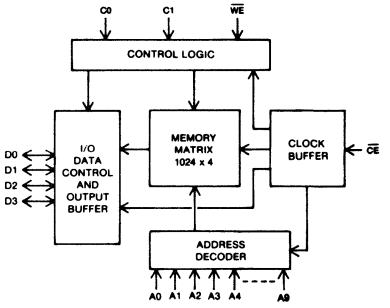
- 1024 word x 4 bit organization
- Latched address and data inputs
- Word or block alterable
- 10 year data storage for ER3400
- 1 year data storage for ER3400IR at +85° C
- and ER3400HR at +95° C
- TTL compatible with pull-up resistors on inputs
- Tri-state outputs
- Read access time 900ns max.
- Write time. 1ms Erase time 10ms
- 10^9 Read cycles/word between refreshes
- 10^7 Read cycles/word for ER3400IR and ER3400HR
- Two extended temperature ranges

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



DESCRIPTION

The ER3400 is a 1024 x 4 bit fully decoded Electrically Alterable Read Only Memory fabricated in General Instrument's proven MNOS technology. Address, control and data inputs are latched on board the device thus releasing these lines during Erase and Write operations Selection of one of the four modes of operation is made by setting the appropriate binary code on control lines C0 and C1 $\overline{CE}$ is used for chip selection and latching of address and control lines. $\overline{WE}$ is used to sample and latch input data on D0-D3 during a Write operation.

Power sequencing protection circuitry is provided on the ER3400 to protect against the accidental alteration of data during power Up/Down. However, due to the unpredictable nature of power up and power down sequences in some systems, it is important to apply and remove the programming voltage V_{GG} only when V_{SS} and V_{DD} are within their specified limits

For applications requiring extended temperature ranges the ER3400I, ER3400IR and ER3400HR are available.

RELATED APPLICATION NOTES

1217 The ER3400: an easy to use 4K EAROM
1218 Interfacing the ER3400 to an eight bit microcomputer
1220 Generating EAROM programming voltages from a 5 volt supply
1210 Data retention testing of the ER3400

PIN FUNCTIONS

Name	Function
A0-A9	10-Bit Word Address
D0-D3	Data input and output pins
$\overline{CE}$	Chip Enable. Chip selected when $\overline{CE}$ is pulsed to logic "0".
C0, C1	Mode Control Inputs C0 C1 0 1 Block Erase Mode: erase operation performed on all words. 1 1 Word Erase Mode: stored data is erased at addressed location. 0 0 Read Mode: addressed data read after leading edge of $\overline{CE}$ pulse. 1 0 Write Mode: input data written at addressed location.
$\overline{WE}$	Write Enable. Input data read when $\overline{WE}$ is pulsed to logic "0".
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{DD}	Power Supply Input. Normally at -12 volts.
V_{GG}	Power Supply Input. Normally at -30 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs except V_{GG} (with respect to V_{SS}).... −20V to +0.3V
Storage temperature (without data retention) ..... −65° C to +150° C
Soldering temperature of leads (10 seconds) ..... +300° C

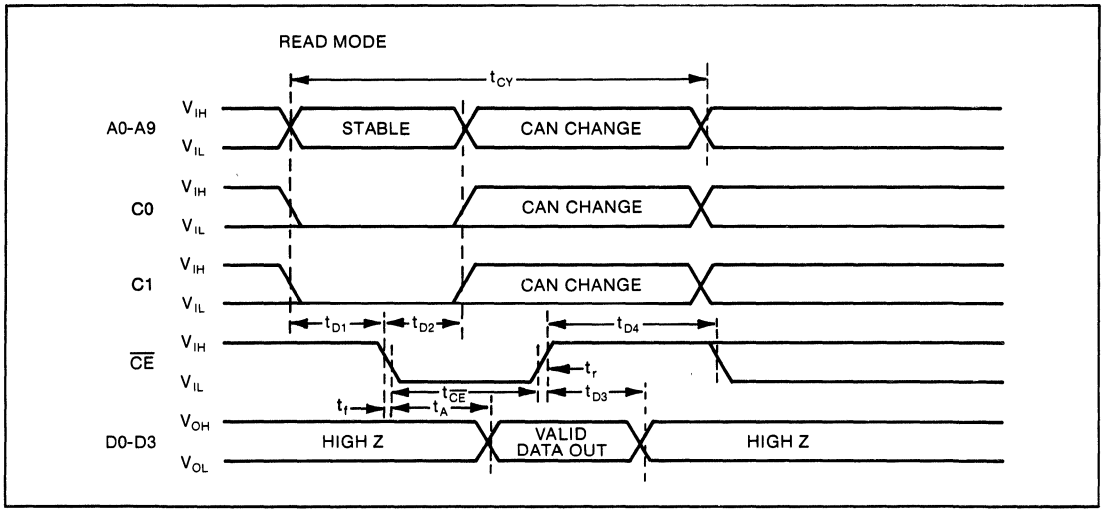
Standard Condition (unless otherwise noted)

V_{SS} = +5V to ±5%
V_{DD} = −12V ±5%
V_{GG} = −30V ±5%
V_{GI} = GND
Operating Temperature (T_A) = 0° C to +70° C (ER3400)
−40° C to +85° C (ER3400I/IR)
−55° C to +95° C (ER3400HR)

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Data labeled "typical" is presented for design guidance only and is not guaranteed.

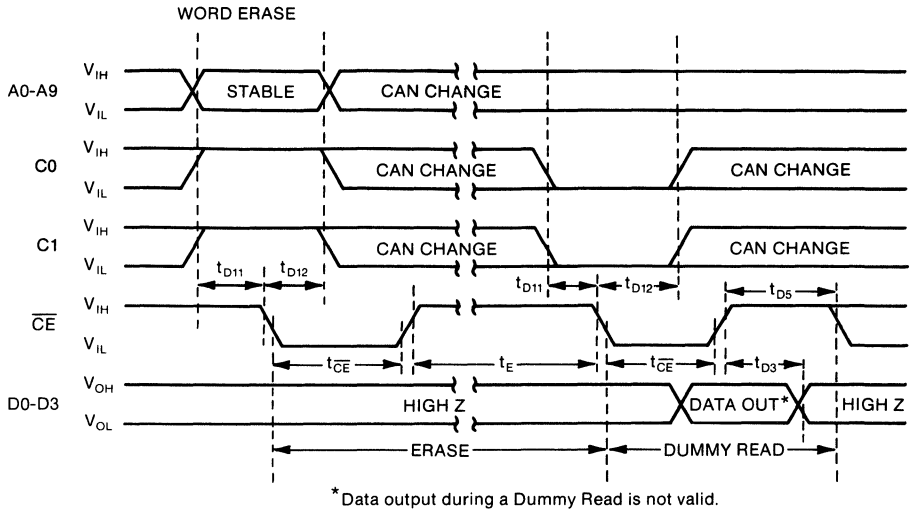
		ER3400			ER3400IR/ER3400HR				
Characteristic	**Sym**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1.5	—	V_{SS} +0.15	V_{SS} −1 0	—	V_{SS} +0 15	V	
Input Logic "0"	V_{IL}	−10	—	0 8	−10	—	0 6	V	
Output Logic "1"	V_{OH}	V_{SS} −1.5	—	—	V_{SS} −1.5	—	—	V	I_{OH} = 2mA
Output Logic "0"	V_{OL}	—	—	0 4	—	—	0 5	V	I_{OL} = 2mA
Control Input Leakage	I_{LC}	—	—	−2 0	—	—	−2 0	μA	$V_{ON} = V_{SS}$ −15 Volts
Data Input Leakage	I_{LD}	—	—	−10 0	—	—	−10.0	μA	$V_{IN} = V_{SS}$ −15 Volts
Power Supply Current									
V_{DD} Supply Current. Chip selected	I_{DD}	—	—	−25.0	—	—	−30.0	mA	$V_{DD} = V_{SS}$ −17 Volts
Chip de-selected	I_{DD}	—	—	−12.0	—	—	−15.0	mA	$V_{DD} = V_{SS}$ −17 Volts
V_{GG} Supply Current· Write mode	I_{GG}	—	—	−4.0	—	—	−5.0	mA	$V_{GG} = V_{SS}$ −35 Volts
V_{SS} Supply Current. Chip selected	I_{SS}	—	—	−31 0	—	—	−37.0	mA	$V_{GG} = V_{SS}$ −17V, $V_{GG} = V_{SS}$ −35V
Chip de-selected	I_{SS}	—	—	−14.5	—	—	−18.0	mA	$V_{GG} = V_{SS}$ −17V, $V_{GG} = V_{SS}$ −35V
AC CHARACTERISTICS									
Input capacitance—control inputs	C_I	—	6	8	—	6	8	pf	
Input capacitance—data inputs	C_D	—	8	10	—	8	10	pf	



Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Read Cycle Time	t_{CY}	1700	—	1750	—	ns	
Address and Control to $\overline{CE}$	t_{D1}	100	—	100	—	ns	
Address and Control Hold Time	t_{D2}	250	—	350	—	ns	
$\overline{CE}$ Rise to Data Tri-state	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High	t_{D4}	700	—	750	—	ns	
Access Time	t_A	—	900	—	1000	ns	Load = 2K + 100pf to V_{SS}
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
$\overline{CE}$ Rise, Fall Time	t_r, t_f	10	100	10	100	ns	
Number of Read Accesses per Location Between Refresh	N_{RA}	10^9	—	10^7	—	—	

READ OPERATION

Address and control line inputs are latched on the falling edge of $\overline{CE}$. With control lines C0 and C1 both low a read cycle will be initiated. After the access time t_A the data read will be output on data lines D0-D3. $\overline{CE}$ must be held high for a minimum of 700ns between memory read cycles. To reduce power consumption the ER3400 may be operated with V_{GG} held at V_{SS} in the read mode.



*Data output during a Dummy Read is not valid.

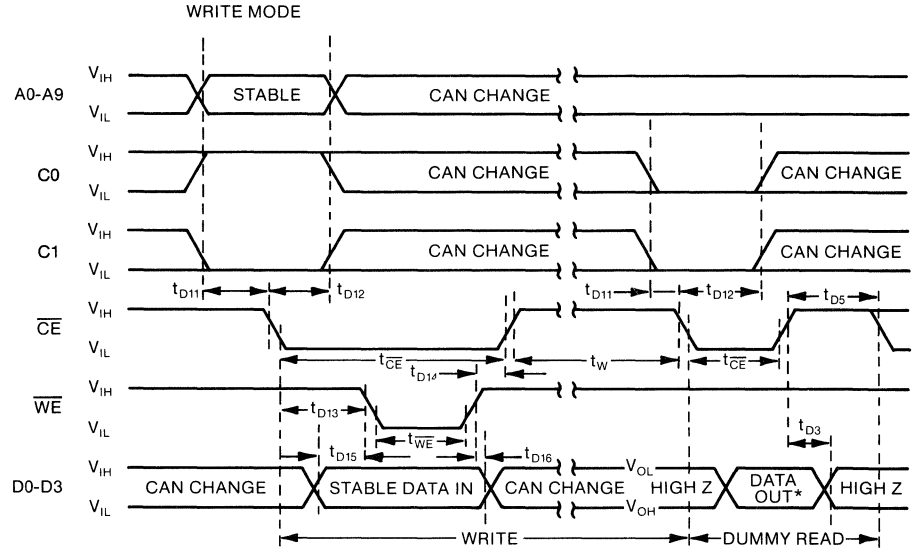
Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Address and Control to $\overline{CE}$	t_{D11}	100	—	100	—	ns	
Address and Control Hold Time	t_{D12}	250	—	250	—	ns	
$\overline{CE}$ Rise to Data Tri-state	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High (Dummy Read)	t_{D5}	1500	—	1500	—	ns	
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
Erase Time	t_E	10	20	10	20	ms	

WORD ERASE OPERATION

An erase cycle is required prior to a write in order to precondition the memory cells to be written. A word erase operation erases only the four bits of the addressed memory location. The falling edge of $\overline{CE}$ latches the control inputs and the address of the word to be erased. The rising edge of $\overline{CE}$ in the erase mode signals the start of the erase cycle which produces a positive shift in the threshold of the selected MNOS memory transistors. An erase operation must be terminated by a dummy read operation The dummy read need not occur on the same location as the preceding erase, therefore, the state of the address lines A0-A9 are immaterial during the dummy read cycle. Data output during a dummy read cycle is not valid data.

BLOCK ERASE OPERATION

A block erase operation erases all 4096 bits of memory to the "1" state, in all other respects the operation is identical to the word erase operation described above.



*Data output during a Dummy Read is not valid

Characteristics	Sym	ER3400 Min	ER3400 Max	ER3400IR/HR Min	ER3400IR/HR Max	Unit	Conditions
Address and Control to $\overline{CE}$	t_{D11}	100	—	100	—	ns	
Address and Control Hold Time	t_{D12}	250	—	350	—	ns	
$\overline{CE}$ Fall to $\overline{WE}$ Fall Delay	t_{D13}	0	—	0	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$
$\overline{WE}$ Rise to $\overline{CE}$ Rise Delay	t_{D14}	−50	—	−100	—	ns	rise by 50ns maximum
Data Stable to $\overline{WE}$	t_{D15}	0	—	0	—	ns	
$\overline{WE}$ Rise to End of Data Stable	t_{D16}	100	—	100	—	ns	
$\overline{CE}$ Pulse Width	$t_{\overline{CE}}$	1	50	1	50	μs	
$\overline{WE}$ Pulse Width	$t_{\overline{WE}}$	500	—	650	—	ns	
Write Time	t_W	1	2	1	2	ms	
$\overline{CE}$ Rise to Data Tri-state	t_{D3}	50	300	50	350	ns	
$\overline{CE}$ High (Dummy Read)	t_{D5}	1500	—	1500	—	ns	
Unpowered Data Storage Time	t_S	10	—	1	—	YRS.	See Note 1
Number of Reprogramming Cycles	N_W	10^3	—	10^3	—	—	See Note 1
Number of Read Accesses/Location between Refresh	N_{RA}	10^9	—	10^9	—	—	

NOTE 1: Does not imply end of useful life See "Write Operation" for further information.

WRITE OPERATION

Control lines C0 and C1 along with address lines A0-A9 are latched on the falling edge of $\overline{CE}$ Input data on D0-D3 is latched on the rising edge of $\overline{WE}$. $\overline{WE}$ may be tied to $\overline{CE}$ for all operations, however, this separate latching allows the ER3400 to be used in certain systems where address and data busses are multiplexed. The writing of the selected memory transistors is initiated by the rising edge of $\overline{CE}$. $\overline{CE}$ must remain high for the duration of the write time. A write operation can only be terminated by a dummy read. To avoid bus contention, the data lines must be tri-stated prior to initiating the dummy read cycle. The data output by a dummy read cycle is not valid data. The dummy read need not occur on the same location as the previous write, therefore, address line A0-A9 may be allowed to change during the dummy read cycle

The specification of 10 years non-volatile data retention after a minimum of 10^3 reprogramming cycles is merely one point on the curve of retention versus reprogramming cycles and does not imply a sudden cut-off or end of life. As the number of Erase/Write cycles per address increases, a gradual, logarithmic reduction in data retention capability occurs with 1 year of retention being a typical figure after 10^4 cycles.

TYPICAL CHARACTERISTIC CURVES

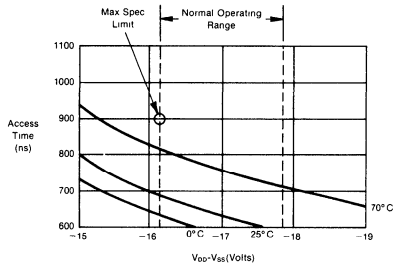


Fig.3 TYPICAL ACCESS TIME vs. POWER SUPPLY VOLTAGE

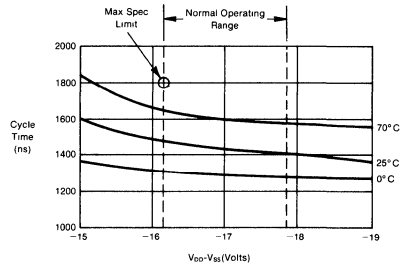


Fig.4 TYPICAL CYCLE TIME vs. POWER SUPPLY VOLTAGE

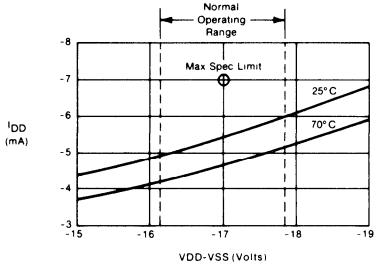


Fig.5 I_{DD} vs. V_{DD}-V_{SS} POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED

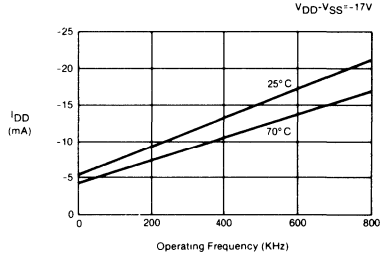


Fig.6 I_{DD} vs. OPERATING FREQUENCY IN READ MODE AND SELECTED

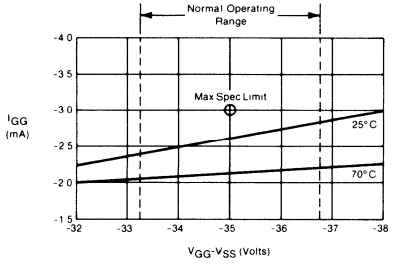


Fig.7 I_{GG} vs. V_{GG}-V_{SS} POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED

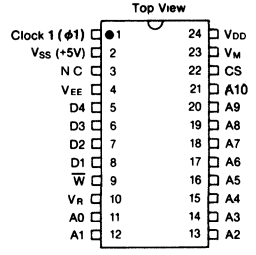
8192 Bit Electrically Alterable Read Only Memory

FEATURES

- 2048 word x 4 bit organization
- 11 bit binary addressing
- ±5, −14, −24V power supplies
- Block erasable
- 1 year unpowered data storage
- TTL compatible with pull up resistors on inputs
- Tri-state outputs
- Read time: 1.6μs
- Write time: 10ms, erase time: 100ms
- Chip select

PIN CONFIGURATION

24 LEAD DUAL IN LINE



DESCRIPTION

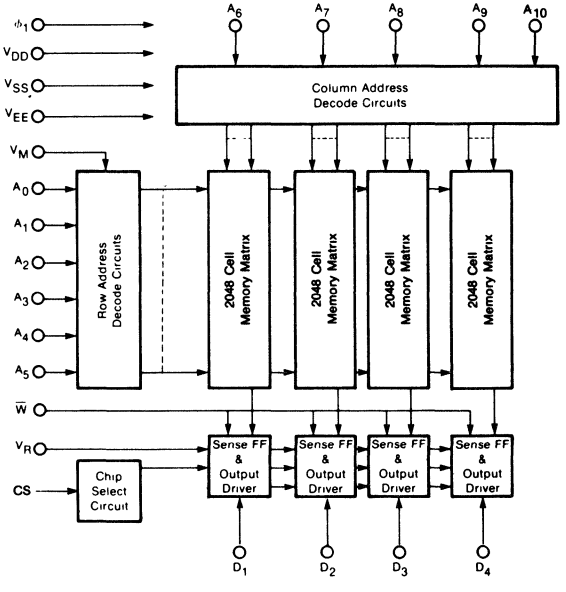
The ER2810 IR and ER2810 HR are fully decoded 2048 x 4-bit electrically erasable and reprogrammable ROMs utilizing second-generation MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 8192 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

The ER2810 IR and ER2810 HR are screened to Mil Std. 883B/ method 5004.1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual They are available in 24 lead ceramic dual in line packages.

Stored data may be accessed a minimum of 2×10^{10} times without refresh and is non-volatile in the unpowered state in excess of one year. Data is erased by applying a V_{SS} −28V pulse to the erase substrate of the device. Data may be reprogrammed, without degradation of the retention time, up to 10^5 times, beyond which a gradual, logarithmic fall off is seen. All outputs are at logic high when the device is in the erased state.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs relative to V_{SS} ..... +0.3V to −30V
Storage temperature ..... −65° C to +150° C
Soldering temperature of leads (10 seconds) ..... +300° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

RECOMMENDED OPERATING CONDITIONS T_A = −40° C to +85° C for ER2810IR
T_A = −55° C to +95° C for ER2810HR

Symbol	Parameter	Erase Mode			Write Mode			Read Mode			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply Voltage	4.75	V_{SS}	V_{SS}+0.3	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{SS}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage	—	V_{SS}	—	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-10.5	V_{SS}-10	V_{SS}-9.5	V
V_R	Reference voltage	—	V_{SS}	—	—	V_{SS}	—	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{EIH}	Erase substrate input high	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V
V_{EIL}	Erase substrate input low	V_{SS}-29	V_{SS}-28	V_{SS}-27	Not Applicable			Not Applicable			V
V_{WH}	Write control input high	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{WI}	Write control input low	V_{SS}-29	—	V_{SS}-4.4	V_{SS}-29	—	V_{SS}-4.4	Not Applicable			V
$V\phi_H$	ϕ_1 input high voltage	—	V_{SS}	—	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V
$V\phi_L$	ϕ_1 input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{IH}	Address and CS input high	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{IL}	Address and CS input low	Don't Care			V_{DD}	—	V_{SS}-4.4	V_{DD}	—	V_{SS}-4.4	V
V_{DH}	Data input high voltage	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	Not Applicable			V
V_{DI}	Data input low voltage	Don't Care			V_{DD}	—	V_{SS}-4.4	Not Applicable			V

STATIC ELECTRICAL CHARACTERISTICS T_A = −40° C to +85° C for ER2810IR
T_A = −55° C to +95° C for ER2810HR
(NO EXTERNAL LOADS EXCEPT AS NOTED)

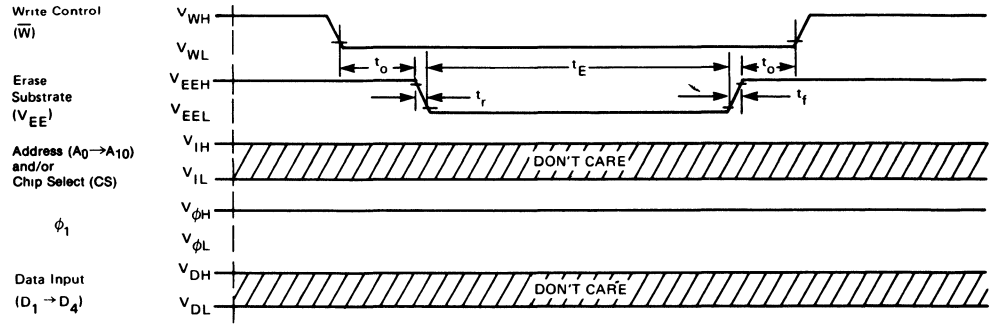
Symbol	Parameter	Conditions All Pins at V_{SS} Unless Noted	Min	Typ	Max	Unit
I_{IN}	Input leakage current (except pins 1, 2, 4, 5, 6, 7, 8, and 24) at V_{SS}-15V	$\phi 1$=V_{DD}=V_{SS}-20	—	—	-2.0	μA
$I\phi_1$	ϕ_1 leakage current at V_{SS}-29V	V_{DD}=V_{SS}-29, $\overline{W}$=V_{SS}-25	—	—	-200	μA
I_O	Output leakage current at V_{SS}-15V	Chip deselected	—	—	-10.0	μA
I_{EIL}	Erase leakage current at V_{SS}-28V	$\overline{W}$=V_{SS}-25	—	—	-200	μA
I_{DD1}	V_{DD} supply current - read mode at V_{SS}-19V	Outputs open (See Figure 6)	—	16	20	mA
I_{DD2}	V_{DD} supply current - Write mode at V_{SS}-28V	Outputs open (See Figure 5)	—	30	40	mA
V_{OH}	Data output high voltage - TTL load	One Series 7400 TTL load with R_S = 1K, V_{CC} = V_{SS}	V_{SS} −1.5	—	—	V
V_{OL}	Data output low voltage - TTL load	(See TTL Notes)	—	—	V_{SS} −10	V
V_{OH}	Data Output high voltage - MOS		V_{SS}-1.5	—	—	V
V_{OI}	Data Output low voltage — MOS	C_L = 100pF	—	—	V_{SS} −14	V
T_S	Unpowered nonvolatile data storage	Typical write conditions	1	—	—	Years

CAPACITANCE AT V_{IN} = V_{SS}, ALL OTHER PINS GROUNDED (V_{SS}), f = 1MHz

Symbol	Parameter	Min	Typ	Max	Unit
C_I	Address and chip select input capacitance	—	5	7	pF
C_W	Write control input capacitance	—	10	20	pF
C_{SI}	Strobe input capacitance	—	10	15	pF
$C\phi_1$	ϕ_1 Input Capacitance.	—	40	50	pF
C_{EI}	Erase substrate capacitance	—	600	700	pF
C_D	Data input/output capacitance	—	6	10	pF

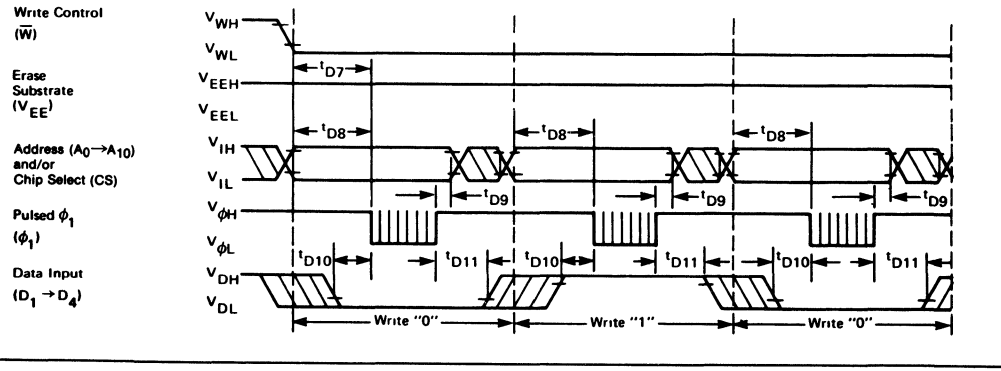
ERASE CYCLE CHARACTERISTICS $T_A = -40°C$ to $+85°C$ for ER2810IR
$T_A = -55°C$ to $+95°C$ for ER2810HR

Symbol	Parameter	Min	Typ	Max	Units
t_E	V_{FF} erase pulse width	100	—	1000	ms
t_R, t_F	V_{FF} rise time, V_{FF} fall time	0.01	—	1.0	ms
t_O	Write-erase overlap	10	—	—	μs



WRITE CYCLE CHARACTERISTICS $T_A = -40°C$ to $+85°C$ for ER2810IR
$T_A = -55°C$ to $+95°C$ for ER2810HR (See Note 3)

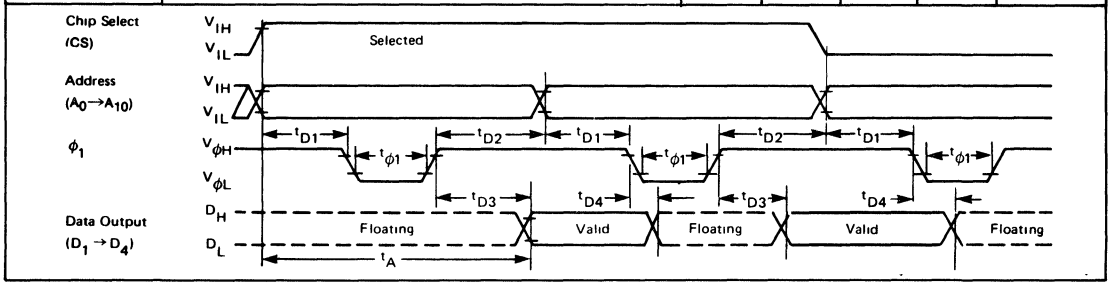
Symbol	Parameter	Min	Typ	Max	Units
$N\phi_W$	Number of ϕ_1 write pulses at 100 μs ±10%, 5 μs min. dead time between pulses)	100	200	300	Pulses
t_{D7}	Write control rise to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D8}	Address change and chip select fall to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D9}	Pulsed ϕ_1 fall to address and chip select change delay	0.0	—	—	μs
t_{D10}	Data input change to pulsed ϕ_1 rise delay	0.0	—	—	μs
t_{D11}	Pulsed ϕ_1 fall to data input change delay	0.0	—	—	μs
N_W	Number of times word may be rewritten	—	—	10^5	—



NOTES:
1. Due to the dynamic nature of the circuit a "ϕ_1 NOT" time in excess of 40 μsec may result in a floated output condition. Consequently data must be resampled with a 40 μsec time period following the fall of ϕ_1 to ensure its validity.
2. Several seconds may be required following a programming operation for the circuit to become operable in the read mode. If data is to be verified immediately following programming, a forward current of +1mA ± 10% may be forced into the erase substrate junction (Pin 4, V_{EE}), for a period not to exceed 10 milliseconds, to quickly dissipate charge trapped at internal circuit nodes.
3. Maximum power dissipation occurs during programming. When programming multichip systems where the application of programming voltages is required for several minutes, forced air cooling is recommended to reduce package temperature. Power is not reduced when chip is deselected.
4. All typical values are at +25°C and nominal voltages.
5. ϕ pulses are required after the fall of the chip select line to force the data outputs into a high impedance state.

READ CYCLE CHARACTERISTICS $T_A = -40°C$ to $+85°C$ for ER2810IR
$T_A = -55°C$ to $+95°C$ for ER2810HR

Symbol	Parameter (See Figures 1 through 4)	Min	Typ	Max	Units	
T_A	Access time	—	16	20	μs	
$t_{\phi 1}$	Pulse width (rise and fall times ≤50ns) (See Note 1)	800	—	5000	ns	
t_{D1}	Address and chip select change to ϕ_1 fall delay	400	—	—	ns	
t_{D2}	ϕ_1 Rise to address and chip select change delay	50	—	—	ns	See Note 1
t_{D3}	ϕ_1 Rise to data output valid delay (See Notes 1 and 2)	—	—	750	ns	See Note 1
t_{D4}	ϕ_1 Fall to floated output delay	—	—	300	ns	
N_{RA}	Number of read accesses/word between refresh	2×10^{10}	—	—	—	



PIN FUNCTIONS

Chip Select (CS)
Must be in the high state to enable the data output terminals or to write data into the device

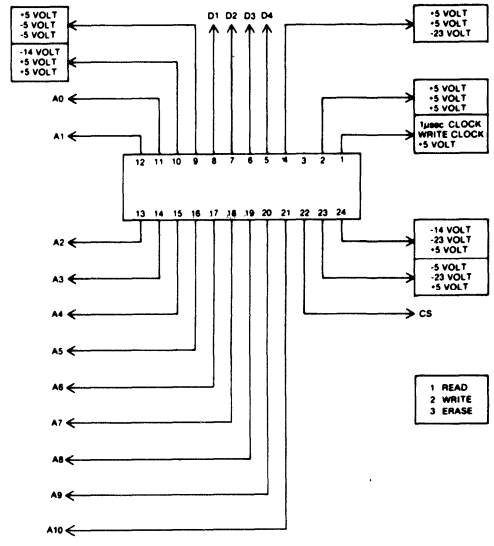
Data Input/Output (D1-D4)
D1 through D4 are bidirectional data terminals Data are entered on these terminals during the write cycle and read out during the read cycle. When deselected, these terminals are in a floating condition.

Write Control ($\overline{W}$)
The write control terminal must be in the low state in order to write data into the device.

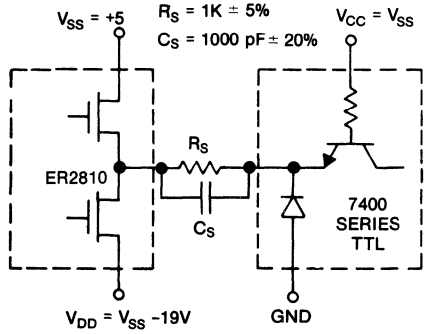
Phase One (ϕ1)
During the write and read operations, pulses must be applied to the ϕ1 terminal to fully shift the memory transistor threshold voltage to its most negative state. This is required for voltage bootstrapping in the row-selection circuitry. The ϕ1 input is high level and not TTL-compatible.

NOTE. All control, address and data inputs are TTL-compatible with pull-up resistors.

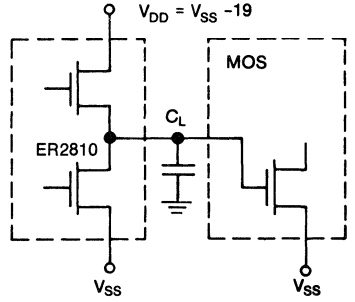
ER2810 OPERATION



TTL INTERFACE



MOS INTERFACE



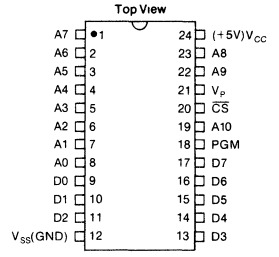
16K N-Channel Electrically Erasable and Programmable ROM

FEATURES

- 2048 word x 8 bit organization, fully decoded
- Electrically Block Erasable with a 1sec., +25V pulse
- Electrically Programmable—1ms per byte
- Single +5V power supply in Read mode
- 300ns Access Time
- 10 year Non-Volatile Data Retention
- Static operation—no clocks
- N-Channel, Silicon gate SNOS technology
- Low Active Power Dissipation. 300mW max.
- Pin for pin compatible with Hitachi HN48016
- Interchangeable with Intel 2716 EPROM

PIN CONFIGURATION

24 pin dual in line



DESCRIPTION

The ER5716 is an Electrically Erasable and Programmable Read Only Memory fabricated in N-Channel, Silicon Gate SNOS technology. Address decoding circuitry is provided on the chip and its operation is fully static, requiring no clocks. +5 volts only is required to perform a Read operation. An additional +25V supply is necessary in the Erase and Write modes.

This device is pin for pin compatible with the Hitachi HN48016 and is also interchangeable with the 2716 family of ultraviolet erasable EPROMs.

Being electrically erasable and programmable, the ER5716 need never be removed from the system for reprogramming since it may be performed, in the circuit, under system or end-user control Also eliminated is the danger of accidental erasure of data by ultraviolet irradiation.

ER5716 VERSUS 2716

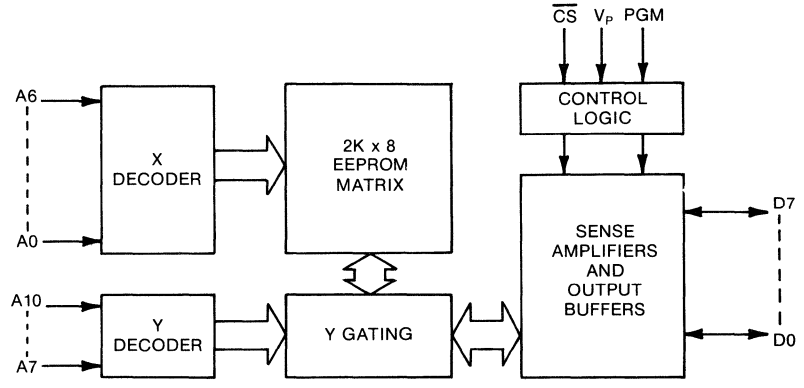
All pins of the two devices are functionally identical with the exception of pins 18 and 20 In order to make the ER5716 electrically alterable, the independent functions of Chip Enable and Output Enable for the 2716 have been combined in the Chip Select ($\overline{CS}$) function of the ER5716, pin 20. Pin 18 retains the Program or Write function, but no longer serves as Chip Enable.

DEVICE OPERATION

V_P (pin 21) requires a d.c supply of +25V in the Erase and Write modes, but remains at +5V for all other operations. Reading may occur with V_P at either level, however continuous operation of the device with V_P at 25V is not recommended.

Writing of data into the memory need not be sequential, it may be performed at any randomly selected byte location. However, writing is possible only after an Erase operation which removes all previously programmed data from the entire memory: individual word erasures are not possible

BLOCK DIAGRAM



MODES OF OPERATION

PGM	$\overline{CS}$	V_P	OPERATING MODE
0	0	+5	READ—Data presented at the output pins a time, t_A after an address change
Don't care	1	+5	STANDBY—Chip deselected, data outputs in the high impedance state
Pulsed 0 to 1	1	+25	SINGLE WORD WRITE—Data at the data inputs is written to the selected address location NOTE that correct writing can occur only if the chip has been previously erased
0	0	+25	PROGRAM VERIFY—Same as Read mode
Pulsed 0 to 1	0	+25	ERASE—All 16,384 bits simultaneously erased to a logic '1' state.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs except V_P (with respect to V_{SS}) .... −0.3V to +7V
V_P (with respect to V_{SS}) ..... −0.3V to +28V
Storage temperature (with Data Retention) ..... −40°C to +85°C
Storage temperature (without Data Retention) ..... −65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{SS} = GND
V_{CC} = +5 ± 5% volts
Programming Voltage, V_P = +25V ± 1V
Operating Temperature range (T_A) = 0°C to +70°C
−40°C to +85°C
−55°C to +125°C

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Unit	Conditions
Input Logic "1"	V_{IH}	2.0	—	V_{CC}+0.3	V	
Input Logic "0"	V_{IL}	−0.3	—	0.8	V	
Input Logic "1" (V_P only)	V_{PH}	V_{CC}−0.6	—	V_{CC}+0.6	V	See Note 1
Output Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 100μA
Output Logic "0"	V_{OL}	V_{SS}	—	0.4	V	I_{OL} = 1.6mA
Input Leakage (except Data)	I_L	—	—	2	μA	V_{IN} = 5.8V
Input Leakage (Data pins)	I_{LD}	—	—	10	μA	V_{IN} = 5.8V
Output Leakage (Data pins)	I_{OD}	—	—	10	μA	V_{OUT} = V_{CC} max
Power Supply Current						
V_P Supply:						
Read mode	I_P	—	4	7	mA	V_P = 6.1V
Write mode	I_P	—	5	10	mA	V_P = 26V
Erase mode	I_P	—	5	10	mA	V_P = 26V
V_{CC} Supply.						
Read mode	I_{CC}	—	32	50	mA	$\overline{CS}$ = V_{IH} or V_{IL}
Write mode	I_{CC}	—	32	50	mA	$\overline{CS}$ = V_{IH} or V_{IL}
Erase mode	I_{CC}	—	32	50	mA	$\overline{CS}$ = V_{IH} or V_{IL}
Power Dissipation						
Read mode	P_{RD}	—	200	318	mW	V_{CC} = 5.5V, V_P = 6.1V
Write mode	P_{WR}	—	306	535	mW	V_{CC} = 5.5V, V_P = 26V
Erase mode	P_{ER}	—	306	535	mW	V_{CC} = 5.5V, V_P = 26V

NOTE: Characteristic data for ER5716IR/HR not available for inclusion at this time. Data available from General Instrument Distributors upon request.

AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Unit	Conditions
Input Capacitance—control inputs	C_I	—	—	7.5	pF	f = 1MHz
Input Capacitance—data inputs	C_D	—	—	15	pF	f = 1MHz
Read Mode Characteristics						
Read Access Time	t_A	—	—	300	ns	
Chip Select to Data Out delay	t_{D1}	—	—	120	ns	Output load 1TTL gate $+C_L = 100pF$
Data hold time	t_{D2}	—	—	100	ns	
Address to Output float time	t_{D3}	10	—	—	ns	
Write Mode Characteristics						
Chip deselect to start of Write	t_{D11}	200	—	—	ns	
Address and Data setup time	t_{D12}	2	—	—	μs	
Data and $\overline{CS}$ hold time	t_{D13}	2	—	—	μs	
Chip Select to Output delay	t_{D14}	—	—	120	ns	See Note 2
Address hold time	t_{D15}	2	—	—	μs	
PGM pulse width	t_{PW}	800	—	—	μs	
PGM pulse rise and fall times	t_r, t_f	5	—	—	ns	
Written state (data I/O)	V_W	—	V_{IL}, V_{OL}	—	V	
Erase Mode Characteristics						
$\overline{CS}$ setup time	t_{D21}	2	—	—	μs	
PGM to Output delay	t_{D22}	2	—	—	μs	
PGM pulse width	t_{PE}	1	—	—	sec	
PGM pulse rise and fall times	t_r, t_f	5	—	—	ns	
Erased state (data I/O)	V_E	—	V_{IH}, V_{OH}	—	V	

NOTES:
1 The wide tolerance of this parameter allows the use of a driver circuit for switching V_P between +5V for reading and +25V in the Erase and Write modes. Although all operations may be performed with +25V applied to the chip, continuous operation is not recommended under these conditions
2. A Read immediately following a Write is not a required operation

NOTE: Characteristic data for ER5716IR/HR not available for inclusion at this time. Data available from General Instrument Distributors upon request

TIMING DIAGRAM

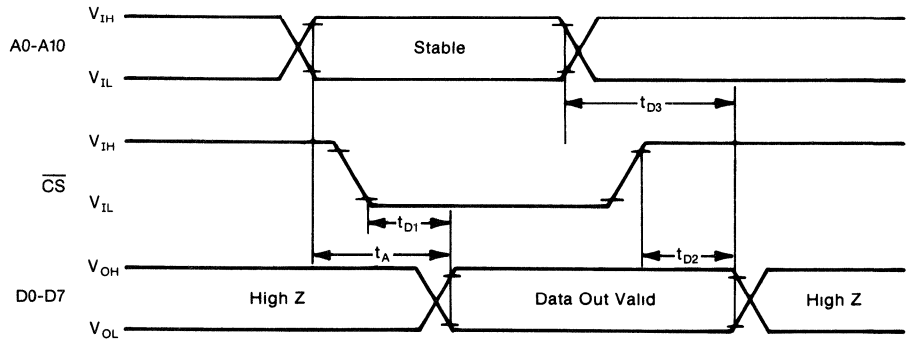


Fig. 1 READ MODE TIMING

TIMING DIAGRAMS

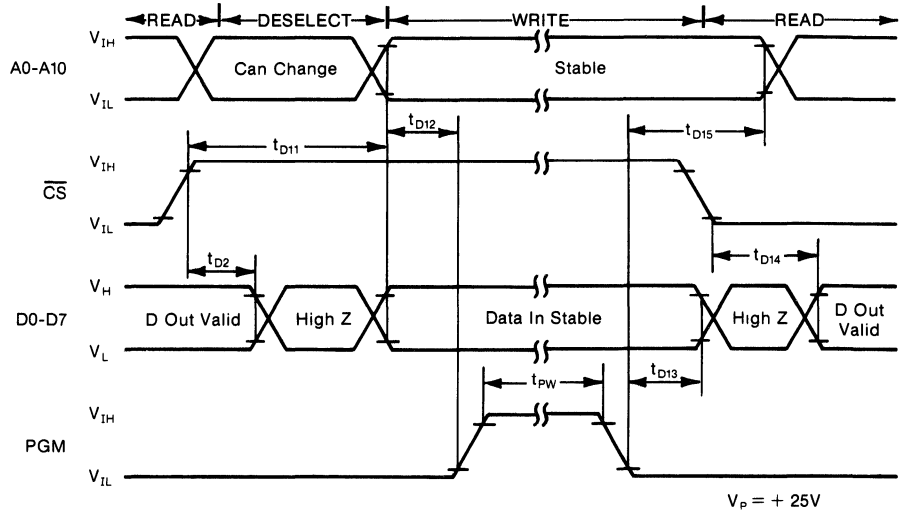


Fig. 2 WRITE MODE TIMING

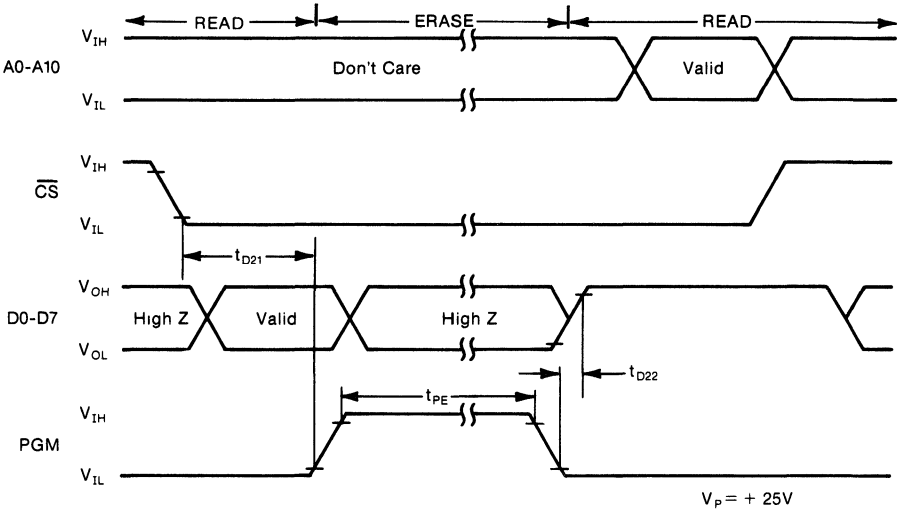


Fig. 3 ERASE MODE TIMING

Word Alterable 16K Bit Electrically Erasable and Programmable ROM

FEATURES

- 5V operation in read mode
- Electrically Word or Block Erasable
- 2048 word x 8 bit organization, fully decoded
- Access time: 300ns maximum
- 10ms Erase and Write times
- Minimum of 10 years' non-volatile data retention
- N-Channel, Sigate, SNOS technology
- Unlimited Read capability
- Conforms to JEDEC byte-wide pinout standards
- Pin for pin compatible with Intel 2816 EEPROM
- Similar pinout to 2716 EPROM

DESCRIPTION

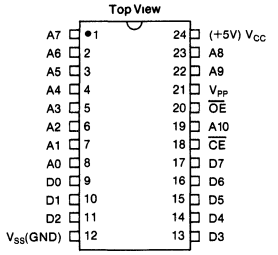
The ER5816 is a high speed electrically word or block erasable and programmable memory fabricated in General Instrument's SNOS technology. Its microprocessor and microcomputer compatible architecture makes it very easy to interface with most popular processors, as does its 300ns maximum access time.

Since the ER5816 is capable of being reprogrammed on a single-byte basis while resident in the operating system, if offers greatly improved system flexibility over previous non-volatile alternatives such as ultraviolet EPROMs. In the case of program storage, software updates may be performed swiftly and easily from a normal system input device such as a keyboard or by downloading from a remote central processing unit via a data link. Where storage of data is necessary, the EEPROM may be programmed under user control from a simple input device as is the case in radio and television tuners, or under the automatic control of the host system, for example in recording system errors or failure modes. The key features of the device, in each case, are non-volatile retention of information, electrical, in-system reprogrammability and reprogrammability on a single-byte basis which does not disturb data stored at adjacent locations. Further system flexibility is afforded by the Block Erase function, which erases all memory bits to the high state in readiness for rapid dumping of data at power loss or when extensive software updates are called for.

The ER5816 conforms to JEDEC byte-wide family standards. It is functionally and pin for pin compatible with the Intel 2816 EEPROM and also pin compatible with the 2716 EPROM. The ER5816, however, does not have special ramping requirements for the V_{PP} supply voltage.

PIN CONFIGURATION

24 PIN DUAL IN LINE



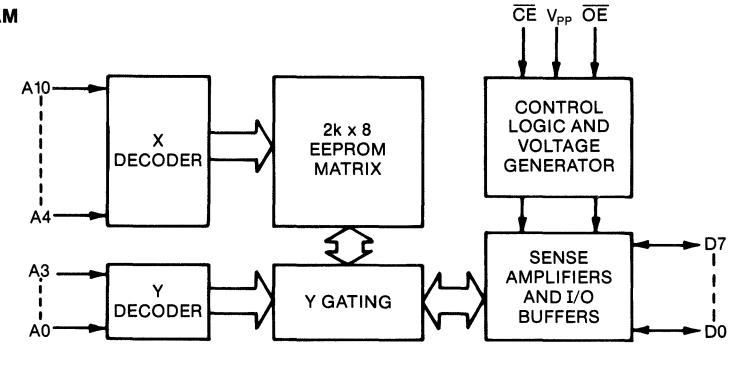
OPERATION

Reading is a ripple-through operation initiated by an address change which results in valid data appearing at the output pins after the normal access time, t_A, provided that both $\overline{CE}$ and $\overline{OE}$ are low. Bus contention problems are minimized by the two-line control provided by CHIP ENABLE ($\overline{CE}$) and OUTPUT ENABLE ($\overline{OE}$) which also makes possible faster access than the normal access time to previously addressed data.

The single-byte Erase and Write operations are the same except that all input data bits must be a logical 1 for a Byte Erase. A Chip Erase is effected in the same way as a Byte Erase with the exception that the $\overline{OE}$ input voltage (V_{OE}) must fall in the range of +8V to +15V. All 16,384 bits are simultaneously erased to a logical high state by a Block Erase. It should be noted that correct writing into memory will only occur if the addressed location has been preconditioned into the erased state by either a Byte or a Block Erase. Preconditioning may occur at any time prior to writing.

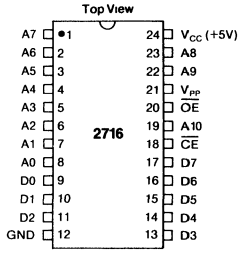
The specification of 10 years non-volatile data retention after a minimum of 10^4 reprogramming cycles is merely one point on the curve of retention versus reprogramming cycles and does not imply a sudden cut-off or end of life. As the number of Erase/Write cycles per address increases, a gradual, logarithmic reduction in data retention capability occurs with 1 year of retention being a typical figure after 10^5 cycles.

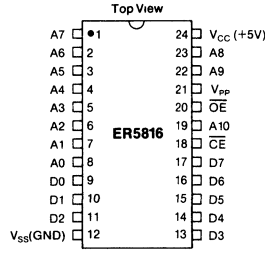
BLOCK DIAGRAM



PIN CONFIGURATION

DEVICE	2716				ER5816			
MODE \ PIN	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	I/O	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	I/O
READ	V_{IL}	V_{IL}	+5	D_{OUT}	V_{IL}	V_{IL}	+4 to +6	D_{OUT}
BYTE ERASE	—	—	—	—	V_{IL}	V_{IH}	+21	V_{IH}
BYTE WRITE	Pulsed	V_{IH}	+25	D_{IN}	V_{IL}	V_{IH}	+21	D_{IN}
CHIP ERASE		ULTRAVIOLET			V_{IL}	+8 to +15	+21	V_{IH}
STANDBY	V_{IH}	Don't Care	+5	High-Z	V_{IH}	Don't Care	+4 to +6	High-Z
PROGRAM INHIBIT	V_{IL}	V_{IH}	+25	High-Z	V_{IH}	Don't Care		High-Z





MODES OF OPERATION

$\overline{CE}$	$\overline{OE}$	V_{PP}	D0-D7	OPERATING MODE	
0	0	+4 to +6	D_{OUT}	READ	— Data stored at the addressed location appears at the output pins a time, t_A after an address change.
0	1	+21	$D_{IN} = 1$	BYTE ERASE	— Only the selected word is erased to the '1' state.
0	1	+21	D_{IN}	BYTE WRITE	— Data at the data inputs is written into the selected location. Note that correct writing may only occur if the location has been previously erased
0	+8 to +15	+21	$D_{IN} = 1$	BLOCK ERASE	— The entire contents of memory is erased to the '1' state.
1	Don't Care		High-Z	CHIP DESELECTED	

PIN FUNCTIONS

NAME	FUNCTION
A0-A10	11-Bit Word Address
D0-D7	Data input and output ports — high impedance in deselected mode.
V_{CC}	Power supply input Normally +5 ± 10% volts.
V_{SS}	Supply pin Normally at ground potential
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input.
V_{PP}	High Voltage power supply for erasing and writing In read mode, the +4 to +6 volt tolerance for the input voltage on this pin allows the use of voltage multiplier for generating the +21V programming voltage

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to Ground except pins 20 and 21 ..... +6V to −0.3V
Input voltage, pins 20 and 21 with respect to Ground ....+24V to −0.3V
Storage Temperature (unpowered and without data retention) ..... −65°C to +150°C
Soldering Temperature of Leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{SS} = GND
V_{CC} = +5 ±5% volts
Operating Temperature Ranges (T_A): 0°C to +70°C
−40°C to +85°C
−55°C to +125°C

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Logic "1" (except pins 20 and 21)	V_{IH}	2 0	—	V_{CC}+0.3	V	
Input Logic "0"	V_{IL}	−0.1	—	+0 8	V	
Output Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = −400μA
Output Logic "0"	V_{OL}	V_{SS}	—	0.45	V	I_{OL} = 2.1mA
Input Leakage Current	I_{IL}	—	—	10	μA	V_{IN} = 5.25V
Power Supply Requirements						
V_{PP} Read Voltage	V_{PP}	4	5	6	V	See Note 1
V_{PP} Erase/Write Voltage	V_{PP}	20	21	22	V	
Chip Erase Voltage	V_{OE}	8	—	15	V	$I_{\overline{OE}}$ = 10μA
V_{CC} Supply:						
Chip Selected	I_{CC}	—	40	90	mA	
Chip Deselected	I_{CC}	—	15	25	mA	
V_{PP} Supply:						
Read Mode	I_{PP}	—	—	5	mA	V_{PP} = 6V
Erase/Write/Block Erase Mode	I_{PP}	—	—	15	mA	V_{PP} = 21V, $\overline{CE}$ = V_{IL}
Program Inhibit Mode	I_{PP}	—	—	5	mA	V_{PP} = 21V, $\overline{CE}$ = V_{IH}
Power Dissipation.						
Chip Selected	P_D	—	200	450	mW	
Chip Deselected	P_D	—	75	125	mW	

NOTE:
1 V_{PP} minimum in Read mode not to exceed V_{CC} −0.6.

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input capacitance	C_I	—	4	6	pF	V_{IN} = 0V
Output capacitance	C_O	—	—	10	pF	V_{OUT} = 0V
Read Mode						All AC Test conditions:
Access time — Address to output delay	t_A	—	—	300	ns	Output load: 1TTL gate + C_L = 100pF
CE to output delay	t_{CE}	—	—	350	ns	
OE to output delay	t_{OE}	10	—	120	ns	Input pulse levels: 0.5V to 2.2V
Data hold time	t_{DH}	—	—	100	ns	
Byte Erase/Write Mode						
Address, $\overline{CE}$ and $\overline{OE}$ setup time	t_{CS}	150	—	—	ns	
Data setup time	t_{DS}	0	—	—	ns	
Address, data, $\overline{CE}$ and $\overline{OE}$ hold time	t_{CH}	50	—	—	μs	
V_{PP} Rise and Fall time	t_R, t_F	0 01	—	100	μs	
Erase time	t_E	9	10	15	ms	
Write time	t_W	9	10	15	ms	
Block Erase Mode						
CE setup time	t_{CS}	150	—	—	ns	
CE hold time	t_{CH}	50	—	—	μs	
V_{PP} Rise and Fall time	t_R, t_F	0.01	—	· 100	μs	
$\overline{OE}$ to V_{PP} set up time	t_{OS}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OH}	0	—	—	ns	
Block erase time	t_{BE}	9	10	15	ms	

MEMORY CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Erase time — byte or block	t_E	9	10	15	ms	
Erased state	V_E	—	V_{IH}, V_{OH}	—	V	
Write time	t_W	9	10	15	ms	
Written state	V_W	—	V_{IL}, V_{OL}	—	V	
Data retention time (powered or unpowered)	t_S	10	—	—	Yrs	
Number of Erase/Write cycles per byte	N_{EW}	10^4	—	—	—	See Note 1
Number of Read accesses between refresh	N_{RA}	—	—	—	—	Unlimited

NOTE
1 Does not imply end of useful life See "Operation" for further explanation.

TIMING DIAGRAMS

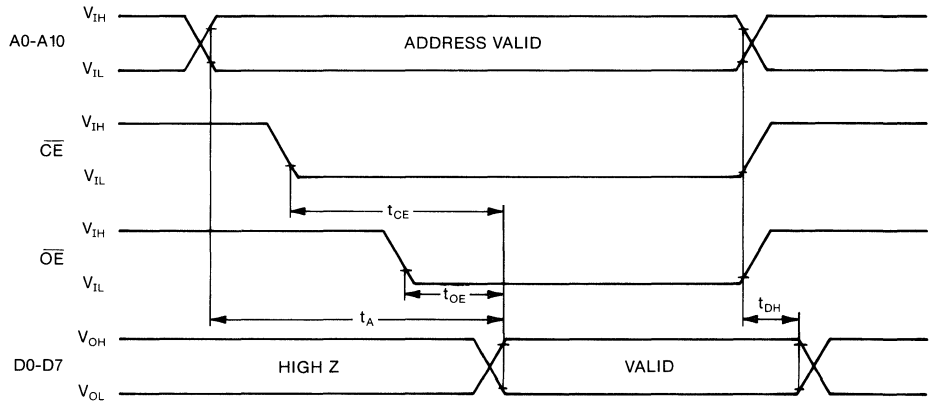


Fig. 1 READ MODE TIMING

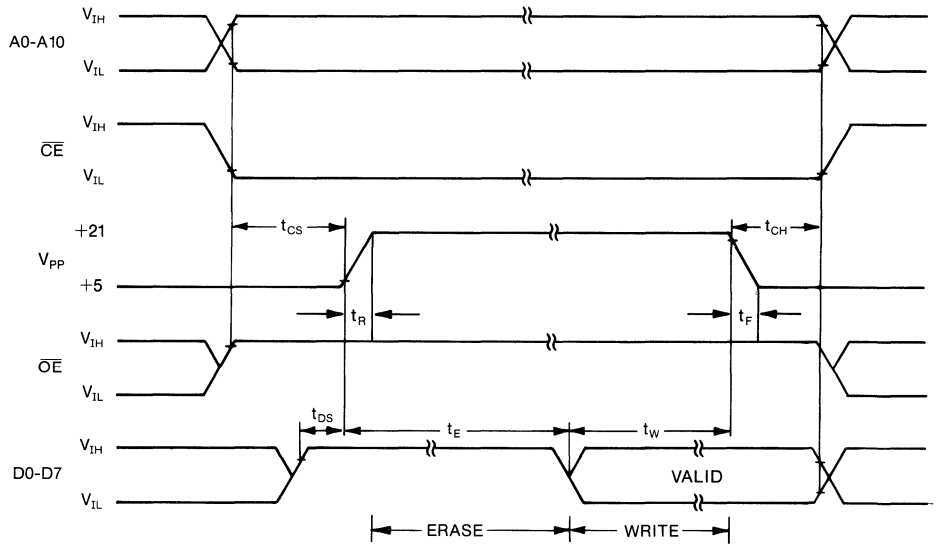


Fig. 2 BYTE ERASE AND WRITE TIMING

TIMING DIAGRAM

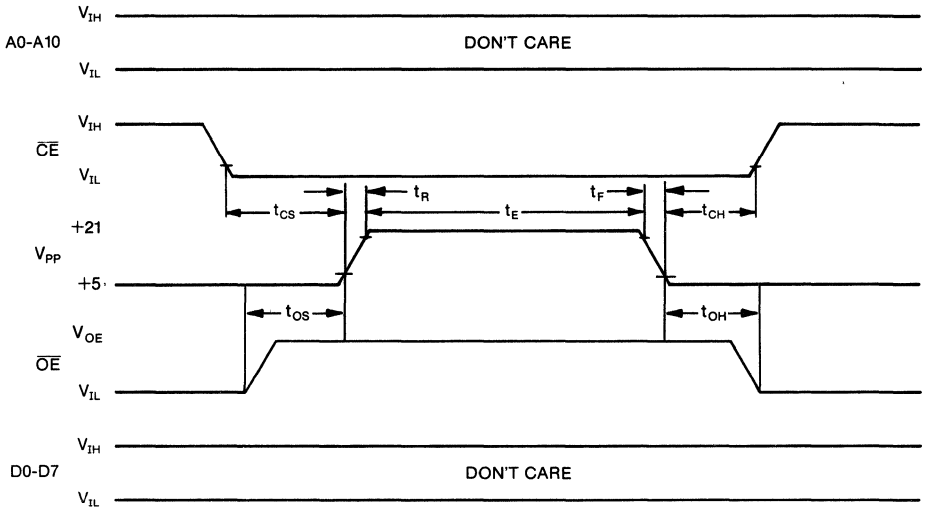


Fig. 3 BLOCK ERASE TIMING

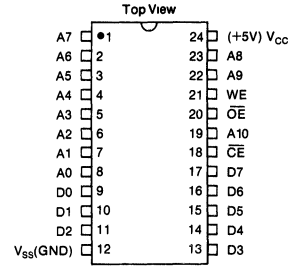
Word Alterable 16K Bit Electrically Erasable and Programmable ROM

FEATURES

- No high voltages – +5V only operation in all modes
- Electrically Word or Block Erasable
- 2048 word x 8 bit organization, fully decoded
- Access time: 300ns maximum
- 20ms Erase and Write times
- Minimum of 10 years' non-volatile data retention
- N-Channel, Si-Gate SNOS technology
- Unlimited Read capability
- Conforms to JEDEC byte-wide pinout standards
- Functionally equivalent to Intel 2816 EEPROM
- Similar pinout to 2716 EPROM

PIN CONFIGURATION

24 PIN DUAL IN LINE



DESCRIPTION

The ER5916 is a high speed electrically word or block erasable and programmable memory fabricated in General Instrument's SNOS technology. Its microprocessor and microcomputer compatible architecture makes it very easy to interface with most popular processors, as does its 300ns maximum access time.

Making it even more attractive to the system design engineer is its +5V only operation in all modes; no high voltages are required for erasing and writing. The ER5916, therefore, offers increased flexibility and opportunities for innovation in new designs since a large amount of data can now be stored in a non-volatile medium and selected portions of it altered with great ease during normal system operation.

This device conforms to JEDEC byte-wide family standards and is functionally compatible with the ER5816 and the Intel 2816 EEPROM. Some differences of pin functions and control logic levels are necessary due to the ER5916's 5V only operation. Refer to the comparison of these two devices included in this data sheet.

Bus contention problems are minimized by the two-line control provided by CHIP ENABLE ($\overline{CE}$) and OUTPUT ENABLE ($\overline{OE}$). Programming operations are controlled by one TTL level input, WRITE ENABLE (WE).

OPERATION

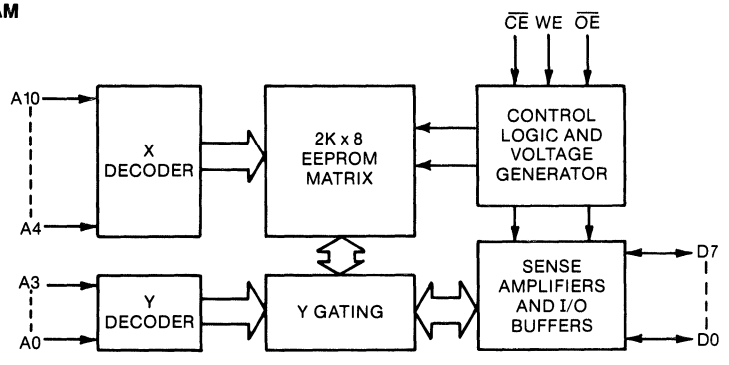
Reading is a ripple-through operation initiated by an address change. If both $\overline{CE}$ and $\overline{OE}$ are low, data appears at the outputs after the normal access time, T_A has elapsed. $\overline{OE}$, when held high, disables the outputs and allows fast access to data when pulsed low.

Erasing and writing of one byte are essentially the same except that all input data bits must be held high for an erase operation.

A chip erase mode is also provided for applications such as program storage in which software updates are made at infrequent intervals. In this mode, all locations are erased into the '1' state with the same, 20ms pulse as required for a single byte erase.

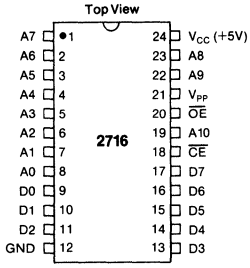
There is a trade-off to be made between the data retention time and the number of Erase/Write cycles performed per location. A gradual, logarithmic reduction in retention time is experienced as the number of Erase/Write cycles increases. The specified limit is merely one point on this curve and does not imply a sudden cut-off or end of life. After 10^5 cycles a typical retention time is 1 year.

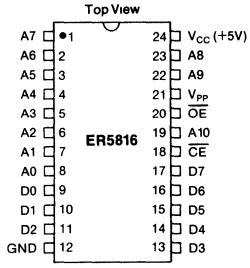
BLOCK DIAGRAM

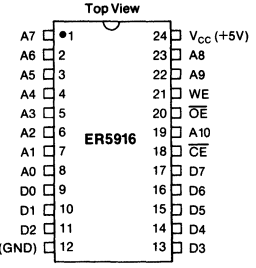


PIN CONFIGURATION

DEVICE	2716				ER5816				ER5916			
MODE \ PIN	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	I/O	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	I/O	$\overline{CE}$ (18)	$\overline{OE}$ (20)	WE (21)	I/O
READ	V_{IL}	V_{IL}	+5	D_{OUT}	V_{IL}	V_{IL}	+4 to +6	D_{OUT}	V_{IL}	V_{IL}	V_{IL}	D_{OUT}
BYTE ERASE	—	—	—	—	V_{IL}	V_{IH}	+21	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IH}
BYTE WRITE	Pulsed	V_{IH}	+25	D_{IN}	V_{IL}	V_{IH}	+21	D_{IN}	V_{IL}	V_{IH}	V_{IH}	D_{IN}
CHIP ERASE		ULTRAVIOLET			V_{IL}	+8 to +15	+21	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Don't Care
STANDBY	V_{IH}	Don't Care	+5	High-Z	V_{IH}	Don't Care	+4 to +6	High-Z	V_{IH}	Don't Care		High-Z
PROGRAM INHIBIT	V_{IL}	V_{IH}	+25	High-Z	V_{IH}	Don't Care		High-Z	V_{IH}	Don't Care		High-Z







MODES OF OPERATION

$\overline{CE}$	$\overline{OE}$	WE	D0-D7	OPERATING MODE	
0	0	0	D_{OUT}	READ	— Data stored at the addressed location appears at the output pins a time, t_A after an address change.
0	1	1	$D_{IN} = 1$	BYTE ERASE	— Only the selected word is erased to the '1' state
0	1	1	D_{IN}	BYTE WRITE	— Data at the data inputs is written into the selected location. Note that correct writing may only occur if the location has been previously erased.
0	0	1	Don't Care	BLOCK ERASE	— The entire contents of memory is erased to the '1' state
1	Don't Care		High-Z	CHIP DESELECTED	

PIN FUNCTIONS

NAME	FUNCTION
A0-A10	11-Bit Word Address
D0-D7	Data input and output ports — high impedance in deselected mode
V_{CC}	Power supply input. Normally +5 ± 10% volts.
V_{SS}	Supply pin. Normally at ground potential.
$\overline{CE}$	Chip enable input.
$\overline{OE}$	Output enable input
WE	Write enable input

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to Ground except pins 20 and 21 ..... +6V to −0 3V
Input voltage, pins 20 and 21 with respect to Ground ..... +24V to −0.3V
Storage Temperature (unpowered and without data retention) ..... −65°C to +150°C
Soldering Temperature of Leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{SS} = GND
V_{CC} = +5 ±5% volts
Operating Temperature Ranges (T_A): 0° C to +70° C
−40° C to +85° C
−55° C to +125° C

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Input Logic "1" (except pins 20 and 21)	V_{IH}	2.0	—	V_{CC}+0.3	V	
Input Logic "1" (pins 20 and 21)	V_{IC}	2.0	—	+ 22	V	
Input Logic "0"	V_{IL}	−0.1	—	+ 0.8	V	
Output Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = −400μA
Output Logic "0"	V_{OL}	V_{SS}	—	0.4	V	I_{OL} = 2.1mA
Input Leakage Current	I_{IL}	—	—	10	μA	V_{IN} = 5.25V
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	—	40	90	mA	
Chip Deselected	I_{CC}	—	15	25	mA	
Power Dissipation:						
Chip Selected	P_D	—	200	450	mW	
Chip Deselected	P_D	—	75	125	mW	

NOTE 1: (T_A) = −40 to +85°C V_{CC} = +5 ±5%, unless otherwise specified.

AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Input capacitance	C_I	—	4	6	pF	V_{IN} = 0V
Output capacitance	C_O	—	—	10	pF	V_{OUT} = 0V
Read Mode						All AC Test conditions:
Access time — Address to output delay	t_A	—	—	300	ns	Output load: 1TTL gate + C_L = 100pF
CE to output delay	t_{CE}	—	—	350	ns	
OE to output delay	t_{OE}	10	—	120	ns	Input pulse levels: 0.5V to 2.2V
Data hold time	t_{DH}	—	—	100	ns	
Byte Erase/Write Mode						
Address, $\overline{CE}$ and $\overline{OE}$ setup time	t_{CS}	200	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Address, data, $\overline{CE}$ and $\overline{OE}$ hold time	t_{CH}	2	—	—	μs	
Erase time	t_E	20	25	30	ms	
Write time	t_W	20	25	30	ms	
Block Erase Mode						
CE setup time	t_{CS}	200	—	—	ns	
CE hold time	t_{CH}	2	—	—	μs	
Block erase time	t_{BE}	20	25	30	ms	

MEMORY CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Erase time — byte or block	t_E	20	25	30	ms	
Erased state	V_E	—	V_{IH}, V_{OH}	—	—	
Write time	t_W	20	25	30	ms	
Written state	V_W	—	V_{IL}, V_{OL}	—	—	
Data retention time (powered or unpowered)	t_S	10	—	—	Yrs	
Number of Erase/Write cycles per byte	N_{EW}	10^4	—	—	—	See Note 1
Number of Read accesses between refresh	N_{RA}	—	—	—	—	Unlimited

NOTE.
1 Does not imply end of useful life. See "Operation" for further explanation.

ELEC. ALTERABLE NON-VOLATILE MEMORY

TIMING DIAGRAMS

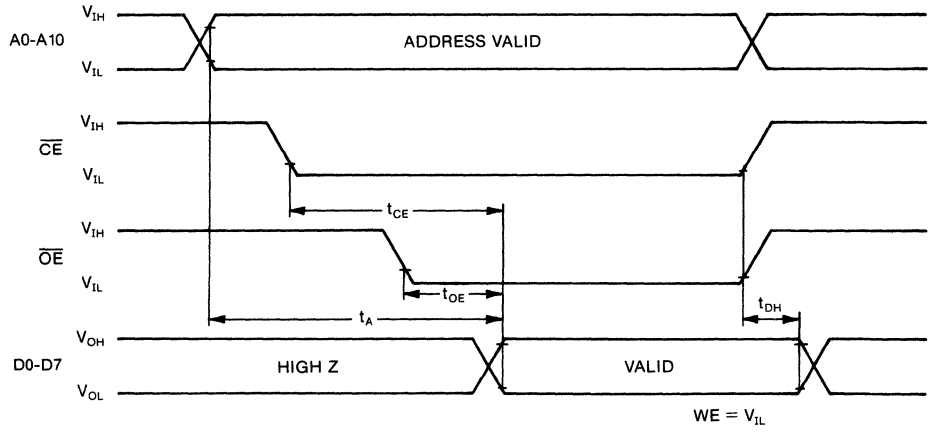


Fig. 1 READ MODE TIMING

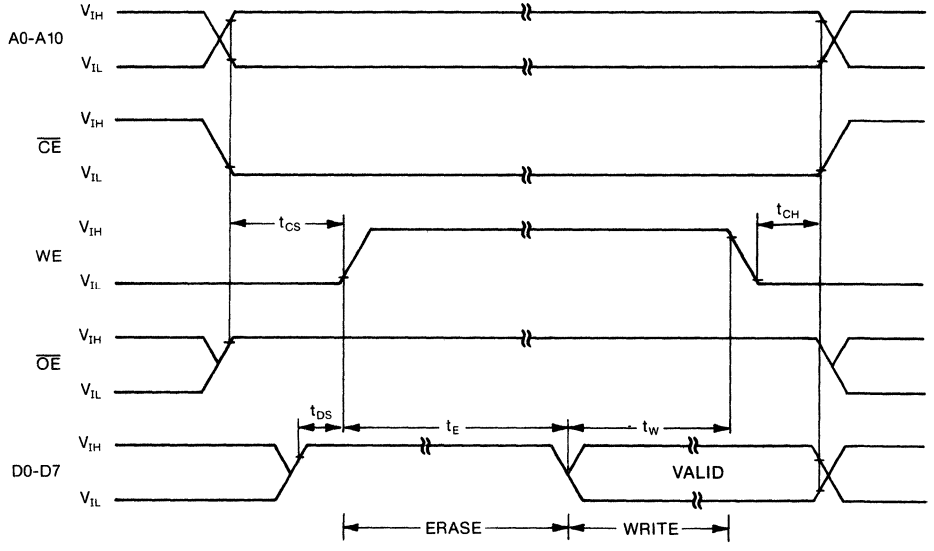


Fig. 2 BYTE ERASE AND WRITE TIMING

TIMING DIAGRAM

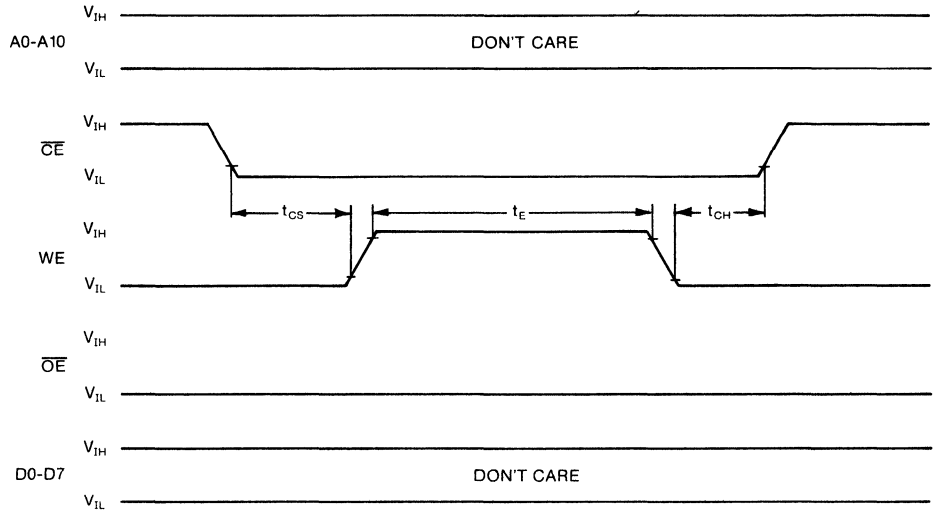


Fig. 3 BLOCK ERASE TIMING

GENERAL INSTRUMENT

Non-Volatile Static RAM

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
4K N-CHANNEL NON-VOLATILE STATIC RAM	4K bits organized 512 x 8	ER5304	3-48

4K N-CHANNEL NON-VOLATILE STATIC RAM

FEATURES

- 512 x 8 bit organization, fully decoded RAM overlaid bit for bit with non-volatile EEPROM
- Single +5V power supply
- 300ns RAM cycle time
- TTL compatible
- Data can be recalled an unlimited number of times
- 10^4 store cycles with 10 year data retention
- Power failure protection

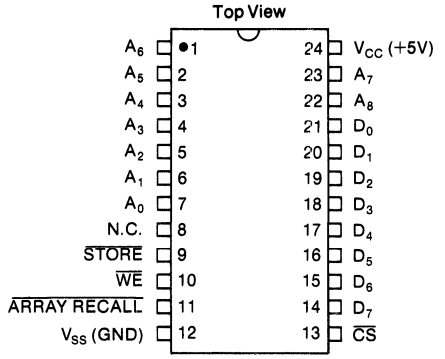
DESCRIPTION

The ER5304 is a high speed non-volatile Si-Gate RAM. The device contains 4K bits of memory organized as a conventional 4K static RAM overlaid bit-for-bit with a non-volatile 4K Electrically Erasable ROM (EEPROM). The device can be used as a conventional static RAM while the non-volatile data stored in the EEPROM remains unaffected. Non-volatile data can be transferred back and forth between the RAM and the EEPROM by simple STORE and ARRAY RECALL signals. During the lifetime of the device, data can be recalled from the EEPROM an unlimited number of times.

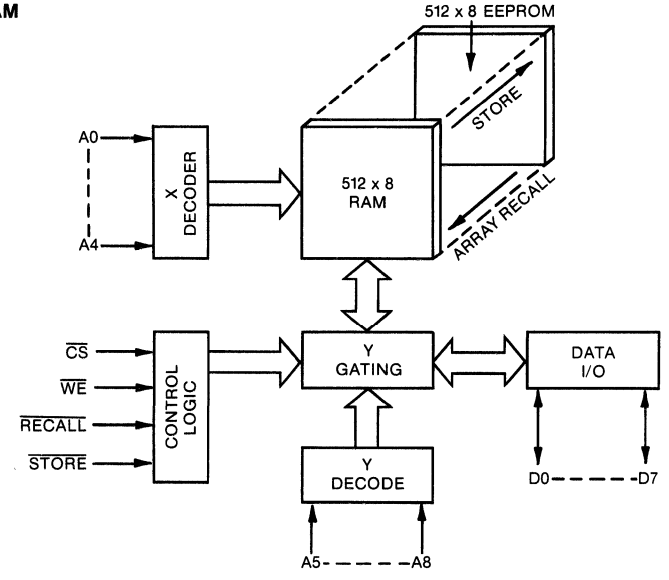
A single 5V supply is the only power source ever required for any function. High voltage pulses or supplies are never required. All inputs and outputs are TTL compatible with Tri-state outputs. The device cycle time for both read and write is 300ns.

The device is capable of protecting against data loss due to a power failure. One simple TTL signal saves the entire RAM contents. A non-volatile copy of all RAM data is internally stored in the EEPROM and can be recalled to the RAM when power returns. No battery backup is required.

PIN CONFIGURATION
24 PIN DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Inputs and Outputs with Respect to Ground ..... −0.3 to +7V
Storage Temperature (without Data Retention) ..... −65°C to +150°C
Storage Temperature (with Data Retention) ..... −40°C to +85°C
Soldering Temperature of Leads (10 seconds) ..... +300°C

Standard Conditions (unless otherwise stated):

V_{SS} = GND
V_{CC} = 5 ± 5% Volts
Operating Temperature T_A = −40°C to +85°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Max	Units	Conditions
Power Supply Current	I_{CC}	—	60	mA	All Inputs = 5.25V D_{OUT} Open T_A = 0°C
Output Leakage Current	I_{LO}	−1.0	+1.0	μA	V_{OUT} = GND to V_{CC}
Input Low Voltage	V_{IL}	−.3	.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC}	V	
Output Low Voltage	V_{OL}	—	.4	V	I_{OL} = 2.0mA
Output High Voltage	V_{OH}	2.4	—	V	I_{OH} = 1mA

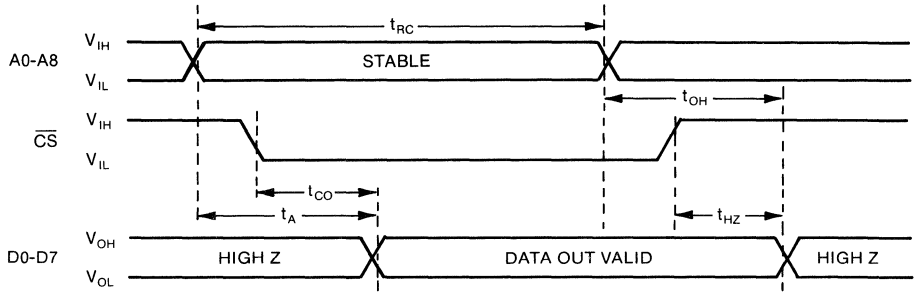
PIN FUNCTIONS

NAME	FUNCTION
A0-A8	Address Lines
D0-D7	Data I/O
CS	Chip Select
$\overline{WE}$	Write Enable
$\overline{ARRAY\ RECALL}$	Transfers Data stored in EEPROM back to RAM
$\overline{STORE}$	Transfers Data from RAM into Non-Volatile EEPROM
V_{CC}	+5 Volts
GND	Ground

MODE \ PINS	$\overline{CS}$ (13)	$\overline{WE}$ (10)	$\overline{STORE}$ (9)	$\overline{ARRAY\ RECALL}$ (11)	DATA I/O (14-21)
Deselected (See Notes 1 & 2)	1	Don't Care			High Z
RAM Write	0	0	1	1	Data In
RAM Read	0	1	1	1	Data Out
EEPROM Store (See Note 2)	0	1	0	1	High Z
EEPROM Recall	0	1	1	0	High Z

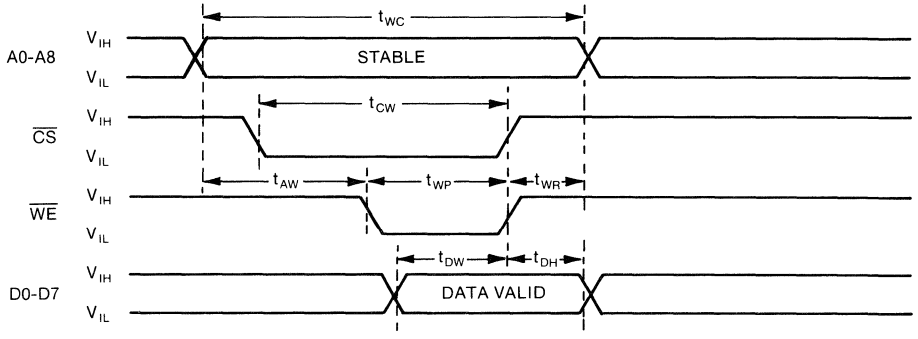
NOTES:
1. Chip is deselected but may be automatically completing a store cycle.
2. $\overline{CS}$ and $\overline{STORE}$ must be low only to initiate a store cycle, after which the cycle will continue to completion automatically ($\overline{CS}$, $\overline{STORE}$ = X).

READ CYCLE



Characteristics	Sym	Min	Typ	Max	Units	Conditions
Read Cycle Time	t_{RC}	300	—	—	ns	
Access Time	t_A	—	—	300	ns	
Chip Select to Output Valid	t_{CO}	—	—	200	ns	
Output Hold from Address Change	t_{OH}	50	—	—	ns	
Chip Deselect to Output in High Z	t_{HZ}	10	—	100	ns	

WRITE CYCLE



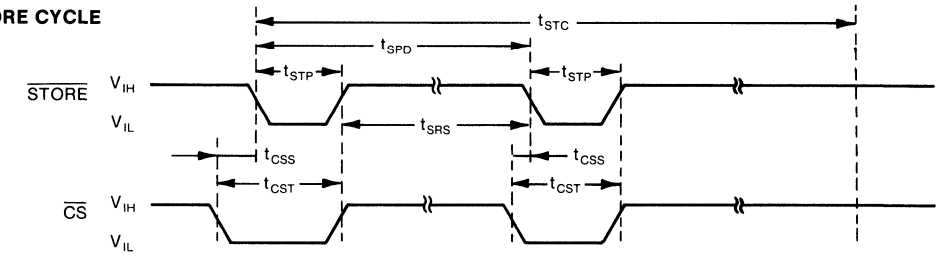
Parameter	Sym	Min	Typ	Max	Units	Conditions
Write Cycle Time	t_{WC}	300	—	—	ns	
Chip Select to End of Write	t_{CW}	150	—	—	ns	
Address to Write Set-up Time	t_{AW}	50	—	—	ns	
Write Pulse Width	t_{WP}	100	—	—	ns	
Write Recovery Time	t_{WR}	25	—	—	ns	
Data Valid to End of Write	t_{OW}	100	—	—	ns	
Data Hold Time	T_{OH}	20	—	—	ns	

In read and Write modes the device operates as a conventional static RAM The device is selected with a logic "0" level applied to the $\overline{CS}$ pin A logic "1" input on $\overline{WE}$ selects the Read mode, a logic "0" selects the Write mode Address lines must remain stable for the duration of the Read or Write cycle Data outputs are in the high impedance state whenever the Device is deselected or during a store or Array Recall Cycle

A Store Cycle is initiated by applying two logic "0" level pulses to the $\overline{\text{STORE}}$ pin of a selected device This causes all 4096 bits of data in the EEPROM to be modified to an exact copy of the current RAM data. The original data in the RAM remains valid. The $\overline{\text{WE}}$ and $\overline{\text{ARRAY RECALL}}$ inputs are inhibited during the store operation and the data outputs are Tri-stated. The inhibited inputs will be enabled upon completion of the Store Operation if the $\overline{\text{STORE}}$ input is high. Data stored in the EEPROM remains valid with or without power supplied to the ER5304.

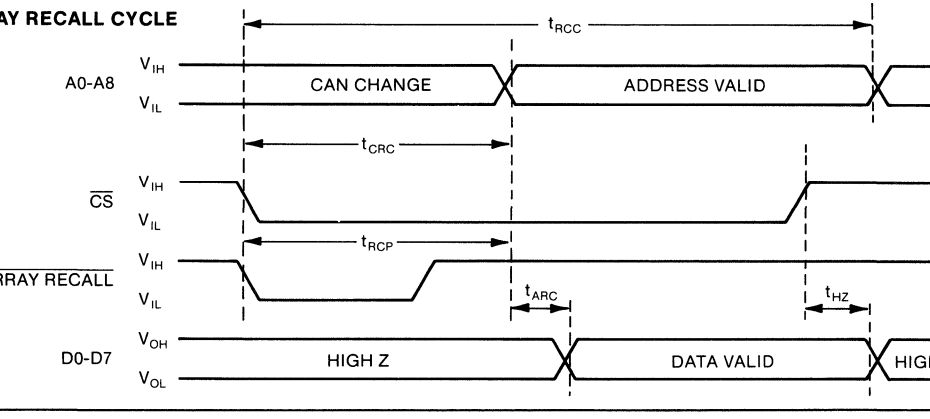
To prevent an unintentional Store Cycle during power-up or power-down either the $\overline{\text{STORE}}$ or $\overline{\text{CS}}$ input should be kept high by tying the input to V_{CC} through a pull up resistor.

STORE CYCLE



Characteristics	Sym	Min	Typ	Max	Units	Conditions
Store Cycle Time (t_{SPD} = 5ms)	t_{STC}	—	—	10	ms	
Store Pulse Width	t_{STP}	100	—	—	ns	
Chip Select to End of Store	t_{CST}	125	—	—	ns	
Chip Select to Store Set-up Time	t_{CSS}	25	—	—	ns	
Store Second Pulse Delay Time	t_{SPD}	5	—	—	ms	
Store Reset Time	t_{SRS}	300	—	—	ns	

ARRAY RECALL CYCLE



Characteristics	Sym	Min	Typ	Max	Units	Conditions
Array Recall Cycle Time	t_{RCC}	1500	1000	—	ns	
Chip Select to End of Recall	t_{CRC}	750	—	—	ns	
Recall Pulse Width	t_{RCP}	750	—	—	ns	
Chip Deselect to Output in High Z	t_{HZ}	10	—	100	ns	
Recalled Data Access Time from End of Recall	t_{ARC}	—	—	600	ns	

The Array Recall Cycle reads the non-volatile data stored in the EEPROM and copies it back into the RAM. A logic "0" on the $\overline{\text{ARRAY RECALL}}$ input of a selected device will initiate a cycle that in a single operation will overwrite all 4096 bits of data in the RAM with the data from the EEPROM The data in the EEPROM remains unaltered. Once the EEPROM data is back in the RAM it can be accessed by normal RAM Read or Write cycles.

Data that has been stored properly in the non-volatile EEPROM of the ER5304 may be recalled an unlimited number of times during the lifetime of the device.

NOTES

Microcomputer 4

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			PIC Series
8 BIT MICROCOMPUTER	The PIC1650 series of microcomputers contain RAM I/O and a central processing unit as well as a customer defined ROM to specify overall functional characteristics of the device.	PIC1650A	4-4
		PIC1650XT	4-16
		PIC1654	4-28
		PIC1655A	4-38
		PIC1655XT	4-50
		PIC16C55	4-62
		PIC1656	4-72
		PIC1670	4-85
			PIC Development Series
8 BIT DEVELOPMENT MICROCOMPUTER	PIC microcomputer without ROM and with addition of a HALT pin.	PIC1664	4-96
		PIC16C63	4-110
		PIC1665	4-121
			PICAL/PICES II
PIC ASSEMBLER	Converts symbolic source programs for PIC series into object code.	PICAL	4-132
PIC DEVELOPMENT SYSTEM	In-circuit emulation and debug system—stand alone or peripheral.	PICES II	4-134
			PIC Field Demo Systems
PIC FIELD DEMO SYSTEMS	Contains PIC microcomputer, PROMs and provisions for on-board RC oscillator or external clock.	PFD Systems	4-138

PIC Series

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
8 BIT MICROCOMPUTER	The PIC1650 series of microcomputers contain RAM I/O and a central processing unit as well as a customer defined ROM to specify overall functional characteristics of the device.	PIC1650A	4-4
		PIC1650XT	4-16
		PIC1654	4-28
		PIC1655A	4-38
		PIC1655XT	4-50
		PIC16C55	4-62
		PIC1656	4-72
		PIC1670	4-85

8 Bit Microcomputer

FEATURES

- User programmable
- Intelligent controller for stand-alone applications
- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Self-contained oscillator
- Access to RAM registers inherent in instruction
- Wide power supply operating range (4.5V to 7.0V)
- Available in two temperature ranges: 0° to 70° C and −40° to 85° C
- 4 sets of 8 user defined TTL-compatible Input/Output lines
- 2 level stack for subroutine nesting

DESCRIPTION

The PIC1650A microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

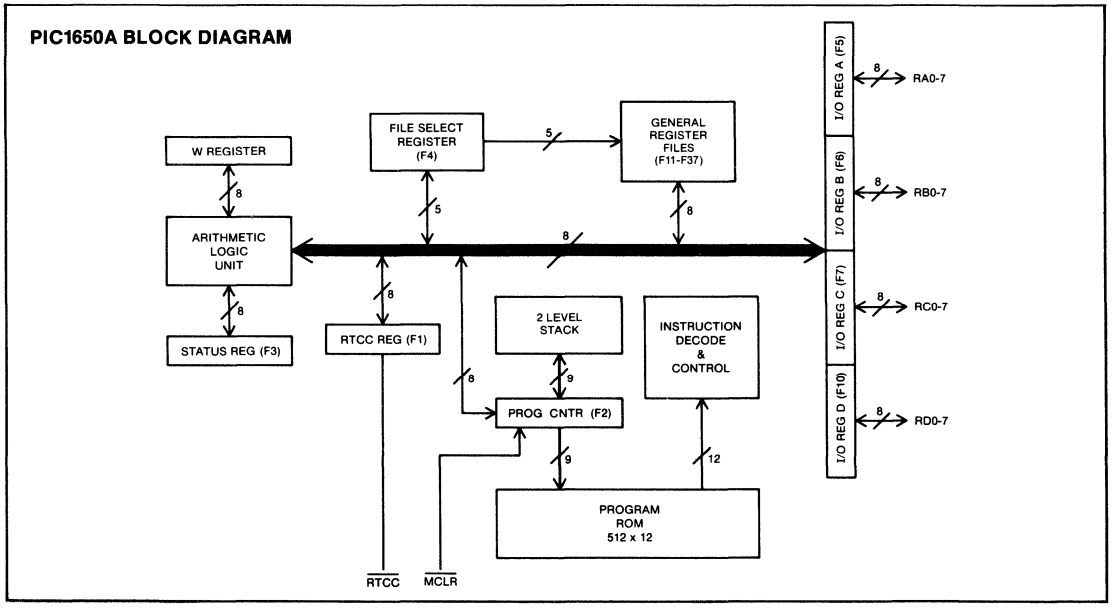
The PIC1650A is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency Inputs and outputs are TTL-compatible

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1664. The PIC1664 is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands The PFD1000 Field Demo System is available containing a PIC1664 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

MICROCOMPUTER

PIC1650A BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus· the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width The Register File is divided into two functional groups operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers The general purpose registers are used for data and control information under command of the instructions

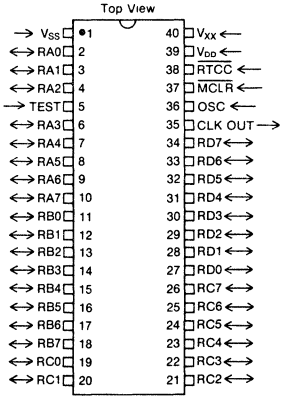
The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register

The Program ROM contains the operational program for the rest of the logic within the controller Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting Activating the $\overline{MCLR}$ input on power up initializes the ROM program to address 777_8

PIN FUNCTIONS

Signal	Function
OSC (input)	Oscillator input This signal can be driven by an external oscillator if a precise frequency of operation is required or an external RC network can be used to set the frequency of operation of the internal clock generator. This is a Schmitt trigger input.
$\overline{RTCC}$ (input)	Real Time Clock Counter Used by the microprogram to keep track of elapsed time between events The RTCC register increments on falling edges applied to this pin. This register can be loaded and read by the program This is a Schmitt trigger input.
RA0-7, RB0-7, RC0-7, RD0-7 (input/output)	User programmable input/output lines These lines can be inputs and/or outputs and are under direct control of the program.
$\overline{MCLR}$ (input)	Master Clear Used to initialize the internal ROM program to address 777_8 and latch all I/O register high Should be held low at least 1-10ms past the time when the power supply is valid for the oscillator to start up This is a Schmitt trigger input.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation
V_{DD}	Primary power supply
V_{XX}	Output Buffer power. Used to enhance output current sinking capability.
V_{SS}	Ground

PIN CONFIGURATION
40 LEAD DUAL IN LINE



MICROCOMPUTER

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$. However, if data are being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits: 3-7 These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	I/O Register A (A0-A7)
F6	I/O Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10	I/O Register D (D0-D7)
F11-F37	General Purpose Registers

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

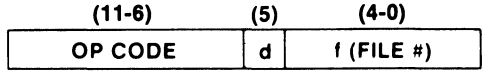
For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS



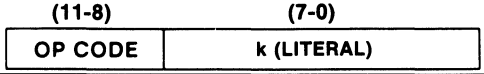
For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇋f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

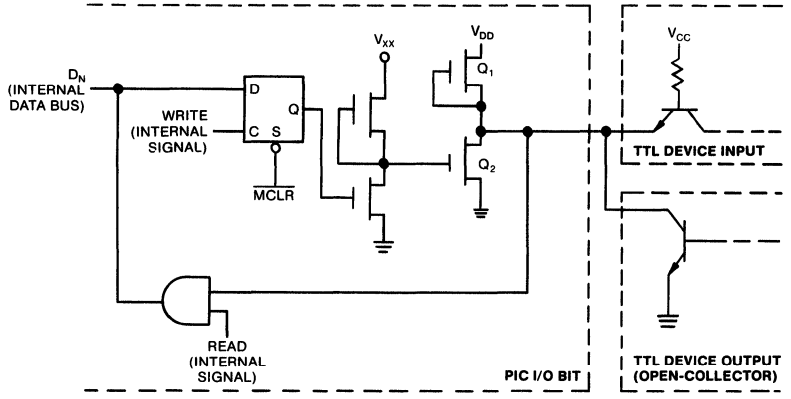
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 0†0 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

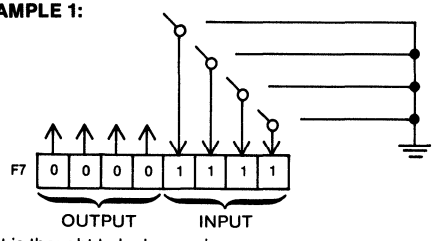
Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions.

As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



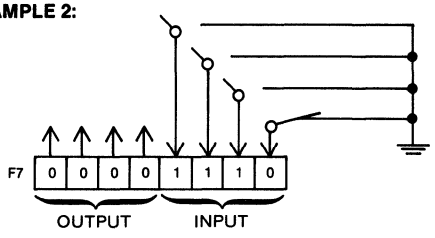
What is thought to be happening:

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any pin with Respect to V_{SS} ..... −0.3V to +10.0V
Power Dissipation 1000mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS/PIC1650A

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	55	mA	All I/O pins @ V_{DD}
Output Buffer Supply Current	I_{XX}	—	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	—	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	V_{DD}−1	2.6	V_{DD}	V	
Output High Voltage	V_{OH}	2.4 3.5	— —	V_{DD} V_{DD}	V V	I_{OH} = −100μA (Note 4) I_{OH} = 0
Output Low Voltage (I/O only)	V_{OL1}	— — — — —	— — — — —	0.45 0.90 0.90 1.20 2.0	V V V V V	I_{OL} = 1.6mA, V_{XX} = 4.5V I_{OL} = 5.0mA, V_{XX} = 4.5V I_{OL} = 5.0mA, V_{XX} = 8.0V I_{OL} = 10.0mA, V_{XX} = 8.0V I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	I_{OL} = 1.6mA (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain I/O pins)	I_{OLC}	—	—	10	μA	$V_{SS} \leq V_{PIN} \leq 10V$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	−1.4	mA	V_{IH} = 2.4V

†Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

DC CHARACTERISTICS/PIC1650AI

Operating Temperature $T_A = -40°C$ to $+85°C$

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	60	mA	All I/O pins @ V_{DD}
Output Buffer Supply Current	I_{XX}	—	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.7	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	—	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	$V_{DD}-1$	2.6	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	$I_{OH} = -100\mu A$ (Note 4) $I_{OH} = 0$
Output Low Voltage (I/O only)	V_{OL1}	— — — — —	— — — — —	0.45 0.90 0.90 1.20 2.0	V V V V V	$I_{OL} = 1.6mA$, $V_{XX} = 4.5V$ $I_{OL} = 5.0mA$, $V_{XX} = 4.5V$ $I_{OL} = 5.0mA$, $V_{XX} = 8.0V$ $I_{OL} = 10.0mA$, $V_{XX} = 8.0V$ $I_{OL} = 20.0mA$, $V_{XX} = 8.0V$ (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	$I_{OL} = 1.6mA$ (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain I/O pins)	I_{OLC}	—	—	10	μA	$V_{SS} \leq V_{PIN} \leq 10V$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.8	mA	$V_{IL} = 0.4V$ internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	−1.8	mA	$V_{IH} = 2.4V$

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS/PIC1650A, PIC1650AI

Operating Temperature $T_A = 0°C$ to $+70°C$ (PIC1650A), $T_A = -40°C$ to $+85°C$ (PIC1650AI)

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.2MHz — 1.0MHz external time base (Note 1)
$\overline{RTCC}$ Input						
Period	t_{RT}	$t_{CY}+0.2\mu s$	—	—	—	
High Pulse Width	t_{RTH}	$\frac{1}{2}t_{RT}$	—	—	—	
Low Pulse Width	t_{RTL}	$\frac{1}{2}t_{RT}$	—	—	—	(Notes 2 and 3)
I/O Ports						
Data Input Setup Time	t_S	—	—	$\frac{1}{4}t_{CY}-125$	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	600	1000	ns	Capacitive load = 50pF
OSC Input						
External Input Impedance High	R_{OSCH}	120	800	3500	Ω	$V_{OSC} = 5V$ } Applies to external
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	$V_{OSC} = 0.4V$ } OSC drive only.

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

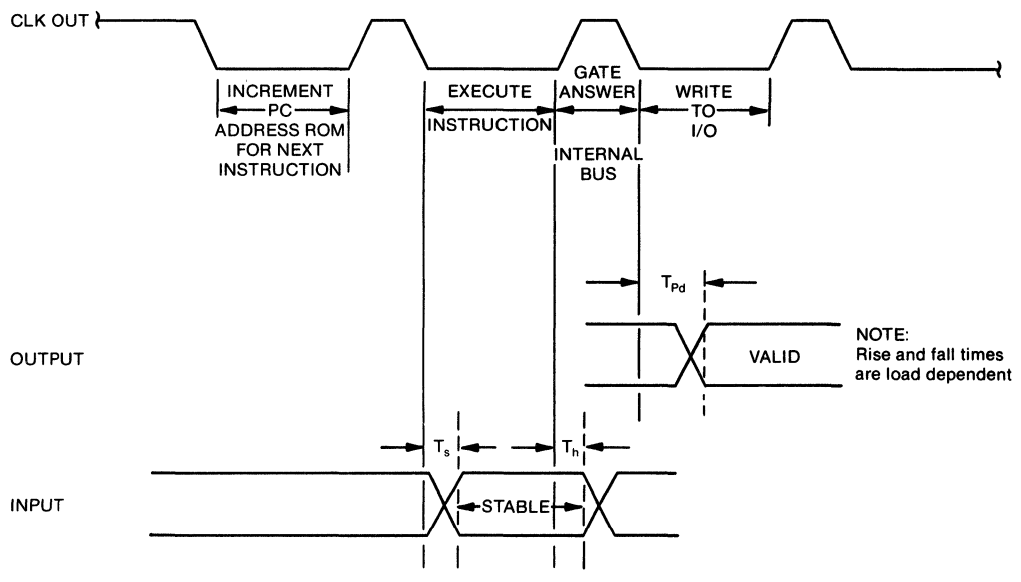
NOTES:

1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the RTCC input, CLK OUT may be directly tied to the RTCC input.
3. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows: $f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)}+0.2\mu s}$

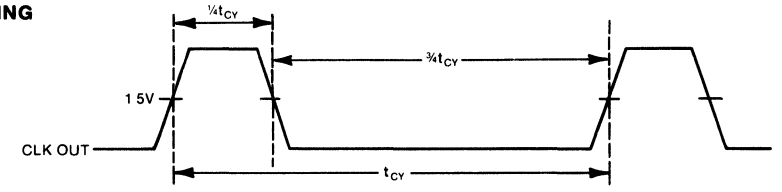
   For example: if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

MICROCOMPUTER

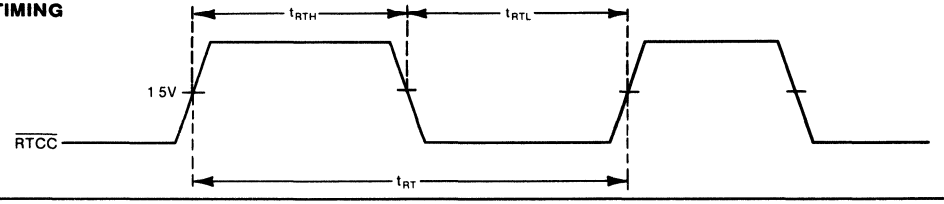
I/O TIMING



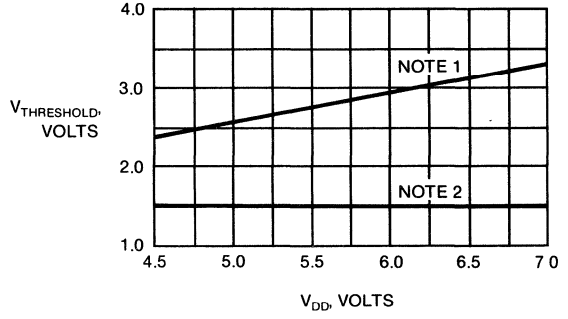
CLK OUT TIMING



$\overline{\text{RTCC}}$ TIMING



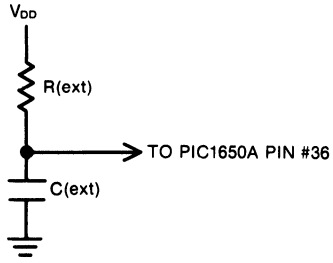
SCHMITT TRIGGER CHARACTERISTICS ($\overline{\text{RTCC}}$, $\overline{\text{MCLR}}$ and OSC PINS) $T_A = 25°C$ (TYPICAL)

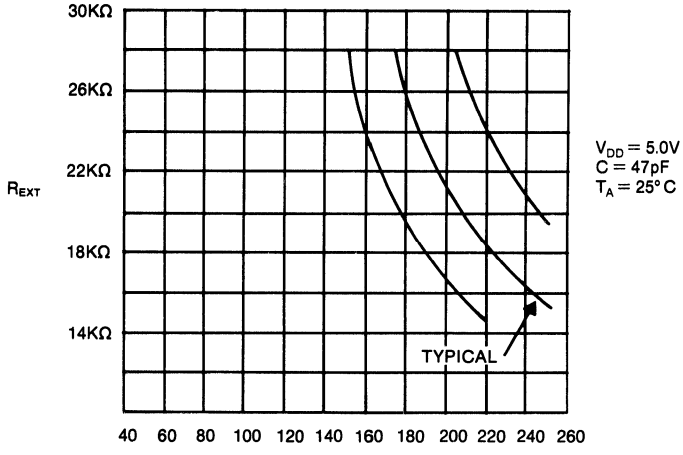


NOTES:
1. Low-to-High Threshold Voltage (V_{TLH}).
2. High-to-Low Threshold Voltage (V_{THL}).

PIC1650A OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

RC OPTION OPERATION

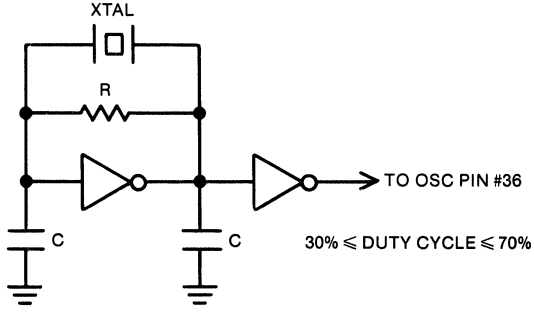




Oscillator Frequency With Typical Unit To Unit Variance

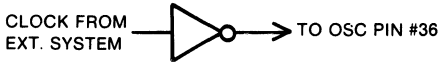
Unit to Unit Variation at V_{DD} = 5.0V, T_A = 25°C is ±25%
Variation from V_{DD} = 4.5V −7.0V referenced to 5V is −3%, +9%
Variation from T_A = 0°C −70°C referenced to 25°C is +3%, −5%

BUFFERED CRYSTAL INPUT OPERATION



The buffer must be capable of driving 120Ω, min. (800Ω, typ.) to 2.0V. However, it is recommended that the pull-down transistor on the OSC pin be removed (an option) if OSC is to be driven externally.

EXTERNAL CLOCK INPUT OPERATION



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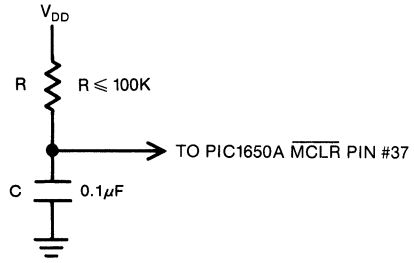
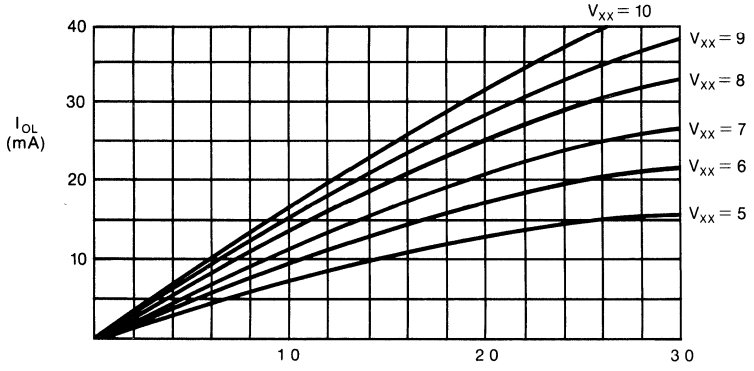
MASTER CLEAR (TYPICAL CIRCUIT)



Master Clear requires >1 0ms delay before activation after power is applied to the V_{DD} pin, for the oscillator to start up. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

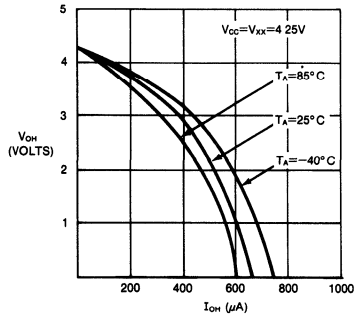
OUTPUT SINK CURRENT GRAPH



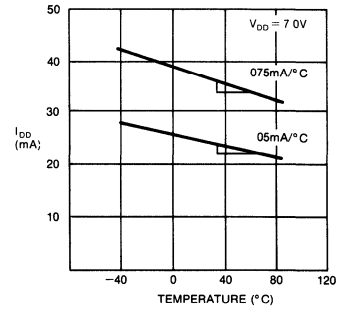
I_{OL} vs. V_{OL} TYP @ 25°C

The Output Sink Current is dependent on the V_{XX} supply and the output load. This chart shows the typical curves used to express the output drive capability.

V_{OH} VS I_{OH} (I/O PORTS) (TYPICAL)



POWER SUPPLY CURRENT VS TEMPERATURE (TYPICAL LIMITS)



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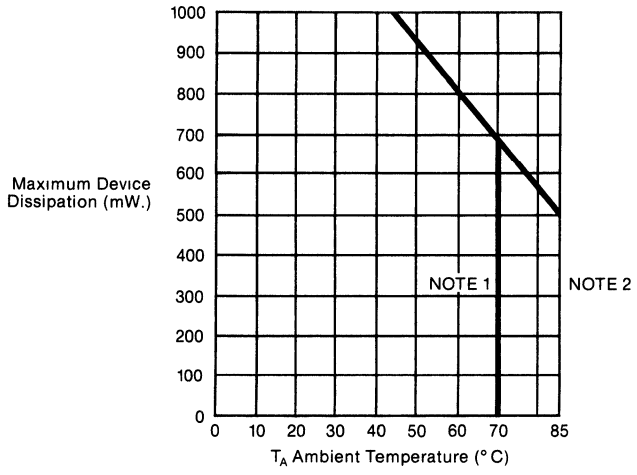
POWER DISSIPATION DERATING GRAPH



NOTES:
1. 70°C is the maximum operating temperature for standard parts.
2. 85°C is the maximum operating temperature for "I" suffix parts.

PIC1650A EMULATION CAUTIONS

When emulating a PIC1650A using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1650A mode. (Refer to PICES II Manual). The PIC1664B contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{MCLR}$ to force all I/O registers high.
2. The OSC1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 40 pin socket for the module plug.

E. Make sure that during an actual application the $\overline{MCLR}$ input swings from a low to high level a minimum of 1msec after the supply voltage is applied to allow the oscillator to start up.

F. If an external oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC1664.

G. The cable length and internal variations may cause some parameter values to differ between the PICES II module and a production PIC1650A.

8 Bit Microcomputer

FEATURES

- User programmable
- Intelligent controller for stand-alone applications
- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Self-contained crystal oscillator
- Access to RAM registers inherent in instruction
- Wide power supply operating range (4 5V to 7 0V)
- Available in two temperature ranges 0° to 70° C and −40° to 85° C
- 4 sets of 8 user defined TTL-compatible Input/Output lines
- 2 level stack for subroutine nesting

DESCRIPTION

The PIC1650XT microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

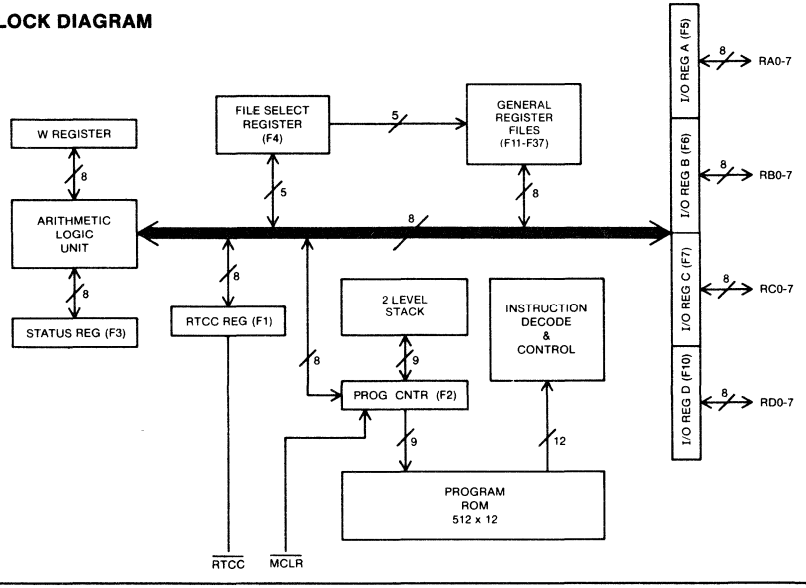
The PIC1650XT is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with an external crystal, ceramic resonator or LC network to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1664 The PIC1664 is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands The PFD1000 Field Demo System is available containing a PIC1664 with sockets for erasable CMOS PROMs Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system Easy program debugging and changing is facilitated because the user's program is stored in RAM With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design

MICROCOMPUTER

PIC1650XT BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations The instruction set also supports computing functions as well as these control and interface functions

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups. operational registers and general registers The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers The general purpose registers are used for data and control information under command of the instructions

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register

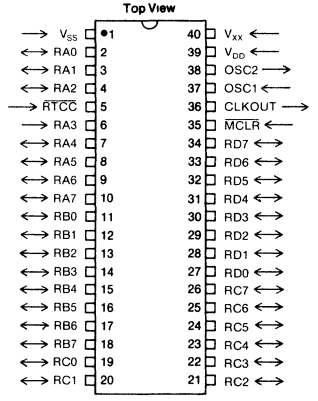
The Program ROM contains the operational program for the rest of the logic within the controller Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting Activating the $\overline{MCLR}$ input on power up initializes the ROM program to address 777_8

PIN FUNCTIONS

Signal	Function
OSC1 (input), OSC2 (output)	Oscillator pins. The oscillator frequency can be set by a crystal ceramic resonator, external LC network or driven externally. The oscillator frequency is sixteen times the instruction frequency
$\overline{RTCC}$ (input)	Real Time Clock Counter Used by the microprogram to keep track of elapsed time between events The RTCC register increments on falling edges applied to this pin This register can be loaded and read by the program This is a Schmitt trigger input
RA0-7, RB0-7, RC0-7, RD0-7 (input/output)	User programmable input/output lines These lines can be inputs and/or outputs and are under direct control of the program
$\overline{MCLR}$ (input)	Master Clear Used to initialize the internal ROM program to address 777_8 and latch all I/O register high Should be held low at least 1-10ms past the time when the power supply is valid for the oscillator to start up. This is a Schmitt trigger input
CLK OUT (output)	A signal derived from the internal oscillator Used by external devices to synchronize themselves to PIC timing
V_{DD}	Primary power supply
V_{XX}	Output Buffer power Used to enhance output current sinking capability.
V_{SS}	Ground

PIN CONFIGURATION

40 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$. However, if data are being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry). For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits: 3-7 These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used The FSR is used in generating effective file register addresses under program control When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	I/O Register A (A0-A7)
F6	I/O Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10	I/O Register D (D0-D7)
F11-F37	General Purpose Registers

The PIC1650XT has the same basic architecture as the PIC1650A with the additional enhancement described below:

Self-Contained Oscillator

When a crystal, ceramic resonator or LC network is connected between the OSC1 and OSC2 pins, the self-contained oscillator will generate a frequency determined by the external components thus allowing an accurate timing reference, a crystal, to be used for time base control with a minimum of external parts.

The output of this oscillator is divided down by 16 to give the instruction cycle time of the microcomputer, thus with a 4MHz crystal the instruction cycle time is 4μs.

When test mode is enabled, the basic instruction cycle time is a division of 4 of the frequency applied to OSC1 and OSC2 allowing simpler synchronizing of the device and tester.

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

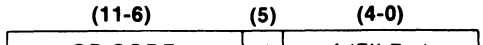
For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 4MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec

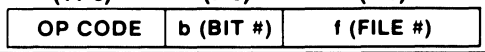
BYTE-ORIENTED FILE REGISTER OPERATIONS



For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

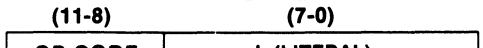
Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇋f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.
3. See notes on input only and output only ports.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

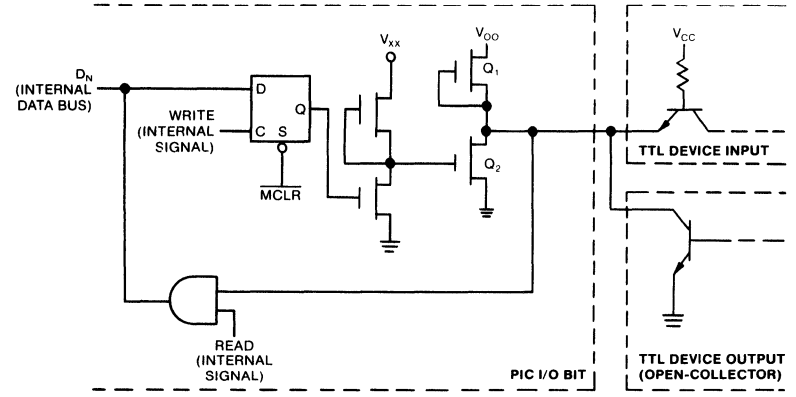
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

Bidirectional I/O Ports

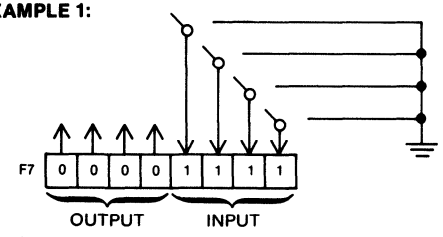
The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



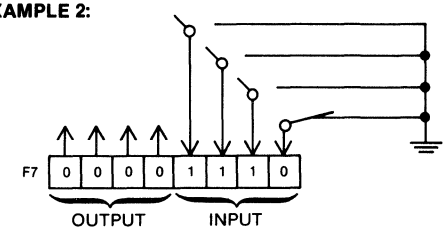
What is thought to be happening:

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient Temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any Pin with Respect to V_{SS}
(except Open Drain) ..... −0.3V to +10.0V
Power Dissipation (Note 1) 800mW
Voltage on any Pin with Respect to V_{SS} (Open Drain) ..... −0.3 to +10V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature $T_A = 0°C$ to $+70°C$

Characteristics	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Supply Current	I_{DD}	—	—	55	mA	All I/O pins @ V_{DD}
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC1)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage (OSC1)	V_{IH2}	$V_{DD}-1$	—	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$ & $\overline{RTCC}$)	V_{ILH}	$V_{DD}-1$	2.6	V_{DD}	V	
Output High Voltage	V_{OH}	2.4 3.5	— —	V_{DD} V_{DD}	V V	$I_{OH} = -100\mu A$ (Note 2) $I_{OH} = 0$
Output Low Voltage (I/O only)	V_{OL1}	—	—	0.45	V	$I_{OL} = 1.6mA$, (Note 3)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Input Low Current (all I/O ports)	I_{IL}	−0.2	—	−2.0	mA	$V_{IL} = 0.4V$ (internal pullup)
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	−1.6	mA	$V_{IH} = 2.4V$
Output Leakage Current (open drain I/O pins)	I_{OLC}	—	—	10	μA	$0V \leq V_{PIN} \leq 10V$

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
2. Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total I_{OL} for all output pins must not exceed 175mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

Operating Temperature $T_A = 0°C$ to $+70°C$

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.2MHz — 1.0MHz external time base (Note 1)
$\overline{RTCC}$ Input						
Period	t_{RT}	$t_{CY}+0.2\mu s$	—	—	—	
High Pulse Width	t_{RTH}	$\frac{1}{2}t_{RT}$	—	—	—	
Low Pulse Width	t_{RTL}	$\frac{1}{2}t_{RT}$	—	—	—	(Notes 2 and 4)
I/O Ports						
Data Input Setup Time	t_S	—	—	$\frac{1}{4}t_{CY}-125$	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	500	900	ns	Capacitive load = 50pF

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

NOTES:

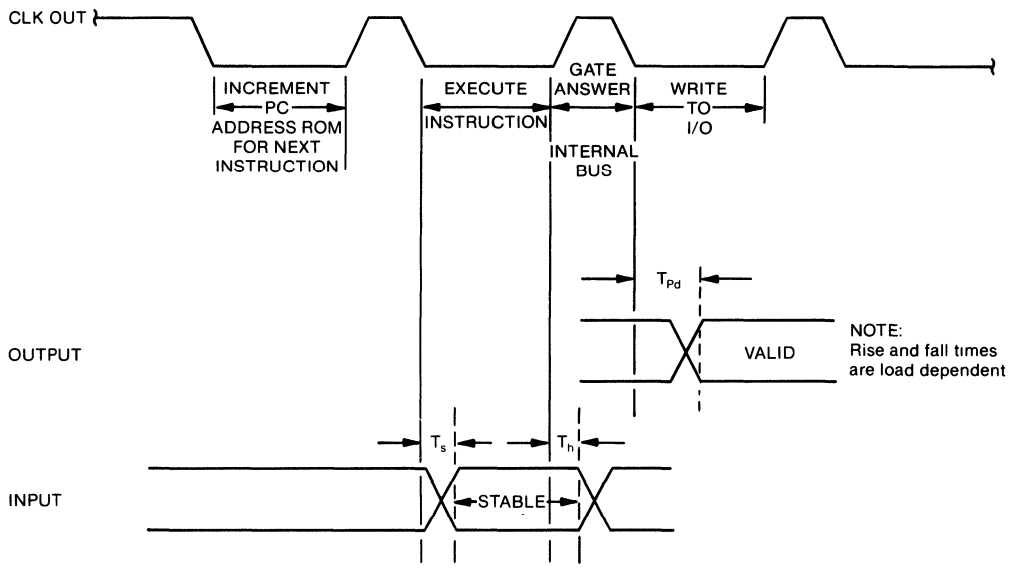
1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RTCC}$ input, CLK OUT may be directly tied to the $\overline{RTCC}$ input.
3. If an RTCC prescaler division ratio of 2, 4, 8 or 16 is selected, the maximum rise and fall times of the signal input to the $\overline{RTCC}$ pin is 200 nsecs and its duty cycle must be between 40% and 60%.
4. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)}+0.2\mu s}$$

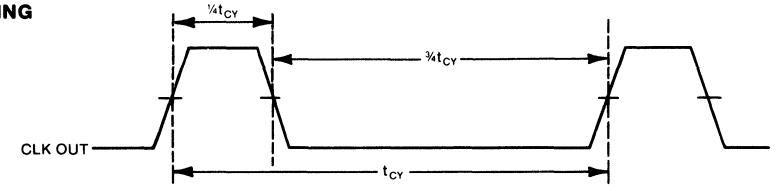
For example:

if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

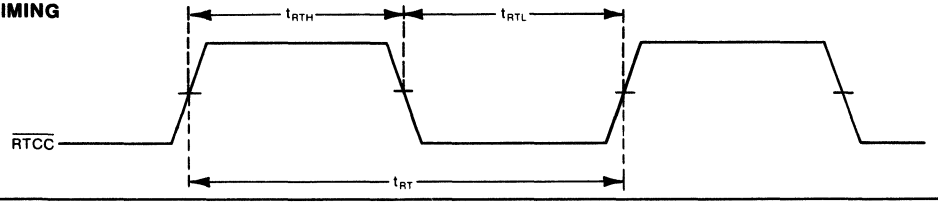
I/O TIMING



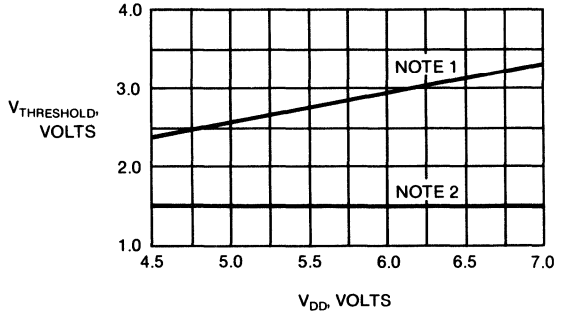
CLK OUT TIMING



$\overline{\text{RTCC}}$ TIMING



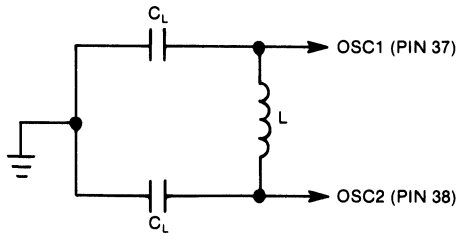
SCHMITT TRIGGER CHARACTERISTICS ($\overline{\text{RTCC}}$, $\overline{\text{MCLR}}$ and OSC PINS) $T_A = 25°C$ (TYPICAL)



NOTES:
1. Low-to-High Threshold Voltage (V_{TLH}).
2. High-to-Low Threshold Voltage (V_{THL}).

PIC1650XT OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

LC INPUT OPERATION

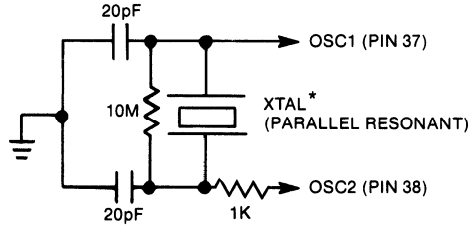


$$f_{OSC} \approx \frac{1}{2\pi \sqrt{L\,(C_L + C_{INT})}},$$

where $C_{INT} = 10pF$.

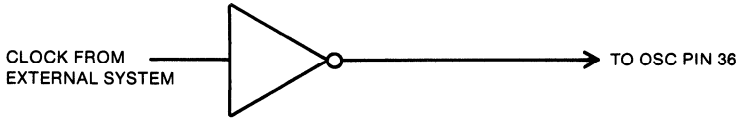
Typical values for 4MHz operation:
$L = 70\mu H$
$C_L = 10pF$

CRYSTAL INPUT OPERATION

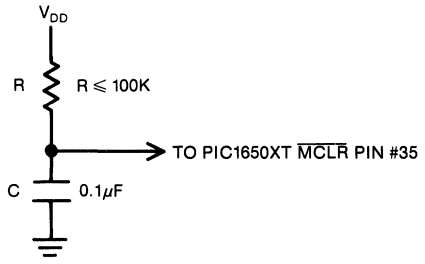


* or ceramic resonator

EXTERNAL CLOCK INPUT OPERATION

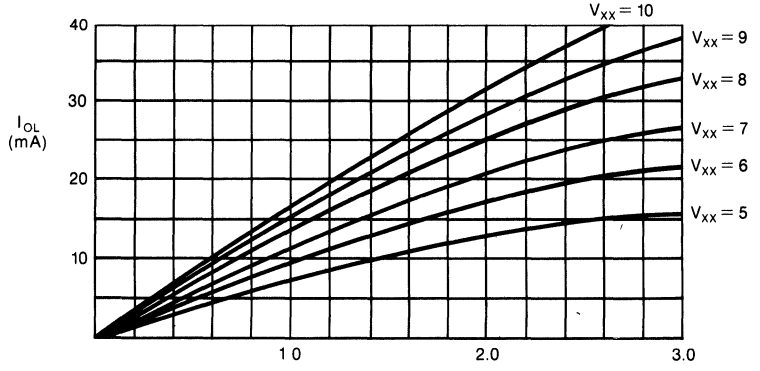


MASTER CLEAR (TYPICAL CIRCUIT)



Master Clear requires 10ms delay (assuming a 4MHz crystal) before activation after power is applied to the V_{DD} pin, for the crystal to start up. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

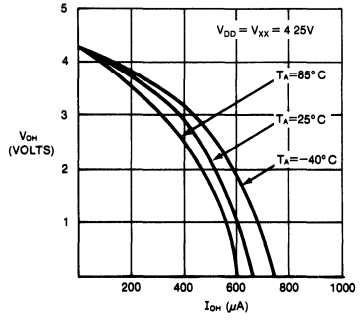
OUTPUT SINK CURRENT GRAPH



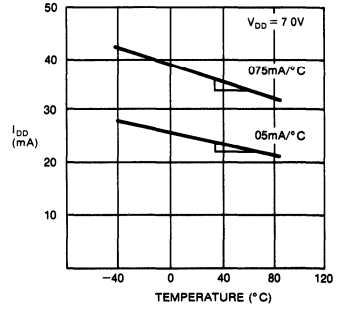
I_{OL} vs. V_{OL} TYP @ 25°C

The Output Sink Current is dependent on the V_{XX} supply and the output load. This chart shows the typical curves used to express the output drive capability.

V_{OH} VS I_{OH} (I/O PORTS) (TYPICAL)

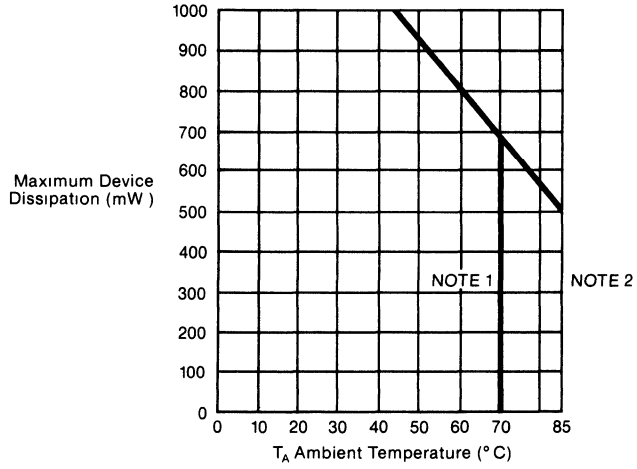


POWER SUPPLY CURRENT VS TEMPERATURE (TYPICAL LIMITS)



MICROCOMPUTER

POWER DISSIPATION DERATING GRAPH



NOTES:
1. 70°C is the maximum operating temperature for standard parts.
2. 85°C is the maximum operating temperature for "I" suffix parts.

PIC1650XT EMULATION CAUTIONS

When emulating a PIC1650XT using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1650XT mode. (Refer to PICES II Manual). The PIC1664 contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{MCLR}$ to force all I/O registers high.
2. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
3. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 40 pin socket for the module plug.

E. Make sure that during an actual application the $\overline{MCLR}$ input swings from a low to high level a minimum of 10msec after the supply voltage is applied to allow for the crystal to start up.

F. The cable length and internal variations may cause some parameter values to differ between the PICES II module and a production PIC1650XT.

G. The emulator PFD board or PICES II module offers only "internal" oscillator operation (i.e. the crystal is on the PFD or module board), as the long cable might cause unreliable crystal operation.

8 Bit Microcomputer

FEATURES

- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Self-contained oscillator for crystal or LC network
- Access to RAM registers inherent in instruction
- Wide power supply operating range (4.5V to 7.0V)
- Available in two temperature ranges: 0° to 70°C and −40° to 85°C
- 18 pin package
- 2 level stack for subroutine nesting
- Open drain option on all I/O lines
- 12 bi-directional I/O lines
- 2 μsec instruction execution time

DESCRIPTION

The PIC1654 microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to power tools, telecommunication systems, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

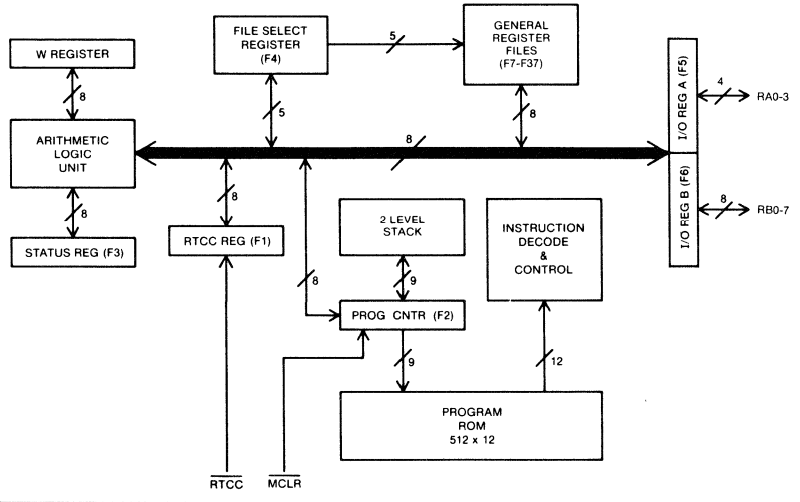
The PIC1654 is fabricated with N-Channel Silicon Gate technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with an external crystal, ceramic resonator or LC network to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling Programs can be assembled into machine language using PICAL, a powerful macroassembler. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1664-1. The PIC1664-1 is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD1007 Field Demo System is available containing a PIC1664-1 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

MICROCOMPUTER

PIC1654 BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus. the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width The Register File is divided into two functional groups· operational registers and general registers The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers The general purpose registers are used for data and control information under command of the instructions

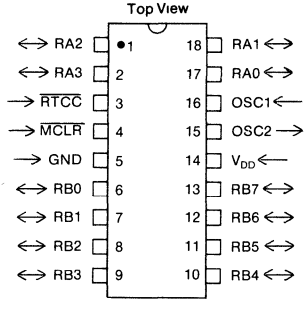
The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting Activating the $\overline{MCLR}$ input on power up initializes the ROM program to address 777_8

PIN FUNCTIONS

Signal	Function
OSC1 (input), OSC2 (output)	These pins are the time base inputs to which a crystal, ceramic resonator, LC network, or external single phase clock may be connected. The frequency of oscillation is 8 times the instruction cycle frequency.
$\overline{RTCC}$ (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The Real Time Clock Counter Register increments on falling edges applied to this pin. This register (F1) can be loaded and read by the program. This is a Schmitt trigger input A mask option will allow an internal clock signal whose period is equal to the instruction execution time to drive the real time clock counter register. In this mode, transitions in the $\overline{RTCC}$ pin will be disregarded.
RA0-3, (input/output)	4 user programmable I/O lines (F5).
RB0-7 (input/output)	8 user programmable I/O lines (F6). All inputs and outputs are under direct control of the program. A mask option will allow any I/O pin at the time of ROM pattern definition to be open drain.
$\overline{MCLR}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O registers high. Should be held low 10-75ms past the time when $V_{DD} \geq 4.5V$, depending on the crystal start up time.
V_{DD}	Power supply
V_{SS}	Ground.

PIN CONFIGURATION
18 LEAD DUAL IN LINE



MICROCOMPUTER

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$. However, if data are being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry). For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits. 3-7 These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	I/O Register A (A0-A3) (A4-A7 defined as zeroes).
F6	I/O Register B (B0-B7)
F7-F37	General Purpose Registers

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 4MHz the instruction execution time is 2 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 4 μsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4-0)
OP CODE	d	f (FILE #)

For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇌f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

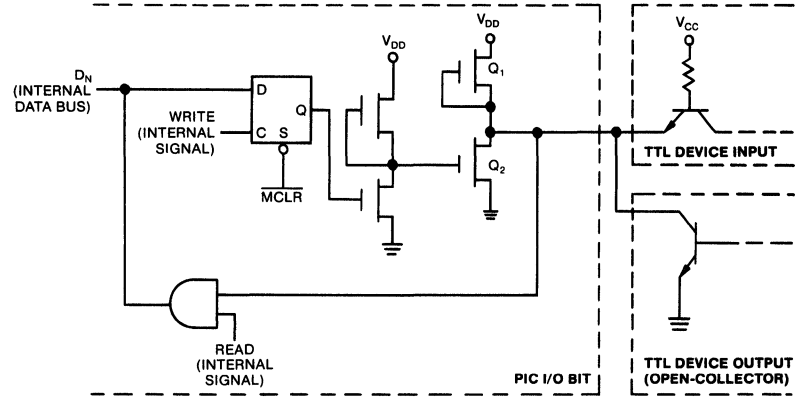
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

Bidirectional I/O Ports

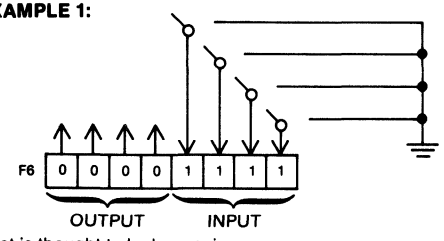
The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a B6F operation on bit 5 of F6 (port RB) will cause all eight bits of F6 to be read into the CPU. Then the BSF operation takes place on bit 5 and F6 is re-output to the output latches. If another bit of F6 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



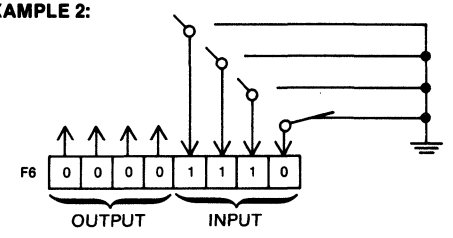
What is thought to be happening:

BSF 6,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F6:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 6,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F6:	00101110

In this case bit 0 is now latched low and is no longer useful as an unput until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient Temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any Pin with Respect to V_{SS} (except open drain) ..... −0.3V to +9.0V
Voltage on any Pin with Respect to V_{SS} (open drain) ..... −0.3V to +10V
Power Dissipation (Note 1) 800mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Power Supply Voltage	V_{DD}	4.5	—	7.0	V	
Primary Supply Current	I_{DD}	—	—	40	mA	All I/O pins @ V_{DD}
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except MCLR, $\overline{RTCC}$ & OSC1)	V_{IH}	2.4	—	V_{DD}	V	
Input High Voltage (MCLR, $\overline{RTCC}$ & OSC1)	V_{IH2}	V_{DD}−1	—	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	I_{OH} = −100μA provided by internal pullups (Note 2)
Output Low Voltage (I/O only)	V_{OL1}	—	—	0.45	V	I_{OL} = 1.6mA (Note 3)
Input Leakage Current (MCLR, $\overline{RTCC}$)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain pins)	I_{OL}	—	—	10	μA	$0V \leq V_{PIN} \leq 9V$
Input Low Current (all I/O ports)	I_{IL}	−0.2	—	−2.0	mA	V_{IL} = 0.4V (internal pullup)
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	—	mA	V_{IH} = 2.4V

† Typical data is at T_A = 25°C, V_{DD} = 5.0V

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma(V_{DD} - V_{IL})(|I_{IL}|) + \Sigma(V_{DD} - V_{OH})(|I_{OH}|) + \Sigma(V_{OL})(I_{OL})$.
2. Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total I_{OL} for all output pins must not exceed 175 mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

Operating Temperature $T_A = 0°C$ to $+70°C$

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	2	—	10	μs	0.8MHz −4.0MHz external time base (Note 1)
$\overline{RTCC}$ Input						
Period	t_{RT}	$t_{CY}+0.2\mu s$	—	—	—	Note 2
High Pulse Width	t_{RTH}	$\frac{1}{2}t_{CY}$	—	—	—	
Low Pulse Width	t_{RTL}	$\frac{1}{2}t_{CY}$	—	—	—	

NOTE:

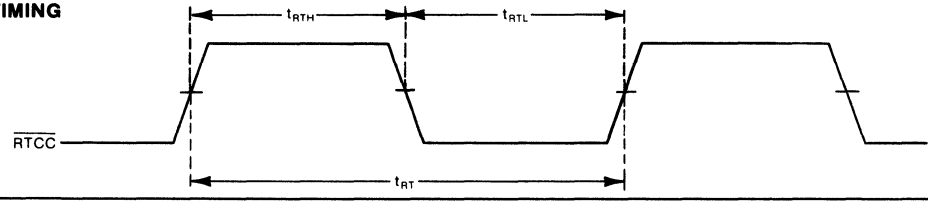
1. Instruction cycle period (t_{CY}) equals eight times the input oscillator time base period.
2. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$$

For example:

if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

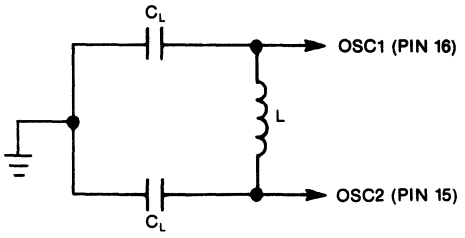
$\overline{RTCC}$ TIMING



MICROCOMPUTER

PIC1654 OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

LC INPUT OPERATION

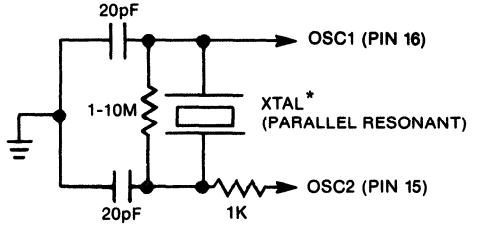


$$f_{OSC} \approx \frac{1}{2\pi\sqrt{L\,(C_L + C_{INT})}},$$

where $C_{INT} = 10pF$.

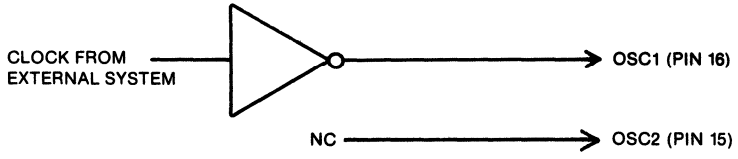
Typical values for 4MHz operation:
$L = 70\mu H$
$C_L = 10pF$

CRYSTAL INPUT OPERATION



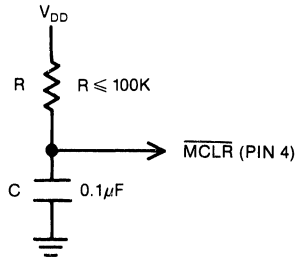
* or ceramic resonator

EXTERNAL CLOCK INPUT OPERATION



MICROCOMPUTER

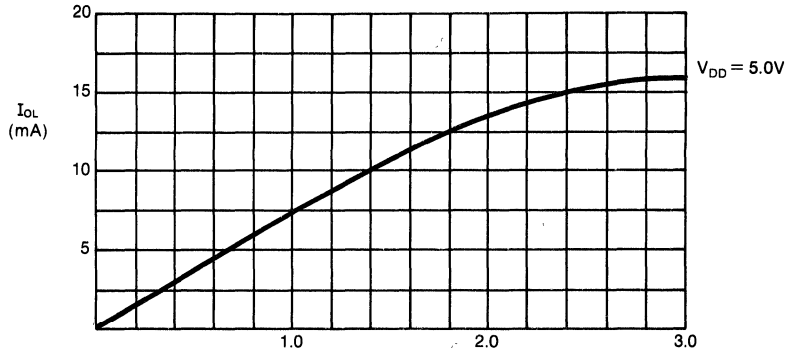
MASTER CLEAR (TYPICAL CIRCUIT)



Typical Values
R = 100K
C = 0.1μf

The $\overline{MCLR}$ signal only needs to be active low for a minimum of 1 complete instruction cycle, but this assumes power is already applied, and the oscillator is running. For initial start-up at least a 10ms delay after $V_{DD} \geq 4.5V$ should be typically allowed on $\overline{MCLR}$ for a 4 MHz crystal to start up.

OUTPUT SINK CURRENT GRAPH (TYPICAL)



V_{OL} (volts)
I_{OL} VS V_{OL}
T_A = 25°C, V_{DD} = 5.0V

8 Bit Microcomputer

FEATURES

- User programmable
- Intelligent controller for stand-alone applications
- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Self-contained oscillator
- Access to RAM registers inherent in instruction
- Wide power supply operating range (4.5V to 7.0V)
- Available in two temperature ranges: 0° to 70° C and −40° to 85° C
- 4 inputs, 8 outputs, 8 bi-directional I/O lines
- 2 level stack for subroutine nesting

DESCRIPTION

The PIC1655A microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

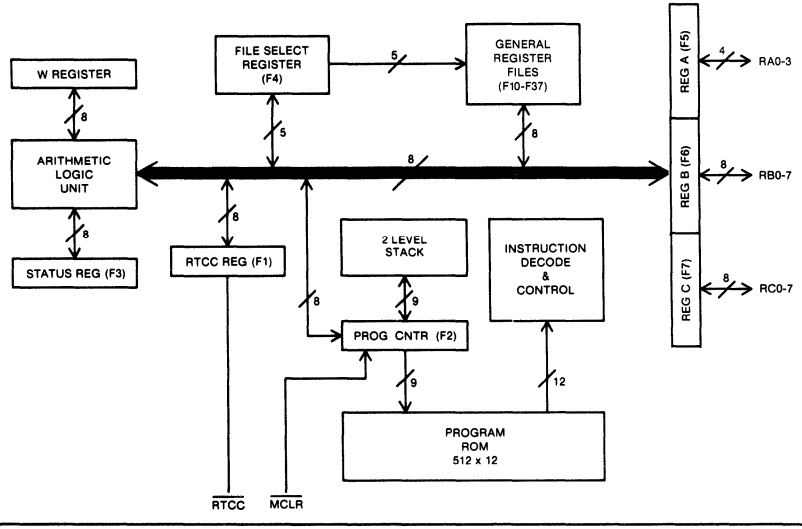
The PIC1655A is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1664. The PIC1664 is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD1000 Field Demo System is available containing a PIC1664 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

MICROCOMPUTER

PIC1655A BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

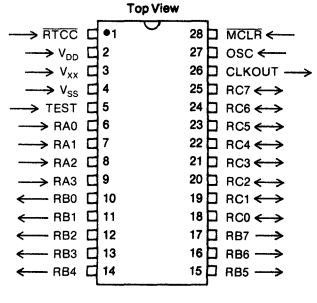
The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{MCLR}$ input on power up initializes the ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
OSC (input)	Oscillator input. This signal can be driven by an external oscillator if a precise frequency of operation is required or an external RC network can be used to set the frequency of operation of the internal clock generator. This is a Schmitt trigger input.
$\overline{RTCC}$ (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The RTCC register increments on falling edges applied to this pin. This register can be loaded and read by the program. This is a Schmitt trigger input.
RA0-3 (input)	4 input lines.
RB0-7 (output)	8 output lines.
RC0-7 (input/output)	8 user programmable input/output lines.
$\overline{MCLR}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O register high. Should be held low at least 1ms past the time when the power supply is valid. This is a Schmitt trigger input.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation.
V_{DD}	Primary power supply.
V_{XX}	Output Buffer power supply. Used to enhance output current sinking capability.
V_{SS}	Ground

PIN CONFIGURATION
28 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram The RTCC register keeps counting up after zero is reached The counter increments on the falling edge of the input $\overline{RTCC}$. However, if data are being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2) The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry) For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source

DC (Digit Carry) For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant

Z (Zero) Set if the result of an arithmetic operation is zero.

Bits: 3-7 These bits are defined as logic ones.

F4	File Select Register (FSR) Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control When accessed as a directly addressed file, the upper 3 bits are read as ones
F5	Input Register A (A0-A3) (A4-A7 defined as zeroes).
F6	Output Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10-F37	General Purpose Registers

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4-0)
OP CODE	d	f (FILE #)

For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1)

Instruction-Binary (Octal)	Name	Mnemonic,	Operands	Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇌f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction-Binary (Octal)	Name	Mnemonic,	Operands	Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

Instruction-Binary (Octal)	Name	Mnemonic,	Operands	Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations 0-377_8. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

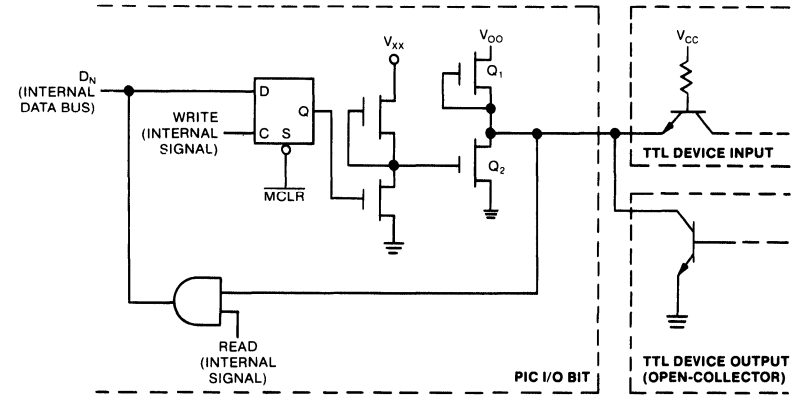
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Input Only Port: (Port RA)

The input only port of the PIC1655A consists of the four LSB's of F5 (port RA). An internal pull-up device is provided so that external pull-ups on open collector logic are unnecessary. The four MSB's of this port are always read as zeroes. Output operations to F5 are not defined. Note that the BTFSC and BTFSS instructions are input only operations and so can be used with F5. Also, file register instructions which leave the results in W can be used.

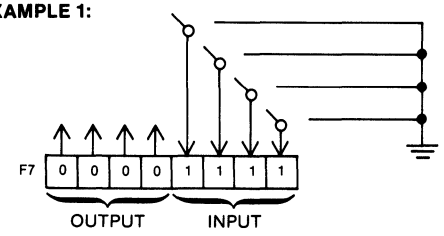
Output Only Port: (Port RB)

The output only port of the PIC1655A consists of F6 (port RB). This port contains no input circuitry and is therefore not capable of instructions requiring an input followed by an output operation. The only instructions which can validly use F6 are MOVWF and CLRF.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



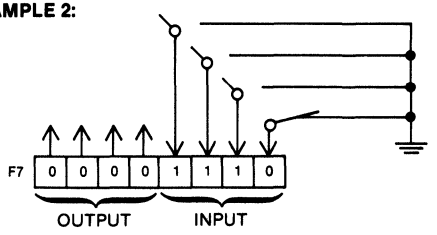
What is thought to be happening:

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any pin with Respect to V_{SS} ..... −0.3V to +10.0V
Power Dissipation (Note 1) 1000mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS/PIC1655A

Operating Temperature $T_A = 0°C$ to $+70°C$

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	50	mA	All I/O pins @ V_{DD}
Output Buffer Supply Current	I_{XX}	—	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	—	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	V_{DD}−1	2.6	V_{DD}	V	
Output High Voltage	V_{OH}	2.4 3.5	— —	V_{DD} V_{DD}	V V	$I_{OH} = -100\mu A$ (Note 4) $I_{OH} = 0$
Output Low Voltage (I/O only)	V_{OL1}	— — — — —	— — — — —	0.45 0.90 0.90 1.20 2.0	V V V V V	$I_{OL} = 1.6mA$, $V_{XX} = 4.5V$ $I_{OL} = 5.0mA$, $V_{XX} = 4.5V$ $I_{OL} = 5.0mA$, $V_{XX} = 8.0V$ $I_{OL} = 10.0mA$, $V_{XX} = 8.0V$ $I_{OL} = 20.0mA$, $V_{XX} = 8.0V$ (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	$I_{OL} = 1.6mA$ (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain I/O pins)	I_{OLC}	—	—	10	μA	$V_{SS} \leq V_{PIN} \leq 10V$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	$V_{IL} = 0.4V$ internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	−1.4	mA	$V_{IH} = 2.4V$

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

DC CHARACTERISTICS/PIC1655AI

Operating Temperature $T_A = -40°C$ to $+85°C$

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	60	mA	All I/O pins @ V_{DD}
Output Buffer Supply Current	I_{XX}	—	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.7	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH}	2.4	—	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{ILH}	$V_{DD}-1$	2.6	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	$I_{OH} = -100\mu A$ (Note 4) $I_{OH} = 0$
Output Low Voltage (I/O only)	V_{OL1}	— — — — —	— — — — —	0.45 0.90 0.90 1.20 2.0	V V V V V	$I_{OL} = 1.6mA$, $V_{XX} = 4.5V$ $I_{OL} = 5.0mA$, $V_{XX} = 4.5V$ $I_{OL} = 5.0mA$, $V_{XX} = 8.0V$ $I_{OL} = 10.0mA$, $V_{XX} = 8.0V$ $I_{OL} = 20.0mA$, $V_{XX} = 8.0V$ (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	$I_{OL} = 1.6mA$ (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain I/O pins)	I_{OLC}	—	—	10	μA	$V_{SS} \leq V_{PIN} \leq 10V$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.8	mA	$V_{IL} = 0.4V$ internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	−1.8	mA	$V_{IH} = 2.4V$

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS/PIC1655A, PIC1655AI

Operating Temperature $T_A = 0°C$ to $+70°C$ (PIC1655A), $T_A = -40°C$ to $+85°C$ (PIC1655AI)

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.2MHz — 1.0MHz external time base (Note 1)
$\overline{RTCC}$ Input						
Period	t_{RT}	$t_{CY}+0.2\mu s$	—	—	—	
High Pulse Width	t_{RTH}	$\frac{1}{2}t_{RT}$	—	—	—	
Low Pulse Width	t_{RTL}	$\frac{1}{2}t_{RT}$	—	—	—	(Notes 2 and 3)
I/O Ports						
Data Input Setup Time	t_S	—	—	$\frac{1}{4}t_{CY}-125$	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	600	1000	ns	Capacitive load = 50pF
OSC Input						
External Input Impedance High	R_{OSCH}	120	800	3500	Ω	$V_{OSC} = 5V$ } Applies to external
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	$V_{OSC} = 0.4V$ } OSC drive only.

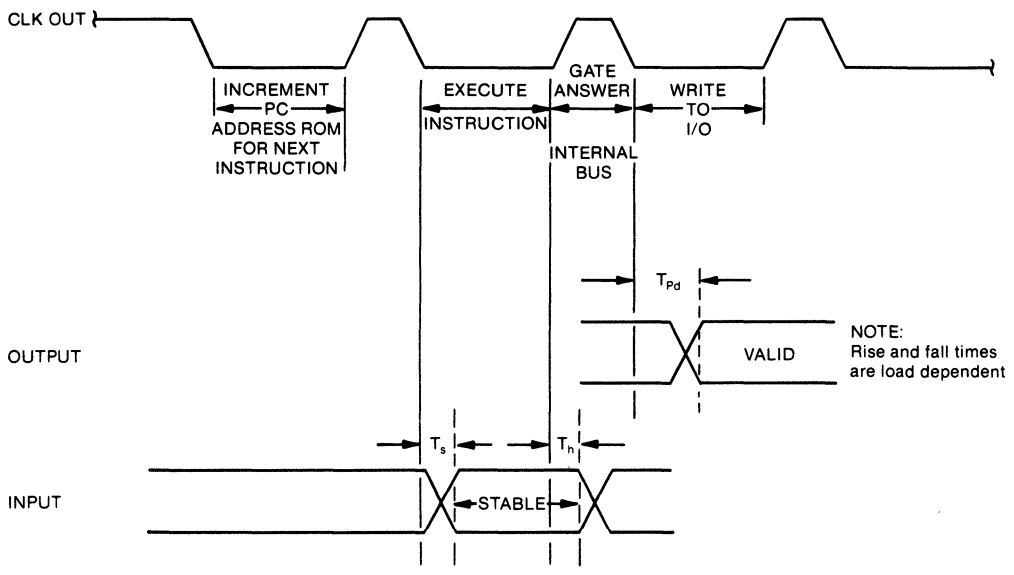
†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

NOTES:

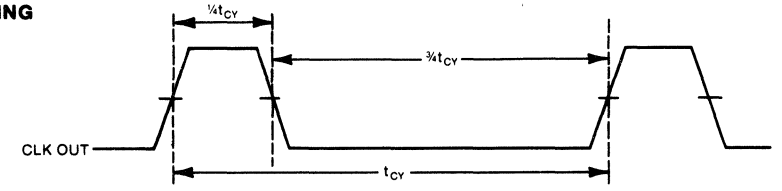
1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the RTCC input, CLK OUT may be directly tied to the RTCC input.
3. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows: $f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$
   For example: if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

MICROCOMPUTER

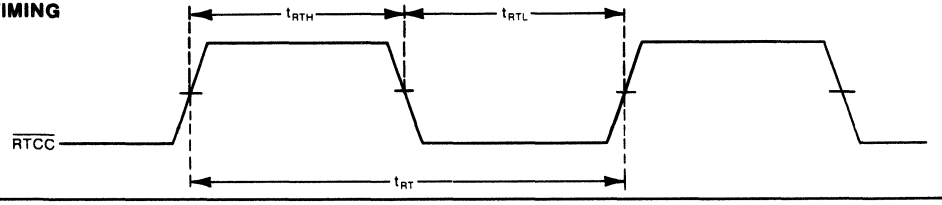
I/O TIMING



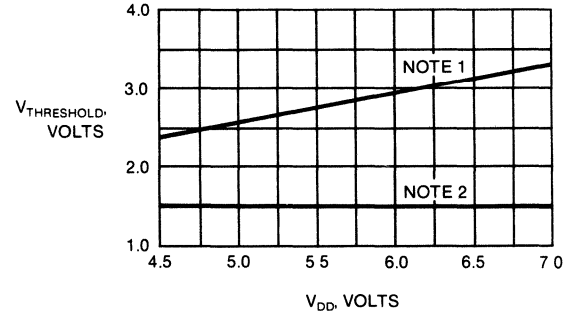
CLK OUT TIMING



$\overline{\text{RTCC}}$ TIMING



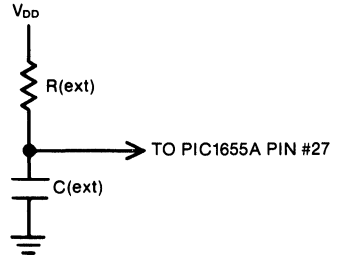
SCHMITT TRIGGER CHARACTERISTICS ($\overline{\text{RTCC}}$, $\overline{\text{MCLR}}$ and OSC PINS) $T_A = 25°C$ (TYPICAL)

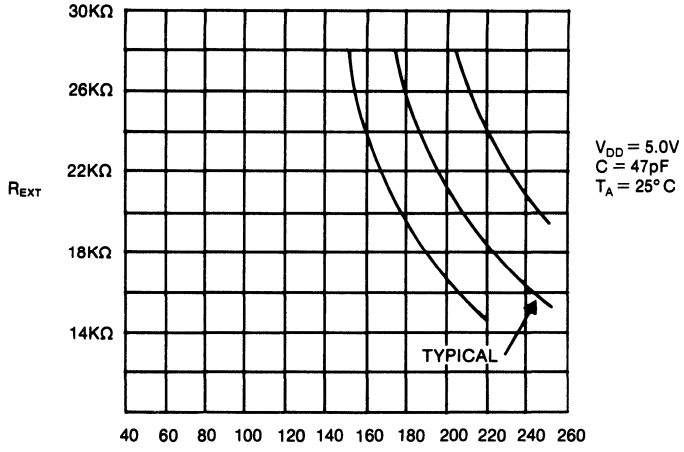


NOTES:
1. Low-to-High Threshold Voltage (V_{TLH}).
2. High-to-Low Threshold Voltage (V_{THL}).

PIC1655A OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

RC OPTION OPERATION

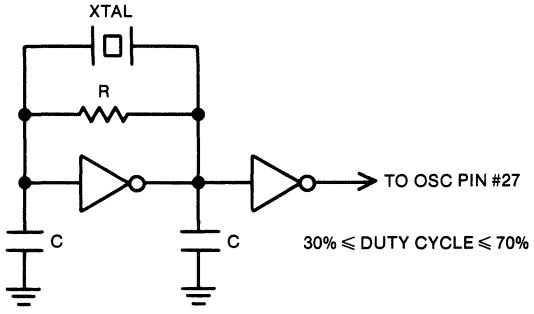




Oscillator Frequency With Typical Unit To Unit Variance

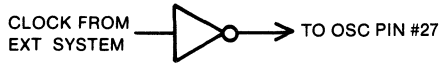
Unit to Unit Variation at V_{DD} = 5.0V, T_A = 25° C is ±25%
Variation from V_{DD} = 4.5V −7.0V referenced to 5V is −3%, +9%
Variation from T_A = 0° C −70° C referenced to 25° C is +3%, −5%

BUFFERED CRYSTAL INPUT OPERATION

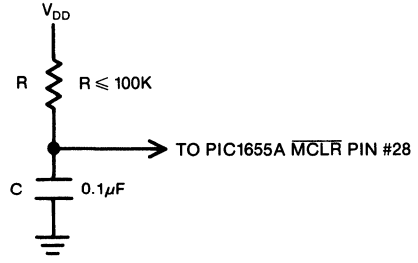


The buffer must be capable of driving 120Ω, min. (800Ω, typ.) to 2.0V. However, it is recommended that the pull-down transistor on the OSC pin be removed (an option) if OSC is to be driven externally.

EXTERNAL CLOCK INPUT OPERATION

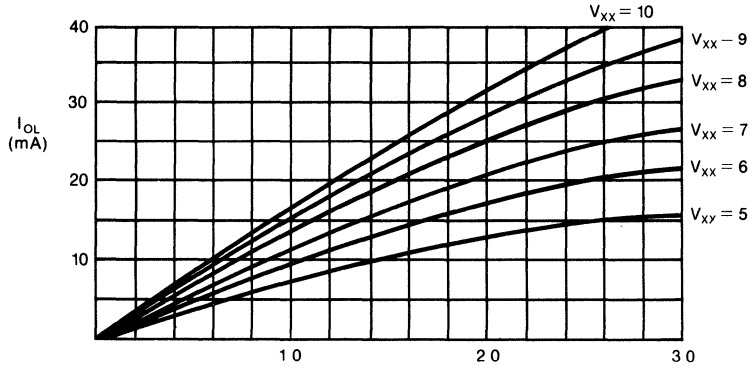


MASTER CLEAR (TYPICAL CIRCUIT)



Master Clear requires >1.0ms delay before activation after power is applied to the V_{DD} pin, for the oscillator to start up. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

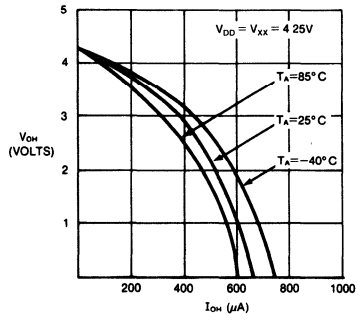
OUTPUT SINK CURRENT GRAPH



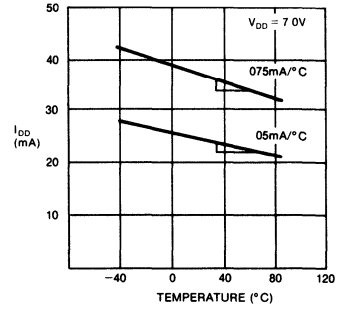
I_{OL} vs. V_{OL} TYP @ 25°C

The Output Sink Current is dependent on the V_{XX} supply and the output load. This chart shows the typical curves used to express the output drive capability.

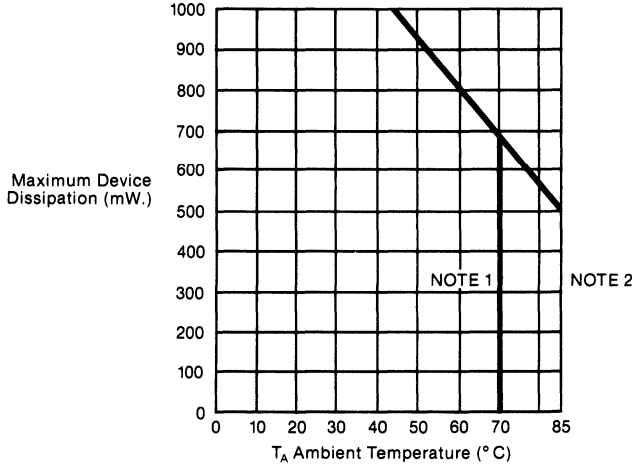
V_{OH} VS I_{OH} (I/O PORTS) (TYPICAL)



POWER SUPPLY CURRENT VS TEMPERATURE (TYPICAL LIMITS)



POWER DISSIPATION DERATING GRAPH



NOTES:
1. 70°C is the maximum operating temperature for standard parts
2. 85°C is the maximum operating temperature for "I" suffix parts.

PIC1655A EMULATION CAUTIONS

When emulating a PIC1655A using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1650A mode. (Refer to the PICES Manual). The PIC1664 contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{\text{MCLR}}$ to force all I/O registers high.
2. The OSC 1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 28 pin socket for the module plug.

E. Make sure that during an actual application the MCLR input swings from a low to high level a minimum of 1msec after the supply voltage is applied.

F. If an oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC1664.

G. The cable length and internal variations may cause some parameter values to differ between the PICES II module and a production PIC1655A.

8 Bit Microcomputer

FEATURES

- User programmable
- Intelligent controller for stand-alone applications
- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Self-contained crystal oscillator
- Access to RAM registers inherent in instruction
- Wide power supply operating range (4.5V to 7.0V)
- Available in two temperature ranges: 0° to 70° C and −40° to 85° C
- 4 inputs, 8 outputs, 8 bi-directional I/O lines
- 2 level stack for subroutine nesting
- Mask programmable prescaler for RTCC
- Mask programmable open drain option on all I/O lines

DESCRIPTION

The PIC1655XT microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

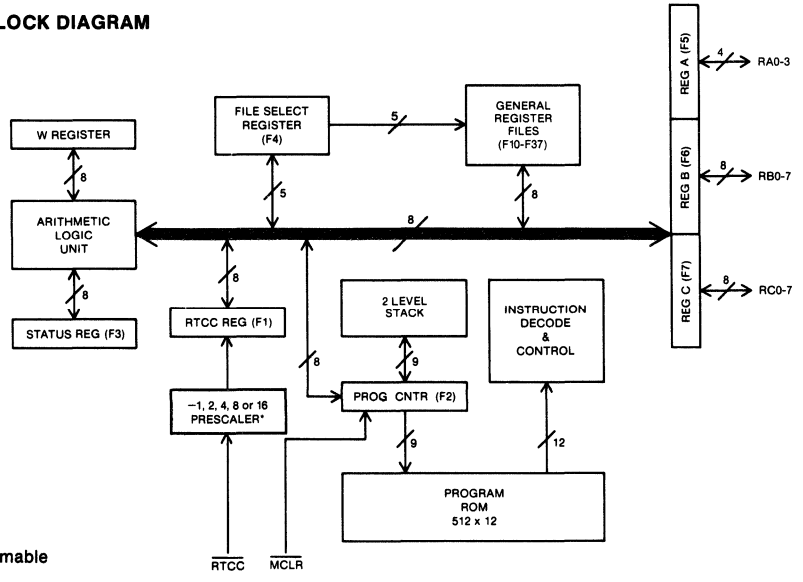
The PIC1655XT is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with an external crystal,ceramic resonator or LC network to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1664. The PIC1664 is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD1000 Field Demo System is available containing a PIC1664 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

MICROCOMPUTER

PIC1655XT BLOCK DIAGRAM



*Mask programmable

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

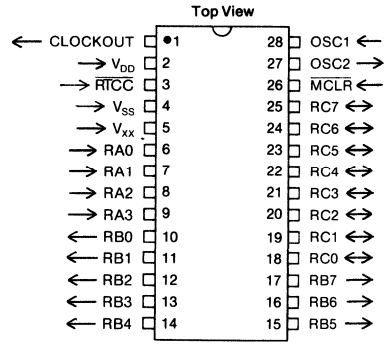
The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{MCLR}$ input on power up initializes the ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
OSC1 (Input), OSC2 (output)	Oscillator pins. The oscillator frequency can be set by a crystal, ceramic resonator, external LC network or driven externally. The oscillator frequency is sixteen times the instruction frequency.
$\overline{RTCC}$ (Input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The Real Time Clock Counter, Register increments on falling edges applied to this pin. This register can be loaded and read by the program. This is a Schmitt trigger input except when a prescaler division ratio of 2, 4, 8 or 16 is selected in which case the input is TTL compatible.
RA0-3 (Input)	4 input lines
RB0-7 (output)	8 output lines
RC0-7 (Input/output)	8 user programmable input/output lines All inputs and outputs are under direct control of the program.
$\overline{MCLR}$ (Input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O registers high. Should be held low at least 1ms past the time when power supply is valid. This is a Schmitt trigger input.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
V_{DD}	Primary power supply.
V_{XX}	Output Buffer power supply. Used to enhance output current sinking capability.
V_{SS}	Ground

PIN CONFIGURATION
28 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register F0 is thus useful as an indirect address pointer For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W
F1	Real Time Clock Counter Register This register can be loaded and read by the microprogram The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$. However, if data are being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2) The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry)·	For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant. For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.
DC (Digit Carry)	For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant
Z (Zero)·	Set if the result of an arithmetic operation is zero
Bits· 3-7	These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones
F5	Input Register A (A0-A3) (A4-A7 defined as zeroes).
F6	Output Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10-F37	General Purpose Registers

The PIC1655XT has the same basic architecture as the PIC1655A with the additional enhancements described below:

Real Time Clock Counter

The Real Time Clock Counter can be read from and written to under software control In addition, it can be used to count external events via the RTCC input. A prescaler counter between the RTCC input and the Real Time Clock Counter can be mask programmed to enable the RTCC register to increment every 1, 2, 4, 8, or 16 negative edges of the RTCC input pin

This allows the maximum frequency of the RTCC input to be (assume an instruction cycle time of 4μs):

Prescaler Division Ratio	Maximum Input Frequency
1	0.238MHz
2	0.476MHz
4	0.952MHz
8	1.904MHz
16	3.808MHz

NOTE: The Schmitt trigger input is valid only when a division ratio of 1 is selected. Otherwise, the input is a normal TTL compatible input.

Self-Contained Oscillator

When a crystal, ceramic resonator or LC network is connected between the OSC1 and OSC2 pins, the self-contained oscillator will generate a frequency determined by the external components thus allowing an accurate timing reference, a crystal, to be used for time base control with a minimum of external parts

The output of this oscillator is divided down by 16 to give the instruction cycle time of the microcomputer, thus with a 4MHz crystal the instruction cycle time is 4μs

When test mode is enabled, the basic instruction cycle time is a division of 4 of the frequency applied to OSC1 and OSC2 allowing simpler synchronizing of the device and tester

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value

For an oscillator frequency of 4MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4-0)
OP CODE	d	f (FILE #)

For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	WVf→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇋f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	kVW→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2 Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.
3. See notes on input only and output only ports (F5 and F6 respectively).

SUPPLEMENTAL INSTRUCTION SET SUMMARY

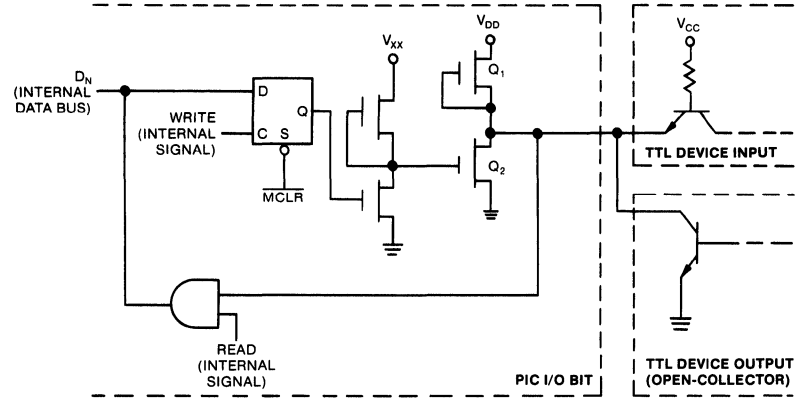
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Input Only Port: (Port RA)

The input only port of the PIC1655XT consists of the four LSB's of F5 (port RA). An internal pull-up device is provided so that external pull-ups on open collector logic are unnecessary. The four MSB's of this port are always read as zeroes. Output operations to F5 are not defined. Note that the BTFSC and BTFSS instructions are input only operations and so can be used with F5. Also, file register instructions which leave the results in W can be used.

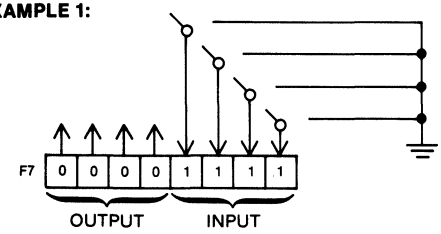
Output Only Port (Port RB)

The output only port of the PIC1655XT consists of F6 (port RB). This port contains no input circuitry and is therefore not capable of instructions requiring an input followed by an output operation. The only instructions which can validly use F6 are MOVWF and CLRF

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



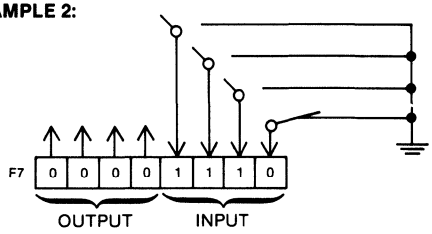
What is thought to be happening:

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low·

BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an unput until set high again.

MICROCOMPUTER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... −0.3V to +9.0V
Power Dissipation (Note 1) 800mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS Operating Temperature $T_A = 0°C$ to $+70°C$

Characteristics	Sym	Min	Typ†	Max	Units	Conditions
Power Supply Voltage	V_{DD}	4.5	—	7.0	V	
Primary Supply Current	I_{DD}	—	—	65	mA	All I/O pins @ V_{DD} (Note 5)
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Output Buffer Supply Current	I_{XX}	—	1	5	mA	All I/O pins @ V_{DD}
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$, OSC1 When Prescaler = 2, 4, 8 or 16)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage (MCLR, $\overline{RTCC}$, OSC1 When Prescaler = 1)	V_{IH2}	V_{DD}−1	—	V_{DD}	V	
Output High Voltage	V_{OH}	2.4 3.5	— —	V_{DD} V_{DD}	V V	$I_{OH} = 100\mu A$ (Note 3) $I_{OH} = 0$
Output Low Voltage (I/O only)	V_{OL}	—	—	0.45	V	$I_{OL} = 1.6mA$ (Note 4)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain pins)	I_{OL}	—	—	10	μA	$0V \leq V$ pin $\leq 10V$
Input Low Current (all I/O ports)	I_{IL}	−0.2	—	−2.0	mA	$V_{IL} = 0.4V$ internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	−1.6	mA	$V_{IH} = 2.4V$

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
2. V_{XX} supply drives only the I/O ports.
3. Positive current indicates current into pin. Negative current indicates current out of pin.
4. Total I_{OL} for all output pins must not exceed 175mA.
5. I_{DD} max current spec is preliminary and subject to change.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

Operating Temperature $T_A = 0°C$ to $+70°C$

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0 2MHz — 1 0MHz external time base (Note 1)
$\overline{RTCC}$ Input						Prescaler division ratio = 1
Period	t_{RT}	$t_{CY}+0.2\mu s$	—	—	—	
High Pulse Width	t_{RTH}	$\frac{1}{2}t_{RT}$	—	—	—	
Low Pulse Width	t_{RTL}	$\frac{1}{2}t_{RT}$	—	—	—	(Notes 2 and 4)
I/O Ports						
Data Input Setup Time	t_S	—	—	$\frac{1}{4}t_{CY}-125$	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	500	900	ns	Capacitive load = 50pF

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

NOTES:

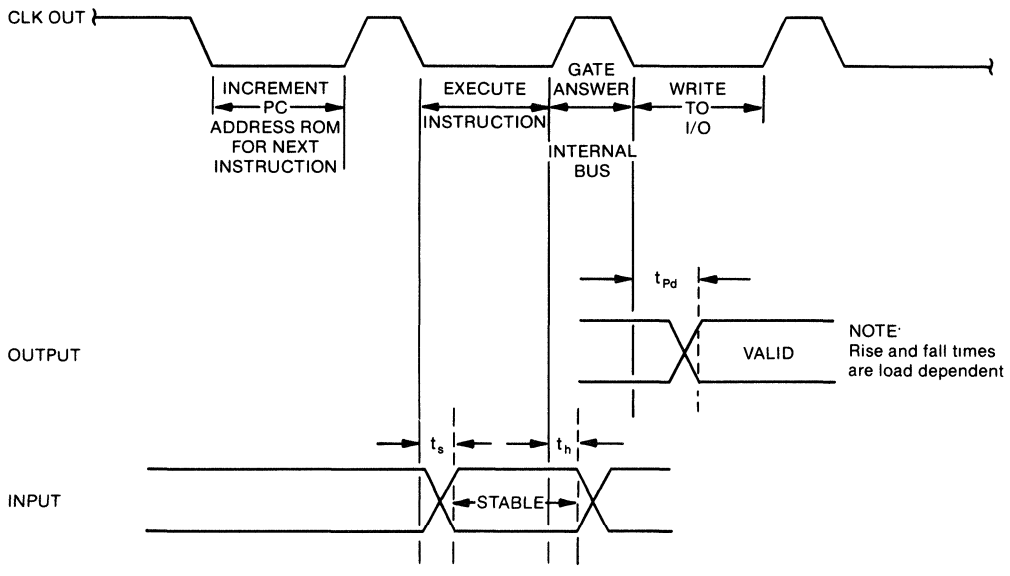
1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RTCC}$ input, CLK OUT may be directly tied to the $\overline{RTCC}$ input.
3. If an $\overline{RTCC}$ prescaler division ratio of 2, 4, 8 or 16 is selected, the maximum rise and fall times of the signal input to the $\overline{RTCC}$ pin is 200 nsecs and its duty cycle must be between 40% and 60%
4. The maximum frequency which may be input to the $\overline{RTCC}$ pin for a division ratio of 1 is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)}+0.2\mu s}$$

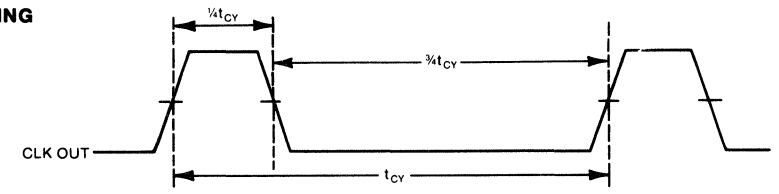
For example:

if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

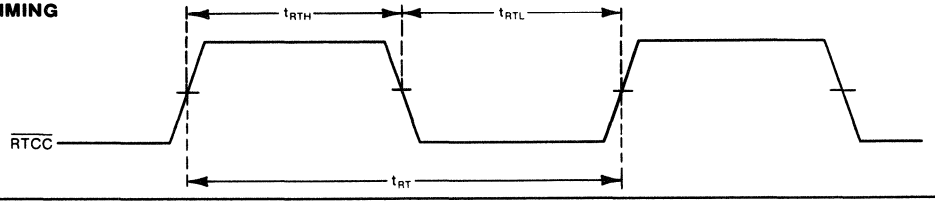
I/O TIMING



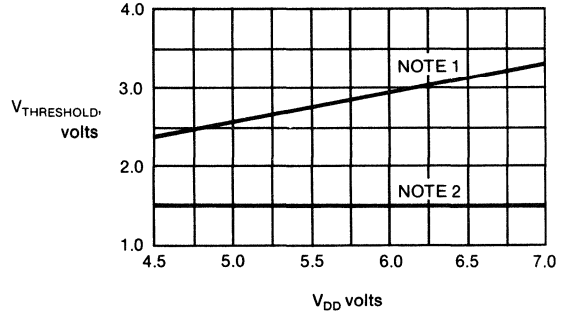
CLK OUT TIMING



$\overline{\text{RTCC}}$ TIMING



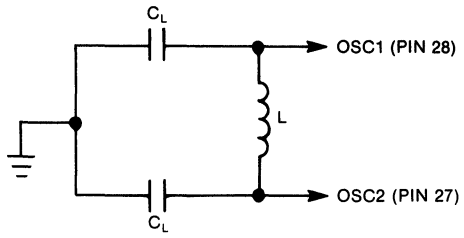
SCHMITT TRIGGER CHARACTERISTICS (Typical @ 25°C)



NOTES:
1. Low-to-High Threshold Voltage (V_{TLH}).
2. High-to-Low Threshold Voltage (V_{THL}).

PIC1655XT OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

LC INPUT OPERATION

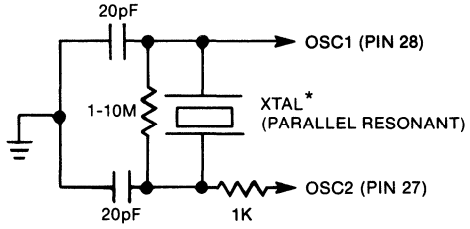


$$f_{OSC} \approx \frac{1}{2\pi\sqrt{L\,(C_L + C_{INT})}},$$

where $C_{INT} = 10pF$.

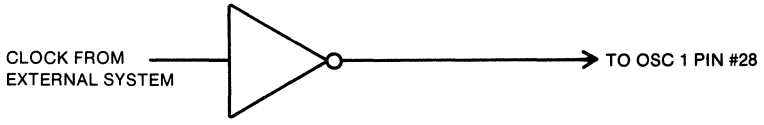
Typical values for 4MHz operation:
$L = 70\mu H$
$C_L = 10pF$

CRYSTAL INPUT OPERATION

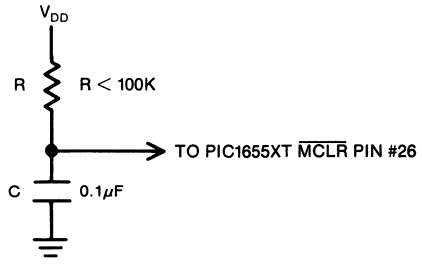


*OR CERAMIC RESONATOR

EXTERNAL CLOCK INPUT OPERATION

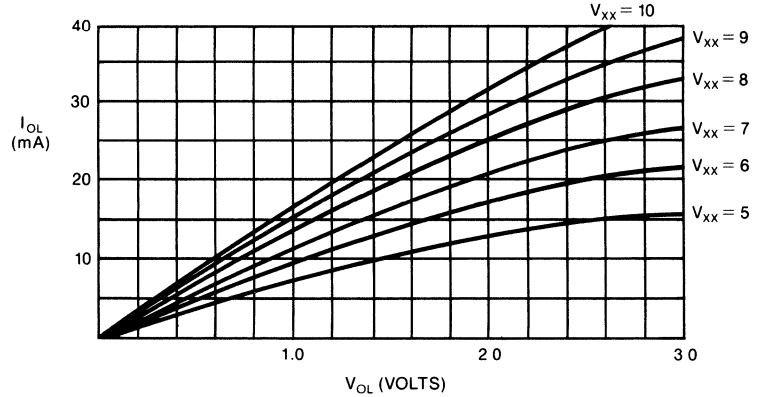


MASTER CLEAR (TYPICAL CIRCUIT)



Master Clear requires 10ms delay (assuming a 4MHz crystal) before activation after power is applied to the V_{DD} pin, for the crystal to start up. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

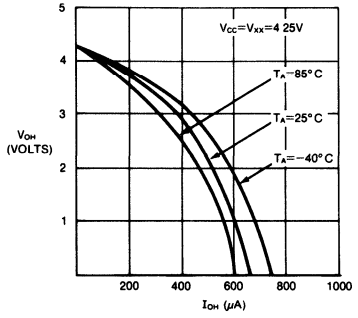
OUTPUT SINK CURRENT GRAPH



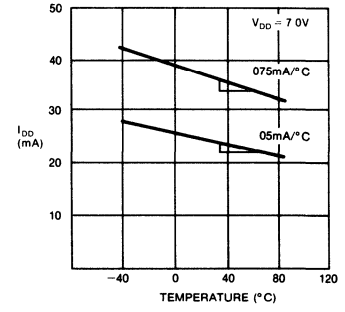
I_{OL} vs. V_{OL} TYP @ 25°C

The Output Sink Current is dependent on the V_{XX} supply and the output load. This chart shows the typical curves used to express the output drive capability.

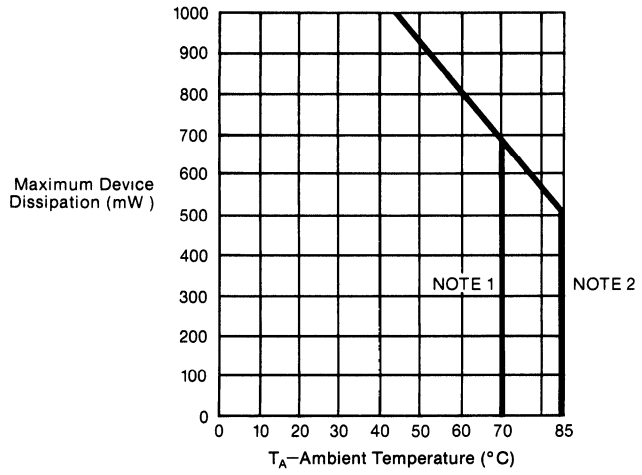
V_{OH} VS I_{OH} (I/O PORTS) (TYPICAL)



POWER SUPPLY CURRENT VS TEMPERATURE (TYPICAL LIMITS)



POWER DISSIPATION DERATING GRAPH



NOTES:
1. 70° C is the maximum operating temperature for standard parts.
2. 85° C is the maximum operating temperature for "I" suffix parts.

PIC1655XT EMULATION CAUTIONS

When emulating a PIC1655XT using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1655XT mode. (Refer to PICES II Manual). The PIC1664 contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{MCLR}$ to force all I/O registers high.
2. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
3. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 28 pin socket for the module plug.

E Make sure that during an actual application the $\overline{MCLR}$ input swings from a low to high level a minimum of 10msec after the supply voltage is applied to allow for the crystal to start up.

F. The cable length and internal variations may cause some parameter values to differ between PICES II Module and a production PIC1655XT.

G. The emulator PFD board or PICES II Module offers only "internal" oscillator operation (i.e. the crystal is on the PFD or Module Board) as the long cable might cause unreliable crystal operation.

8 Bit Microcomputer

FEATURES

- User programmable
- Intelligent controller for stand-alone applications
- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Self-contained oscillator for crystal, ceramic resonator or RC network
- Access to RAM registers inherent in instruction
- Wide power supply operating range (2.5V to 6.0V)
- Low power dissipation
- 4 inputs, 8 outputs, 8 bi-directional I/O lines
- 2 level stack for subroutine nesting
- Software compatible with other PIC series microcomputers

DESCRIPTION

The PIC16C55 microcomputer is a CMOS device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to power tools, telecommunications systems, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

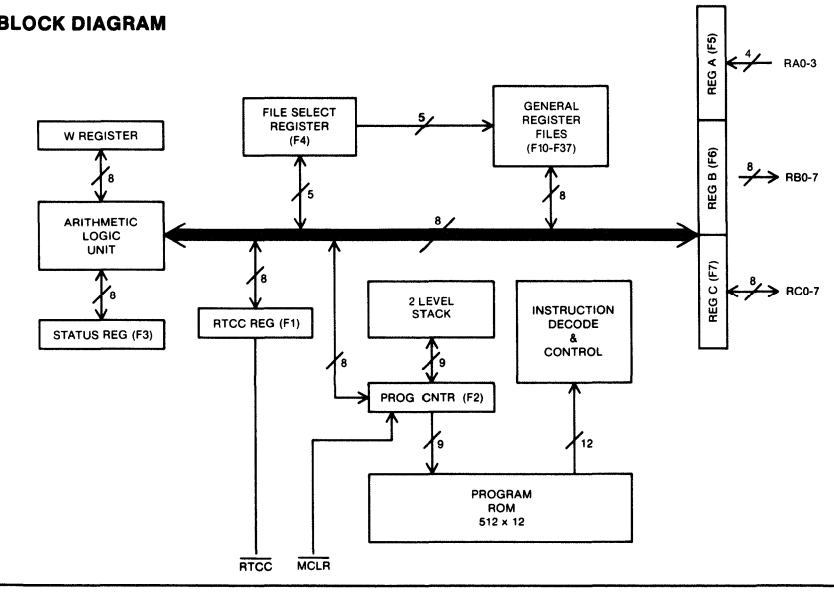
The PIC16C55 is fabricated with complementary MOS technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or crystal or ceramic resonator, for greater accuracy) to establish the frequency.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC16C63. The PIC16C63 is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PIC Field Demo System is available containing a PIC16C63 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

MICROCOMPUTER

PIC16C55 BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus· the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers The general purpose registers are used for data and control information under command of the instructions.

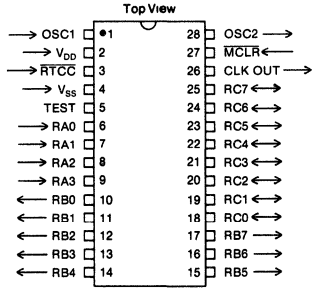
The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting

PIN FUNCTIONS

Signal	Function
OSC1 (input), OSC2 (output)	Oscillator pins. These pins are used to derive the internal clock for the chip. A crystal, ceramic resonator or RC network may be used in conjunction with OSC1 and OSC2. Additionally, OSC1 may be driven by an external oscillator.
$\overline{\text{RTCC}}$ (input)	Real Time Clock Counter. File 1 increments on falling edges applied to this pin. This register can be loaded and read by the program.
RA0-3 (input)	Dedicated input lines read under control of the program.The 4 MSB's are always read as logic zeroes.
RB0-7 (output)	Dedicated output lines, user programmable under direct control of the program.
RC0-7 (input/output)	User programmable input/output lines. These are controlled by the program to be inputs and/or outputs.
$\overline{\text{MCLR}}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777 octal and set output status latches into the high impedance state.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be connected to V_{SS} or left open circuit for normal operation.
V_{DD}	Power supply.
V_{SS}	Ground

PIN CONFIGURATION
28 LEAD DUAL IN LINE



MICROCOMPUTER

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$. However, if data are being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2) The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. When F3 is the destination register, the status flags are overwritten.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source

DC (Digit Carry). For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits: 3-7 These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	Input Register A (A0-A3). (A4-A7 defined as zeroes). Output operations to this register are not defined.
F6	Output Register B (B0-B7). When an instruction involving a read is executed on this port (all instructions except literal and control operations, NOP, MOVWF, CLRW and CLRF) the data will be read from the latch (not from the pins).
F7	I/O Register C (C0-C7). For use as an input port, the output latch should be tristated. The input port is non-latching so an input must be present until read by an instruction. When an instruction involving a read is executed on this port (as in F6), the data will be read from the pins, whether or not it is tristated (i.e., selected as an input or an output).
F10-F37	General Purpose Registers.

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

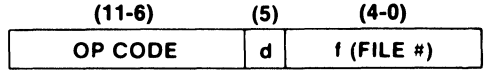
For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz the instruction execution time is 5 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 10 μsec.

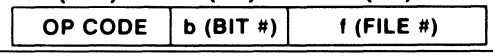
BYTE-ORIENTED FILE REGISTER OPERATIONS



For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇋f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 010 (0002)	Return	RETURN	—	Stack→PC	None
000 000 0ff fff (0000)	Tristate port f	TRIS	f	W→Tristate status f [f=F6 or F7]	None
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations 0-377_8. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.
3. TRIS f(where f=6 or 7) causes the contents of W to be written to the tristate latches of the specified file. A one forces the pin to trist the output buffer to a high impedance state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

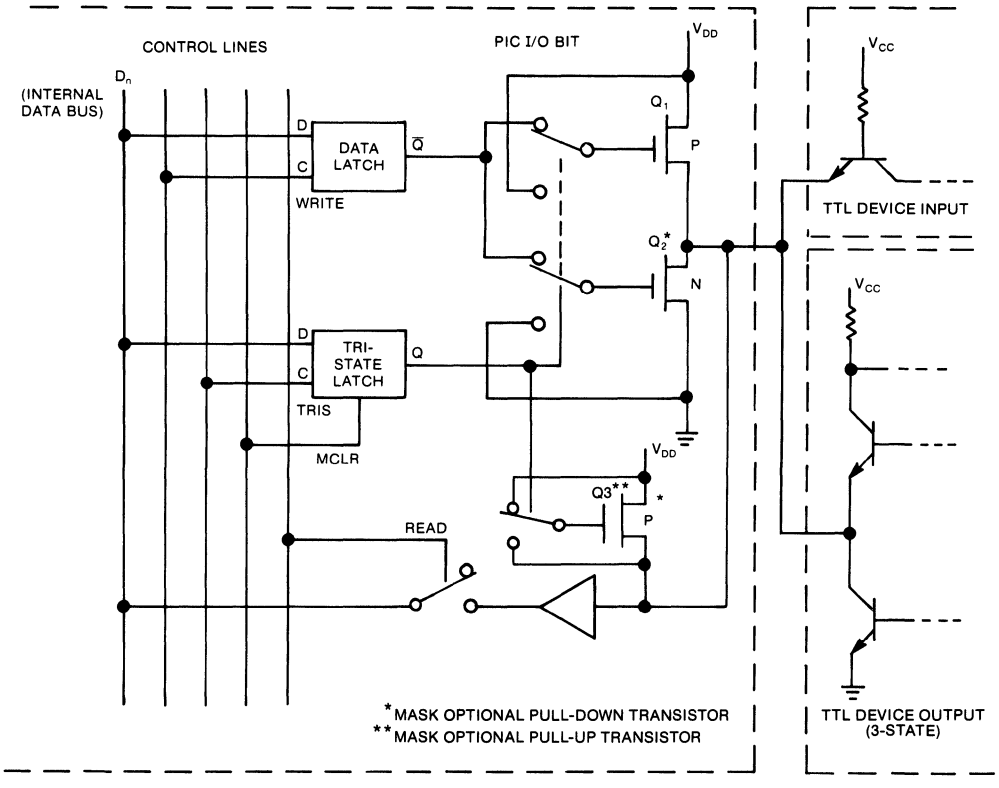
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of a tri-state TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port must first be set to the high impedance state under program control. This turns off Q_1 and Q_2 and turns on Q_3 (if present), allowing the TTL tri-state device to drive the pin.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE
(shown in active I/O state)



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation. (Note that for an output only port the latch, not the pin is read.)

Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. For use as an input port the output must be set to the high impedance state via the tri-state latch. Thus the external device inputs to the PIC circuit by forcing the input line high or low. If the input lines are not tri-stated then refer to PIC1650A programming cautions. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $^1/_5t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient Temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any Pin with Respect to V_{SS} (Note 1) ..... −0.3V to V_{DD} +0.3V
Voltage on V_{DD} with Respect to V_{SS} ..... −0.3V to +6.5V
Power Dissipation (Note 5) 300mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristics	Sym	Min	Typ†	Max	Units	Conditions
Supply Voltage	V_{DD}	2.5	—	6.0	V	
Supply Current	I_{DD}	— —	— —	2 5	mA mA	V_{DD} = 4V, All I/O pins tri-state, t_{CY} = 4 μsec V_{DD} = 6V, All I/O pins tri-state, t_{CY} = 4 μsec
Input Low Voltage	V_{IL}	V_{SS}	—	0.2V_{DD}	V	
Input High Voltage	V_{IH}	0.8V_{DD}	—	—	V	
Output High Voltage (RB0-7, RC0-7)	V_{OH}	V_{DD} −0.4 V_{DD} −0.4	— —	— —	V V	I_{SOURCE} = 0.2mA, V_{DD} = 4.75V I_{SOURCE} = 80μA, V_{DD} = 2.5V
Output Low Voltage (RB0-7, RC0-7) (Note 1)	V_{OL}	—	—	0.4	V	I_{SINK} = 0.2mA, V_{DD} = 2.5V I_{SINK} = 1.6mA, V_{DD} = 4.75V
Input Low Current (RA0-3, RC0-7) (Note 2)	I_{IL}	—	—	250	μA	V_{DD} = 6V, V_{IN} = 0.4V
Input High Current (RA0-3, RC0-7) (Note 2)	I_{IH}	2	—	—	μA	V_{IN} = V_{DD} −0.4V
Leakage Current (Note 3)	I_{LC}	−1	—	1	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$

†Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. The output pull-down transistor can be removed via a mask option to facilitate interfacing with external circuitry which has signal swings below V_{SS}. If this is the case, the maximum voltage permitted to be applied to the pin is −12V with respect to V_{DD}.
2. Current is being sourced by the internal pull-up resistors which are available as a mask option on ports RA0-3 and RC0-7. (RC0-7 have their pull-ups turned off when selected as outputs.)
3. This applies to ports RA0-3 and RC0-7 without the mask optional internal pull-up resistors, port RB0-7 and RC0-7 in the high impedance state, $\overline{RTCC}$, $\overline{MCLR}$ and OSC 1.
4. Total output sink current for all output pins (including CLK OUT) must not exceed 50mA. Total output source current must not exceed 20mA. Maximum output sink or source current for each individual output must not exceed 10mA.
5. Total power dissipation should not exceed 300mW for the package. Power dissipation is calculated as follows:
   $P_{DIS} = V_{DD} [I_{DD} - \Sigma (I_{IN} + I_{OH})] + \Sigma (V_{DD} - V_{IN}) (I_{IN}) + \Sigma (V_{DD} - V_{OH}) (I_{OH}) + \Sigma (V_{OL}) (I_{OL})$.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

Operating Temperature $T_A = 0°C$ to $+70°C$, $V_{DD} = 2.5 - 6.0V$ except as noted.

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Oscillator Frequency	f_{OSC}	25	—	1000	kHz	$V_{DD} = 2.5V$
	f_{OSC}	25	—	1250	kHz	$V_{DD} = 3.2V$
	f_{OSC}	25	—	1650	kHz	$V_{DD} = 5.0V$
	f_{OSC}	25	—	1800	kHz	$V_{DD} = 6.0V$
CLOCK OUT						
Period (Instruction Cycle Time)	t_{CY}	—	$5/f_{OSC}$	—	μs	(Note 1)
Pulse Width	t_{CLKH}	—	$1/f_{OSC}$	—	μs	
Rise/Fall Time	t_r/t_f	—	—	200	ns	1 TTL Load + 60pF $V_{DD} = 5V$
RTCC Input						
Period	t_{RT}	$t_{CY}+0.2\mu s$	—	—	—	(Notes 2 and 3)
Pulse Width (High or Low Level)	t_{pw}	500	—	—	ns	
I/O Ports						
Data Input Setup Time	t_S	—	—	$1/5t_{CY}-300$	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	—	1.6	μs	60pF + 2.2K to $0.8V_{DD}$

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$

NOTES:

1. Instruction cycle period (t_{CY}) equals five times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RTCC}$ input, CLK OUT may be directly tied to the $\overline{RTCC}$ input.
3. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows:

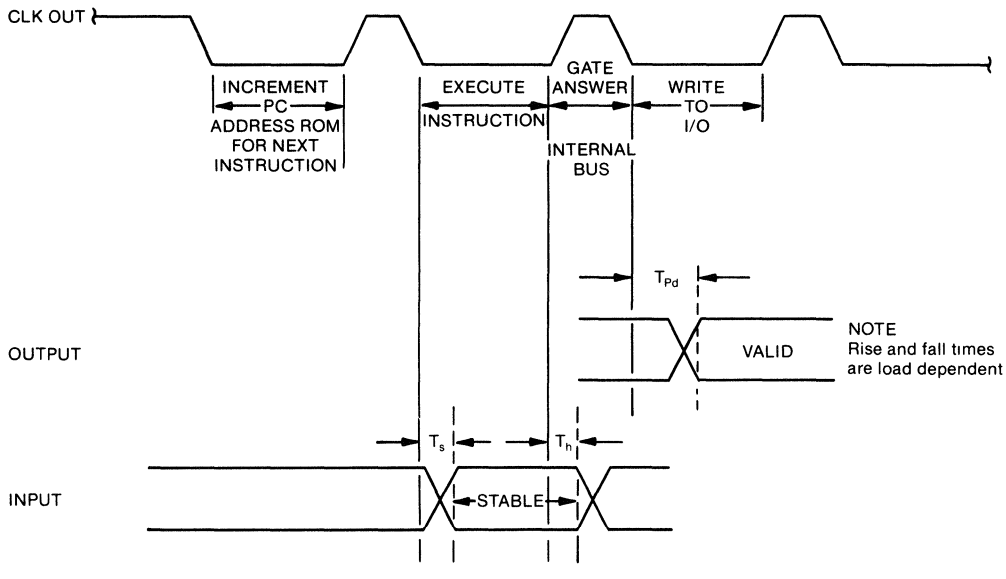
$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$$

For example:

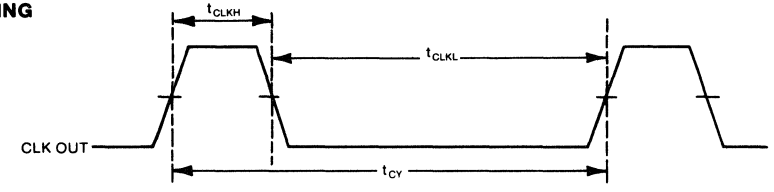
if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

MICROCOMPUTER

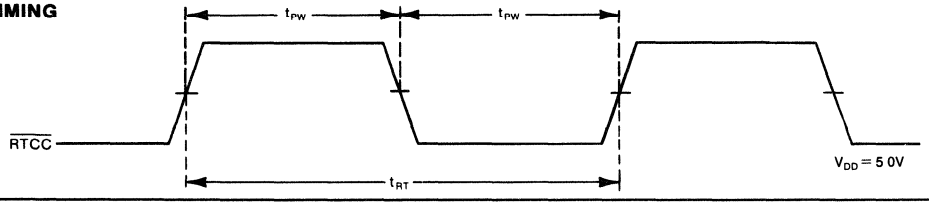
I/O TIMING



CLK OUT TIMING



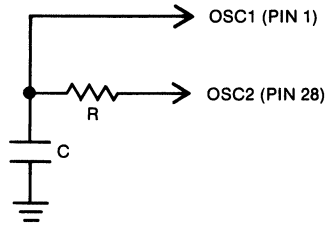
$\overline{\text{RTCC}}$ TIMING



MICROCOMPUTER

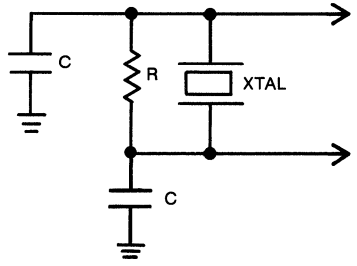
PIC16C55 OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

RC OPTION OPERATION



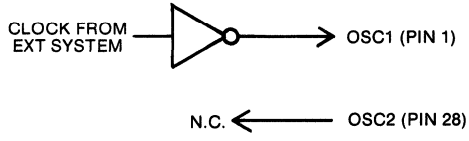
$10K \leq R \leq 1M$.
TYPICAL VALUES
$R \geq 10K$
$C \geq 100pf$

CRYSTAL INPUT OPERATION

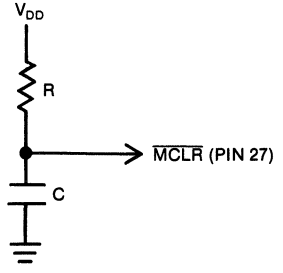


TYPICAL VALUES
R = 1M
C = 10-20pF

EXTERNAL CLOCK INPUT OPERATION



MASTER CLEAR



TYPICAL VALUES
R = 1M
C = 0.1μF

Master Clear may require up to a 75ms delay before activation after power is applied to the V_{DD} pin for a 1MHz crystal to start up. To achieve this an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function). The RC oscillator option, shown above, should start up in less time.

8 Bit Microcomputer

FEATURES

- Vectored interrupt servicing capability
- User programmable
- Intelligent controller for stand-alone applications
- 32 8-bit RAM registers
- 512 x 12-bit program ROM
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Event counter capability
- Self-contained oscillator for RC network or crystal
- Access to RAM registers inherent in instruction
- Wide power supply operating range (4.5V to 7.0V)
- Available in two temperature ranges: 0° to 70°C and −40° to 85°C
- 4 inputs, 8 outputs, 8 bi-directional I/O lines
- 3 level stack for subroutine nesting
- Same PIC instruction sets as PIC1650A or PIC1655A with the addition of RETURN (0002_8) instruction

DESCRIPTION

The PIC1656 microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit ALU.

The PIC1656 is designed for real-time control applications requiring external and internal clock-driven interrupts. The PIC1656 has 20 I/O lines organized as two 8-bit registers and the 4 LSB's of a third register.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

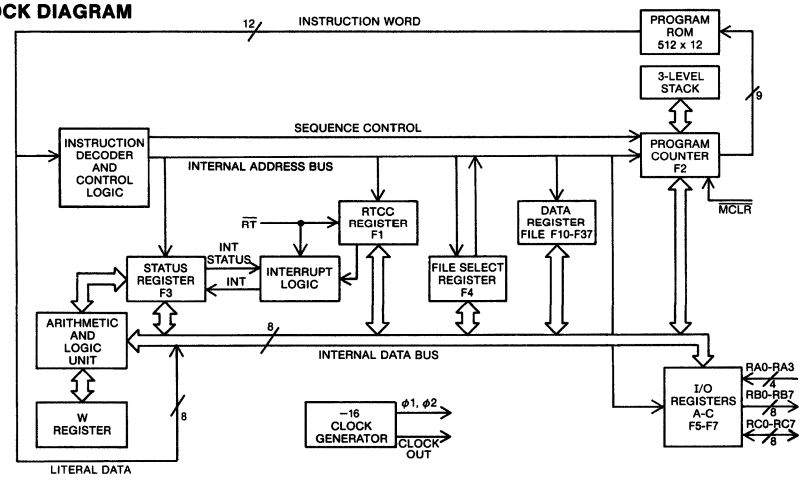
The PIC1656 is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with an external crystal ceramic resonator or LC network to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance The PIC's operation can be verified in any hardware application by using the PIC1664. The PIC1664 is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD1010 Field Demo System is available containing a PIC1664 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

MICROCOMPUTER

PIC1656 BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

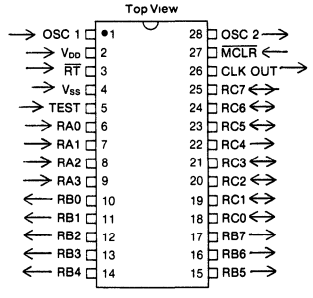
The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{MCLR}$ input on power up initializes the ROM program to address 777_8

PIN FUNCTIONS

Signal	Function
OSC1 (input), OSC2 (output)	Oscillator inputs. The oscillator frequency can be set by a crystal (if a precise frequency is required), ceramic resonator or LC network, or driven from an external source.
$\overline{RT}$ (input)	Real Time Input. Function is controlled by bits 4 and 7 of the Status Word Register (F3). A high-to-low transition of this pin will increment the RT register (event counter mode) or will initiate a vectored interrupt (external interrupt mode).
RA0-3 (input)	Dedicated input lines, read under direct control of the program. The 4 MSB's are always read as logic zeroes.
RB0-7 (output)	Dedicated output lines, user programmable under direct control of the program.
RC0-7 (input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program.
$\overline{MCLR}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch I/O registers F6 and F7 low. Also clears bits 3-7 of status register (F3).
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation.
V_{DD}	Primary Power Supply.
V_{SS}	GND.

PIN CONFIGURATION
28 LEAD DUAL IN LINE



MICROCOMPUTER

REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to the contents of W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RT}$. However, if data are being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
CNT	RTCR	IR	RTCE	IE	Z	DC	C

BIT 0: Carry (C) bit — For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.

For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

BIT 1: Digit Carry (DC) bit — For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

BIT 2: Zero (Z) bit — Set if the result of an arithmetic operation is zero.

BITS: 3-7 — Interrupt Service Flags (Cleared on $\overline{MCLR}$).

BIT 3: Interrupt Enable (IE) status bit. When set to a one, this bit enables the external interrupt to occur when and if the interrupt request (IR) status bit (bit 5) is also set. When reset to a zero, the external interrupt is disabled.

BIT 4: Real Time Clock Enable (RTCE) status bit. When set to a one, this bit enables the real-time clock/counter interrupt to occur when and if the real-time clock interrupt request (RTCR) status bit (bit 6) is also set. When reset to a zero, the interrupt is disabled.

BIT 5: Interrupt Request (IR) status bit. This bit is set by a high-to-low transition on the $\overline{RT}$ pin, generating an interrupt request. If and when the interrupt enable (IE) bit (bit 3) is also set, an interrupt will occur. This causes the current PC address to be pushed onto the stack and the processor to execute the instruction at location 760_8. The IR bit is then immediately cleared. Note that the IR bit can be set regardless of the state of the IE bit, thus requesting an interrupt which can be serviced or not at the programmer's option.

BIT 6: Real Time Clock/Counter Interrupt Request (RTCR) status bit. This bit is set when the RTCC register (File 1) transitions from a full count (377_8) to a zero count (000_8). If and when the RTCE bit is also set, an interrupt will occur. This causes the current PC address to be pushed onto the stack and the processor to execute the instruction at location 740_8. The RTCR bit is then immediately cleared. Note that the RTCR bit can be set regardless of the state of the RTCE bit, thus requesting an interrupt which can be serviced or not, at the programmer's option.

NOTE: Although the processor cannot be interrupted during an interrupt (i.e., until the RETFI instruction is executed), (an) other interrupt(s) can be requested (status bits 5 and/or 6 can be set). This will cause the processor to reinterrupt immediately upon its return from the current interrupt assuming the interrupt(s) is (are) enabled. (Pending external interrupts have priority over pending real-time clock/counter interrupts.)

BIT 7: Count Select (CNT) status bit. When CNT bit is set to a one, the RTCC register will increment on each high-to-low transition at the $\overline{RT}$ pin. If the CNT bit is sent to a zero, the RTCC register will increment at the internal clock rate (1/16 of the frequency at the OSC pins).

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	Input Register A (A0-A3). A4-A7 defined as zeroes.
F6	Output Register B (B0-B7)
F7	I/O Register (C0-C7)
F10-F37	General Purpose Registers

INTERRUPT LOGIC

The interrupt logic generates an interrupt request to the control unit to initiate a vectored interrupt. One of two possible interrupt requests (external interrupt request or RTCC interrupt request) can be generated. Only one interrupt at a time can be serviced. Nested interrupts are not possible since additional interrupts are disabled by an internal latch.

The contents of the status register indicate whether any interrupts are pending. If only one interrupt is pending, it is serviced immediately providing the interrupt is enabled (i.e., IE or RTCE is set) and the processor is not already servicing another interrupt. If both external and RTCC interrupts are pending and enabled, the external interrupt has priority. If an external interrupt is input on the $\overline{RT}$ pin while another external interrupt is being serviced, a new external interrupt request will be generated to the processor which will reinterrupt immediately upon its return from the current interrupt.

CAUTION

A return from an interrupt routine must not be executed using any other instruction but RETURN. If any other instruction is executed to restore the return address to the program counter, the interrupt logic will not be enabled. This effectively prevents any other interrupts from being serviced. If the interrupt routine contains subroutines, returns from the subroutines should be made using the RETLW instruction. If the RETURN instruction is used mistakenly, additional interrupts that occur while the first interrupt routine is in process will be enabled and can corrupt the interrupt routine in process.

STACK

A three-level stack is provided to accommodate three return addresses. One level of the stack should be reserved to store the return address of an interrupt. The other two levels provide storage for two return addresses from a nested subroutine.

NOTE: One level of the stack must always be available to accommodate an interrupt return address. When an interrupt occurs, the firmware automatically pushes the return address onto the stack. Should three subroutines be nested, the return address of the current subroutine will be destroyed. Only if the PIC1656 is not programmed for interrupts is it permissible to use all three levels of the stack for subroutines.

RTCC REGISTER

The RTCC register (F1), in conjunction with the status register, is programmable for internal clock or $\overline{RT}$ clock operation

Bit 7 of the status register, when set to a one, selects the $\overline{RT}$ pin as the clocking source and, when reset to a zero, selects the internal clock as the clocking source. When the RTCC register transitions from a count of 377_8 to a count of 000_8, bit 6 (RTCR) of the status register sets to a one, requesting a real-time clock interrupt. An interrupt to 740_8 is generated if RTCE (bit 4) is set.

The RTCC register can be preset and read under program control at any time. If the RTCC register is not used as a counter, it can be used as a general-purpose data register provided the $\overline{RT}$ pin is tied low and CNT is set to a one. (Note MCLR resets CNT.)

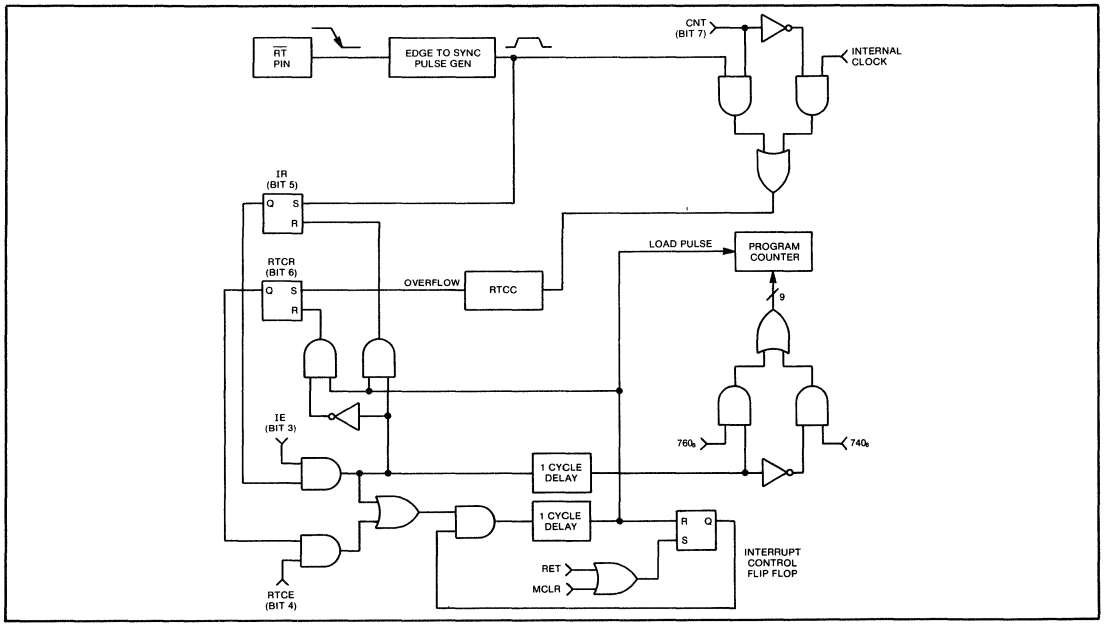
I/O REGISTERS (F5-F7)

The I/O interface consists of three I/O registers controlling 20 input/output lines. These registers (A, B, and C) are addressable as F5 through F7, respectively. Register A (F5) controls four dedicated non-latching input lines Register B (F6) controls eight dedicated latched output lines, and register C (F7) controls eight bidirectional input/output lines. As with the PIC1655A, register file F-10, which in the PIC1650A was I/O register D, is an additional general purpose register in the PIC1656.

CLOCK GENERATOR

The internal timing rate of the PIC1656 is controlled by an external control source connected across two input pins, OSC 1 and OSC 2. This may be established by an RC network (RC control) connected across the OSC 1 and OSC 2 pins or by a non-buffered external crystal connected across the OSC 1 and OSC 2 pins.

The PIC1656 clock generator divides the frequency at the OSC 1 and OSC 2 pins by 16 to derive the internal machine cycle rate. A 4MHz frequency at the OSC 1 and OSC 2 pins will result in a 4μs (0.25MHz) instruction cycle. This enables the use of a low-cost standard 3.58MHz crystal to provide a machine cycle of approximately 4μs. Figure 14 illustrates both the crystal and RC input configurations to the OSC 1 and OSC 2 input pins.



Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

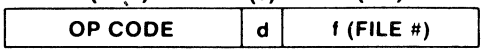
For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 4MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

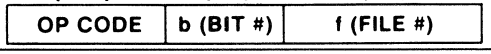
BYTE-ORIENTED FILE REGISTER OPERATIONS



For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

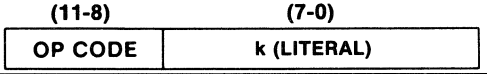
Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇋f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 010 (0002)	Return from Interrupt	RETURN	—	Stack→PC	None
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.
3. See notes on input only and output only ports (F5 and F6, respectively).

SUPPLEMENTAL INSTRUCTION SET SUMMARY

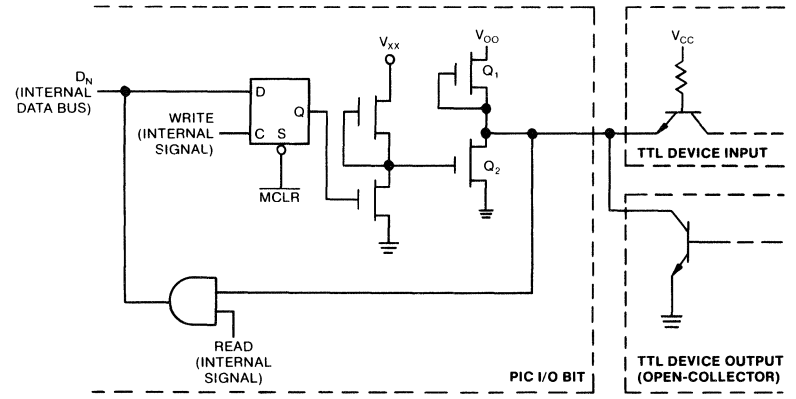
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Input Only Port: (Port RA)

The input only port of the PIC1656 consists of the four LSB's of F5 (port RA). An internal pull-up device is provided so that external pull-ups on open collector logic are unnecessary. The four MSB's of this port are always read as zeroes. Output operations to F5 are not defined. Note that the BTFSC and BTFSS instructions are input only operations and so can be used with F5. Also, file register instructions which leave the results in W can be used.

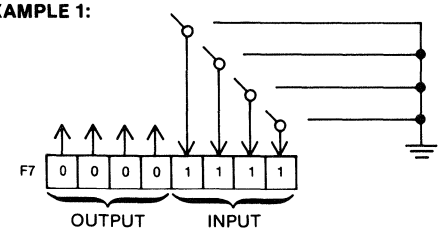
Output Only Port: (Port RB)

The output only port of the PIC1656 consists of F6 (port RB). This port contains no input circuitry and is therefore not capable of instructions requiring an input followed by an output operation. The only instructions which can validly use F6 are MOVWF and CLRF.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



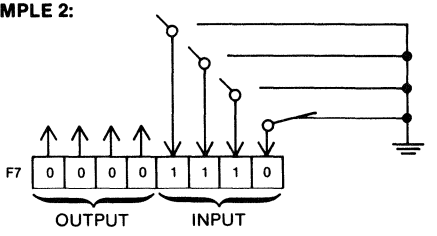
What is thought to be happening:

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... −0.3V to +12.0V
Power Dissipation (Note 1) 1000mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS/PIC1656

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Primary Supply Current	I_{DD}	—	30	55	mA	All I/O pins high
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RT}$ & OSC1)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage (RT & OSC1)	V_{IH2}	V_{DD}−1	—	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$)	V_{ILH}	V_{DD}−1	2.6	V_{DD}	V	
Output High Voltage	V_{OH}	2.4 3.5	— —	V_{DD} V_{DD}	V V	I_{OH} = −100μA (Note 2) I_{OH} = 0
Output Low Voltage (I/O only)	V_{OL1}	— —	— —	0.45 0.90	V V	I_{OL} = 1.6mA, V_{DD} = 4.5V I_{OL} = 5.0mA, V_{DD} = 4.5V (Note 3)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	I_{OL} = 1.6mA (Note 3)
Input Leakage Current ($\overline{MCLR}$, $\overline{RT}$ & OSC1)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain I/O pins)	I_{OLC}	—	—	10	μA	$V_{SS} \leq V_{PIN} \leq 10V$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	−1.4	mA	V_{IH} = 2.4V

†Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

DC CHARACTERISTICS/PIC1656I

Operating Temperature $T_A = -40°C$ to $+85°C$

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Primary Supply Current	I_{DD}	—	30	60	mA	All I/O pins high
Input Low Voltage	V_{IL}	−0.2	—	0.7	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RT}$ & OSC1)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage ($\overline{RT}$ & OSC1)	V_{IH2}	$V_{DD}-1$	—	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$)	V_{ILH}	$V_{DD}-1$	2.6	V_{DD}	V	
Output High Voltage	V_{OH}	2.4 3.5	— —	V_{DD} V_{DD}	V V	$I_{OH} = -100\mu A$ (Note 2) $I_{OH} = 0$
Output Low Voltage (I/O only)	V_{OL1}	— —	— —	0.45 0.90	V V	$I_{OL} = 1.6mA$, $V_{DD} = 4.5V$ $I_{OL} = 5.0mA$, $V_{DD} = 4.5V$ (Note 3)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	$I_{OL} = 1.6mA$ (Note 3)
Input Leakage Current ($\overline{MCLR}$, $\overline{RT}$ & OSC1)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Output Leakage Current (open drain I/O pins)	I_{OLC}	—	—	10	μA	$V_{SS} \leq V_{PIN} \leq 10V$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.8	mA	$V_{IL} = 0.4V$ internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	−1.8	mA	$V_{IH} = 2.4V$

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD}) + \Sigma\,(V_{DD} - V_{IL})\,(|I_{IL}|) + \Sigma\,(V_{DD} - V_{OH})\,(|I_{OH}|) + \Sigma\,(V_{OL})\,(I_{OL})$.
   The term I/O refers to all interface pins; Input, Output or I/O.
2. Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS/PIC1656, PIC1656I

Operating Temperature $T_A = 0°C$ to $+70°C$ (PIC1656), $T_A = -40°C$ to $+85°C$ (PIC1656I)

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.8MHz—4.0MHz external time base (Note 1)
$\overline{RT}$ Input						
Period	t_{RT}	$t_{CY}+0.2\mu s$	—	—	—	
High Pulse Width	t_{RTH}	$\frac{1}{2}t_{RT}$	—	—	—	
Low Pulse Width	t_{RTL}	$\frac{1}{2}t_{RT}$	—	—	—	(Notes 2 and 3)
I/O Ports						
Data Input Setup Time	t_S	—	—	$\frac{1}{4}t_{CY}-125$	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	600	1000	ns	Capacitive load = 50pF
OSC 1 Input						
External Input Impedance High	R_{OSCH}	—	10^6	—	Ω	$V_{OSC} = V_{DD} = 5V$ } Applies to external
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	$V_{OSC} = 0.4V$ } OSC drive only.

NOTES:

1. Instruction cycle period (t_{CY}) equals sixteen times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RT}$ input, CLK OUT may be directly tied to the $\overline{RT}$ input.
3. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows: $f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$
   For example: if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

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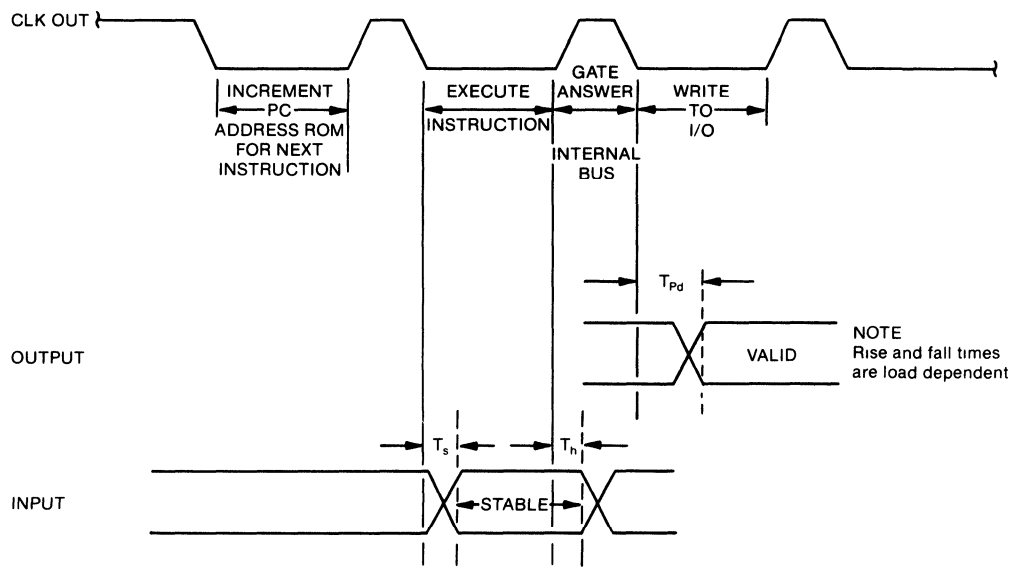
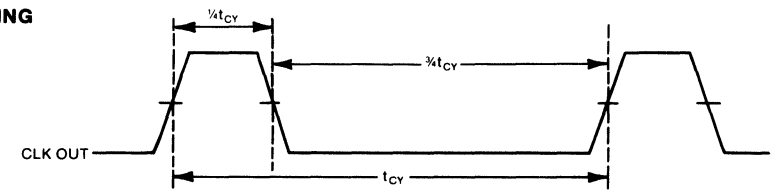
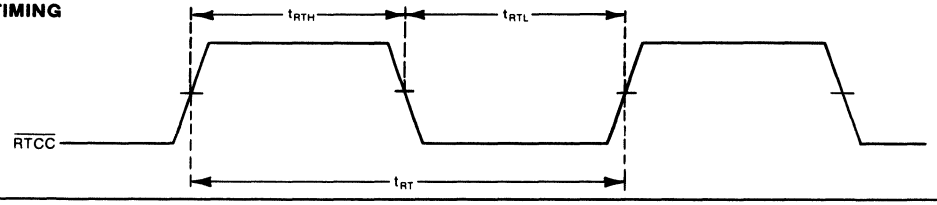
I/O TIMING



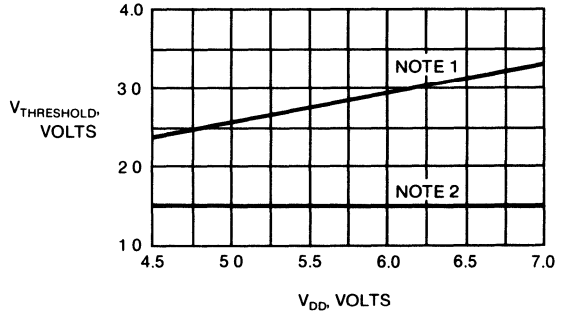
CLK OUT TIMING



$\overline{\text{RTCC}}$ TIMING



SCHMITT TRIGGER CHARACTERISTICS ($\overline{\text{RTCC}}$, $\overline{\text{MCLR}}$ and OSC PINS) $T_A = 25°C$ (TYPICAL)

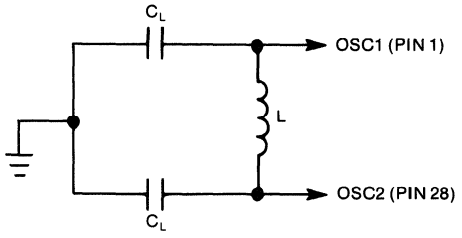


NOTES:
1. Low-to-High Threshold Voltage (V_{TLH}).
2. High-to-Low Threshold Voltage (V_{THL}).

MICROCOMPUTER

PIC1656 OSCILLATOR OPTIONS (Typical Circuits)

LC INPUT OPERATION

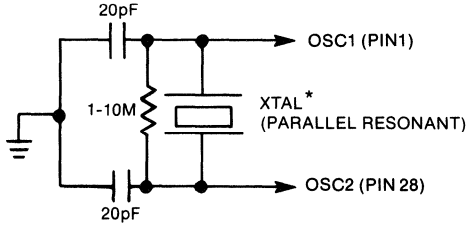


$$f_{OSC} \approx \frac{1}{2\pi \sqrt{L\,(C_L + C_{INT})}},$$

where $C_{INT} = 10pF$.

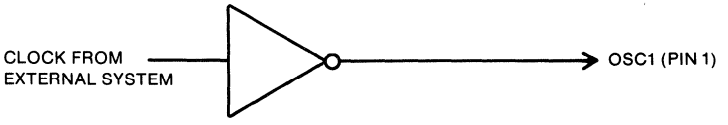
Typical values for 4MHz operation.
$L = 70\mu H$
$C_L = 10pF$

CRYSTAL INPUT OPERATION



* or ceramic resonator,

EXTERNAL CLOCK INPUT OPERATION



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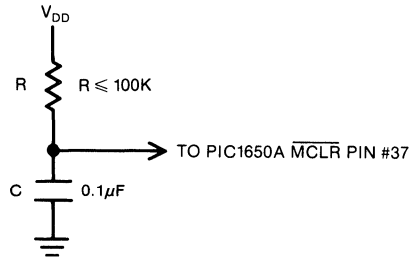
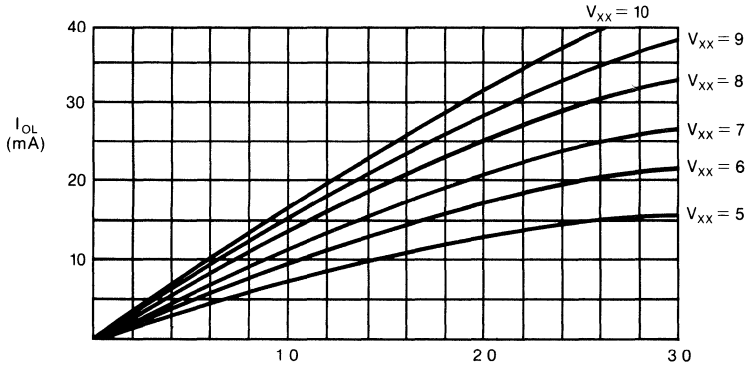
MASTER CLEAR (TYPICAL CIRCUIT)



Master Clear requires >1.0ms delay before activation after power is applied to the V_{DD} pin, for the oscillator to start up To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

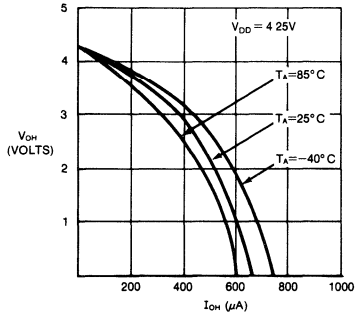
OUTPUT SINK CURRENT GRAPH



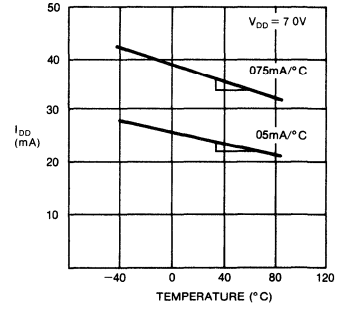
I_{OL} vs. V_{OL} TYP @ 25°C

The Output Sink Current is dependent on the V_{XX} supply and the output load This chart shows the typical curves used to express the output drive capability

V_{OH} VS I_{OH} (I/O PORTS) (TYPICAL)



POWER SUPPLY CURRENT VS TEMPERATURE (TYPICAL LIMITS)



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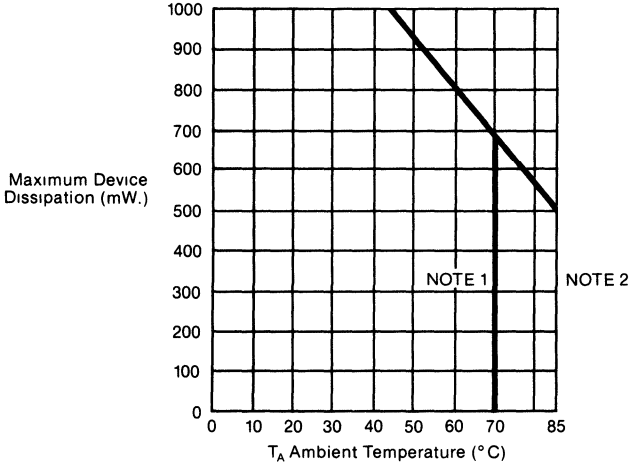
POWER DISSIPATION DERATING GRAPH



NOTES:
1. 70° C is the maximum operating temperature for standard parts.
2. 85° C is the maximum operating temperature for "I" suffix parts.

PIC1656 EMULATION CAUTIONS

When emulating a PIC1656 using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1656 mode. (Refer to PICES II Manual). The PIC1664 contained within the module should have the MODE pin #22 set to a low state.

1. This causes the $\overline{\text{MCLR}}$ to register F5 high and register F6, and F7 low.
2. The OSC becomes a two input clock (pins 1 & 28).
3. The interrupt system becomes enabled and the RT always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are used for interrupt service.

B. Three levels of stack can be used within the program. If interrupts are used, allow one level of the stack for interrupt servicing.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 28 pin socket for the module plug.

E. Make sure that during an actual application that the MCLR input swings from a low to high level a minimum of 1 msec after the supply voltage is applied.

F. The cable length and internal variations may cause some parameter values to differ between the PICES II module and a production PIC1656.

8 Bit Microcomputer

FEATURES

- 1024 x 13-bit Program ROM
- 64 x 8-bit RAM (16 special purpose registers)
- Arithmetic Logic Unit
- Sophisticated interrupt structure
- 6 level pushdown stack
- Versatile self contained oscillator
- 2.0μs instruction execution time
- Wide power supply operating range (4.5-5.5 volts)
- 4 sets of 8 user defined TTL compatible I/O lines
- Available in two temperature ranges: 0°C to 70°C and −40°C to 85°C.

DESCRIPTION

The PIC1670 microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and system control functions can be done at the same time due to the power of the 8-bit CPU.

The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 13-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1670 is fabricated with N-Channel Silicon Gate technology resulting in a high performance product. Only a single wide range power supply is required for operation. An on-chip oscillator provides the operating clock with either an external crystal or RC network to establish the frequency. Inputs and outputs are TTL-compatible, with open-drain option available.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC1665. The PIC1665 is a ROM-less PIC1670 microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD 1020 Field Demo System is available containing a PIC1665 with sockets for erasable PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

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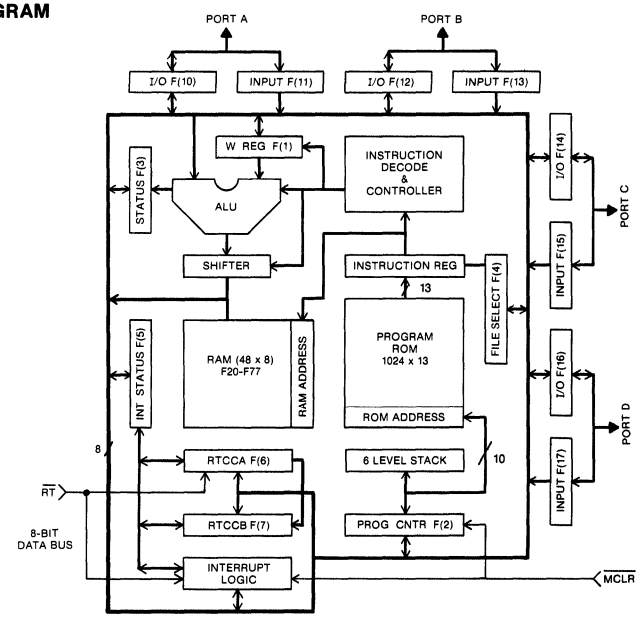
PIC1670 BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC1670 microcomputer is based on a register file concept with simple yet powerful instruction commands designed to optimize the code for bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the functional blocks of the PIC1670 are connected by an 8-bit bidirectional bus: the 64 8-bit registers of which the first 16 are special purpose, an Arithmetic Logic Unit, and a user defined program ROM composed of 1024 x 13 words. The register file is divided into two functional groups: operational registers and general purpose registers. The first sixteen are the operational registers and they include the Real Time Clock Counter A and B, four I/O registers, two Status registers, a Program Counter and a File Select Register. The general purpose registers are used for data and control information under command of the instructions.

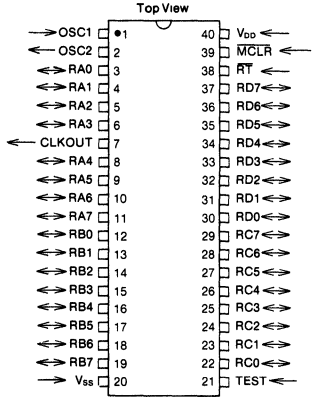
The Arithmetic Logic Unit contains one temporary working register (W Register), an adder, and hardware for decimal adjust. Manipulation between data in the working register and any other register can be performed.

The Program ROM contains the user defined application program and is supported by an instruction decoder and instruction register. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. The Program Counter is modified by bit test, jump, call or branch instructions and the lower 8-bits can be modified for computed addresses by file register instructions. In addition, an on-chip six level stack is employed to push and pull the contents of the program counter. This provides easy to use subroutine nesting. Activating the MCLR input on power-up initializes the ROM program to address 1777_8.

PIN FUNCTIONS

Signal	Function
OSC1 (input), OSC2 (output)	Oscillator pins. The on-board oscillator can be driven by an external crystal, ceramic resonator or LC network, or an external clock via these pins.
$\overline{RT}$ (input)	Real Time Input. Negative transitions on this pin increment the RTCC (F6) register. This pin can also be used for an interrupt input. This pin uses a Schmitt trigger input. There is no internal active pull-up device.
RA0-7, RB0-7, RC0-7, RD0-7	User programmable input/output lines. These lines can be used as inputs and/or outputs and are under direct control of the program.
$\overline{MCLR}$ (Input)	Master Clear. Used to initialize the internal ROM program to address 1777_8, latch all I/O registers high, and disables the interrupts. This pin uses a Schmitt trigger input. There is no internal active pull-up device.
TEST	Test pin. This pin is used for testing purposes only. It must be grounded for normal operation.
V_{DD}	Power supply pin.
V_{SS}	Ground pin.
CLKOUT	Clock Output. A signal derived from the internal oscillator. May be used by external circuitry to synchronize with PIC1670 timing.

PIN CONFIGURATION
40 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physical register. F0 calls for contents of the FSR (F4) to be used to select a file register. F4 is used as an indirect address pointer.
F1	W Register — The working register
F2	Program Counter — Points to the next program ROM address to be executed.
F3	Arithmetic Status Register 7 6 5 4 3 2 1 0 0 X A9 A8 OV Z DC C Bit 0 (C) — Bit 0 is the carry flag, and is usually the carry from the A.L.U., also used as a borrow in subtract instructions. Bit 1 (DC) — Bit 1 is the half carry (decimal carry) and is used to indicate a carry from bit 3 in the A.L.U as the result of an addition (byte). This bit is used in the decimal adjust instruction to allow B.C.D. decimal addition Bit 2 (Z) — Bit 2 is the zero flag and is set to a one if the results of the previous operation was identically zero. Bit 3 (OV) — Bit 3 is the overflow flag, and is set to a one by operations which cause a signed two's complement arithmetic overflow. The bit is set when the carry from the MSB in the A.L.U. is opposite to the carry from the MSB-1 bit. Bit 4 (A8) — Bit 4 is the 9th bit of the program counter. This bit is a read only bit Bit 5 (A9) — Bit 5 is the 10th bit of the program counter. This bit is a read only bit.
F4	File Select Register — The FSR is used in generating effective file register addresses under program control.
F5	Interrupt Status Register X CNTE A/B CNTS RTCIR XIR RTCIE XIE — Used to control interrupts and registers F6 and F7.
F6,F7	RTCCA and RTCCB — Real Time Clock Counters A & B respectively can be configured as a single 16 bit counter, an 8 bit counter and an 8 bit general purpose register, or two general purpose registers when no external counting is required. The RTCC registers can be loaded and read by the program, as well as count negative transitions on the $\overline{RT}$ pin or count at 1/8 the frequency of the oscillator. If data are being stored into RTCCA simultaneous with a negative transition on the RT pin (and CNTE=1 and CNTS=1), RTCCA will contain the new stored value and the external transition will be ignored by the microcomputer. (See the section "Real Time Clock Interrupt" for further details about the RTCC.)
F10,11	I/O Port A
F12,13	I/O Port B
F14,15	I/O Port C
F16,17	I/O Port D
F20,77	General Purpose Registers—Used for temporary and general purpose storage during program execution time.

NOTE: F10, 12, 14 & 16 are the I/O registers and F11, 13, 15 & 17 are used for reading the actual pin levels.

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Basic Instruction Set Summary

Each PIC instruction is a 13-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 4MHz the instruction execution time is 2.0 μsec unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 4.0 μsec.

BYTE ORIENTED FILE REGISTER OPERATIONS

(12-7)	(6)	(5-0)
OP CODE	d	f (FILE #)

Instruction—Binary (Octal)	Name	Mnemonic,	Operands	Operation	Status Affected
0 0 0 0 0 0 0 0 0 1 0 0 (00004)	Decimal adjust W	DAW	—	(Note 1)	C
0 0 0 0 0 1 f f f f f f (00100)	Move W to file	MOVWF	f	W→f	—
0 0 0 0 0 0 1 d f f f f f f (00200)	Subtract W from file w/borrow	SUBBWF	f,d	f+$\overline{W}$+c →d	OV,C,DC,Z
0 0 0 1 0 d f f f f f f (00400)	Subtract W from file	SUBWF	f,d	f+$\overline{W}$ + 1→d	OV,C,DC,Z
0 0 0 1 1 d f f f f f f (00600)	Decrement file	DECF	f,d	f - 1→d	OV,C,DC,Z
0 0 1 0 0 d f f f f f f (01000)	Inclusive or W with file	IORWF	f,d	WVf→d	Z
0 0 1 0 1 d f f f f f f (01200)	And W with file	ANDWF	f,d	W•f→d	Z
0 0 1 1 0 d f f f f f f (01400)	Exclusive OR W with file	XORWF	f,d	W⊕f→d	Z
0 0 1 1 1 d f f f f f f (01600)	Add W with file	ADDWF	f,d	W+f→d	OV,C,DC,Z
0 1 0 0 0 d f f f f f f (02000)	Add W to file with carry	ADCWF	f,d	W+f+c→d	OV,C,DC,Z
0 1 0 0 1 d f f f f f f (02200)	Complement file	COMPF	f d	$\overline{f}$→d	Z
0 1 0 1 0 d f f f f f f (02400)	Increment file	INCF	f,d	f+1→d	OV,C,DC,Z
0 1 0 1 1 d f f f f f f (02600)	Decrement file, skip if zero	DECFSZ	f,d	f - 1→ d, skip if zero	—
0 1 1 0 0 d f f f f f f (03000)	Rotate file right thru carry	RRCF	f,d	f(n)→d(n−1), c→d(7), f(0)→c	C
0 1 1 0 1 d f f f f f f (03200)	Rotate file left thru carry	RLCF	f,d	f(n)→d(n+1), c→d(0), f(7)→c	C
0 1 1 1 0 d f f f f f f (03400)	Swap upper and lower nibble of file	SWAPF	f,d	f(0-3)⇌(4-7)→d	—
0 1 1 1 1 d f f f f f f (03600)	Increment file, skip if zero	INCFSZ	f d	f+1→d, skip if zero	—

(12-6)	(5-0)
OP CODE	f (FILE #)

Instruction—Binary (Octal)	Name	Mnemonic,	Operands	Operation	Status Affected
1 0 0 0 0 0 0 f f f f f f (10000)	Move file to W	MOVFW	f	f→W	Z
1 0 0 0 0 0 1 f f f f f f (10100)	Clear file	CLRF	f	0→f	Z
1 0 0 0 0 1 0 f f f f f f (10200)	Rotate file right/no carry	RRNCF	f	f(n)→d(n−1), f(0), →f(7)	—
1 0 0 0 0 1 1 f f f f f f (10300)	Rotate file left/no carry	RLNCF	f	f(n)→d(n+1), f(7), →f(0)	—
1 0 0 0 1 0 0 f f f f f f (10400)	Compare file to W, skip if F < W	CPFSLT	f	f - W, Skip if C = 0	—
1 0 0 0 1 0 1 f f f f f f (10500)	Compare file to W, skip if F = W	CPFSEQ	f	f - W, Skip if $\overline{Z}$ = 1	—
1 0 0 0 1 1 0 f f f f f f (10600)	Compare file to W, skip if F > W	CPFSGT	f	f - W, Skip if $\overline{Z}$ • C = 1	—
1 0 0 0 1 1 1 f f f f f f (10700)	Move file to itself	TESTF	—	f→f	Z

BIT ORIENTED FILE REGISTER OPERATIONS

(12-9)	(8-6)	(5-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction—Binary (Octal)	Name	Mnemonic,	Operands	Operation	Status Affected
0 1 0 0 b b b f f f f f f (04000)	Bit clear file	BCF	f,b	0→f(b)	—
0 1 0 1 b b b f f f f f f (05000)	Bit set file	BSF	f,b	1→f(b)	—
0 1 1 0 b b b f f f f f f (06000)	Bit test skip if clear	BTFSC	f,b	Bit Test f(b) skip if clear	—
0 1 1 1 b b b f f f f f f (07000)	Bit test, skip if set	BTFSS	f b	Bit Test f(b) skip if set	—

LITERAL AND CONTROL OPERATIONS

(12-8)	(7-0)
OP CODE	k (LITERAL)

Instruction—Binary (Octal)	Name	Mnemonic,	Operands	Operation	Status Affected
0 0 0 0 0 0 0 0 0 0 0 0 (00000)	No Operation	NOP	—	—	—
0 0 0 0 0 0 0 0 0 0 0 1 (00001)	Halt in PIC1665	HALT	—	—	—
0 0 0 0 0 0 0 0 0 1 0 (00002)	Return from Interrupt	RETFI	—	Stack → PC	—
0 0 0 0 0 0 0 0 0 1 1 (00003)	Return from Subroutine	RETFS	—	Stack → PC	—
1 0 0 1 0 k k k k k k k k (11000)	Move Literal to W	MOVLW	k	k→W	—
1 0 0 1 1 k k k k k k k k (11400)	Add Literal to W	ADDLW	k	k+W→W	OV,C,DC,Z
1 0 1 0 0 k k k k k k k k (12000)	Inclusive OR Literal to W	IORLW	k	kVW→W	Z
1 0 1 0 1 k k k k k k k k (12400)	And Literal and W	ANDLW	k	k•W→W	Z
1 0 1 1 0 k k k k k k k k (13000)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z
1 0 1 1 1 k k k k k k k k (13400)	Return and load literal in W	RETLW	k	k→W, Stack →PC	—

(12-10)	(9-0)
OP CODE	k (LITERAL)

Instruction—Binary (Octal)	Name	Mnemonic,	Operands	Operation	Status Affected
1 1 0 k k k k k k k k k (14000)	Go to address	GOTO	k	k→PC	—
1 1 1 k k k k k k k k k (16000)	Call Subroutine	CALL	k	PC+1→Stack, k→PC	—

NOTE:
DAW Decimal Adjust W
This instruction adjusts the eight bit number in the W register to form two valid BCD (binary coded decimal) digits, one in the lower and one in the upper nibble. (The results will only be meaningful if the number in W to be adjusted is the result of adding together two valid two digit BCD numbers.)

The adjustment obeys the following two step algorithm.
1 If the lower nibble is greater than 9 or the digit carry flag (DC) is set, 06 is added to the W register.
2 Then, if the upper nibble is greater than 9 or the carry from the original or step 1 addition is set, 60 is added to the W register The carry bit is set if there is a carry from the original, step 1 or step 2 addition.

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INTERRUPT SYSTEM

The interrupt system of the PIC1670 is comprised of an external interrupt and a real-time clock counter interrupt. These have different interrupt vectors, enable bits and status bits. Both interrupts are controlled by the status register (F5)** shown below.

NOT USED	CNTE	A/B	CNTS	RTCIR	XIR	RTCIE	XIE
7*	6	5	4	3	2	1	0

*Bit 7 is unused and is read as zero.

**Register 5 will power up to all zeroes.

EXTERNAL INTERRUPT

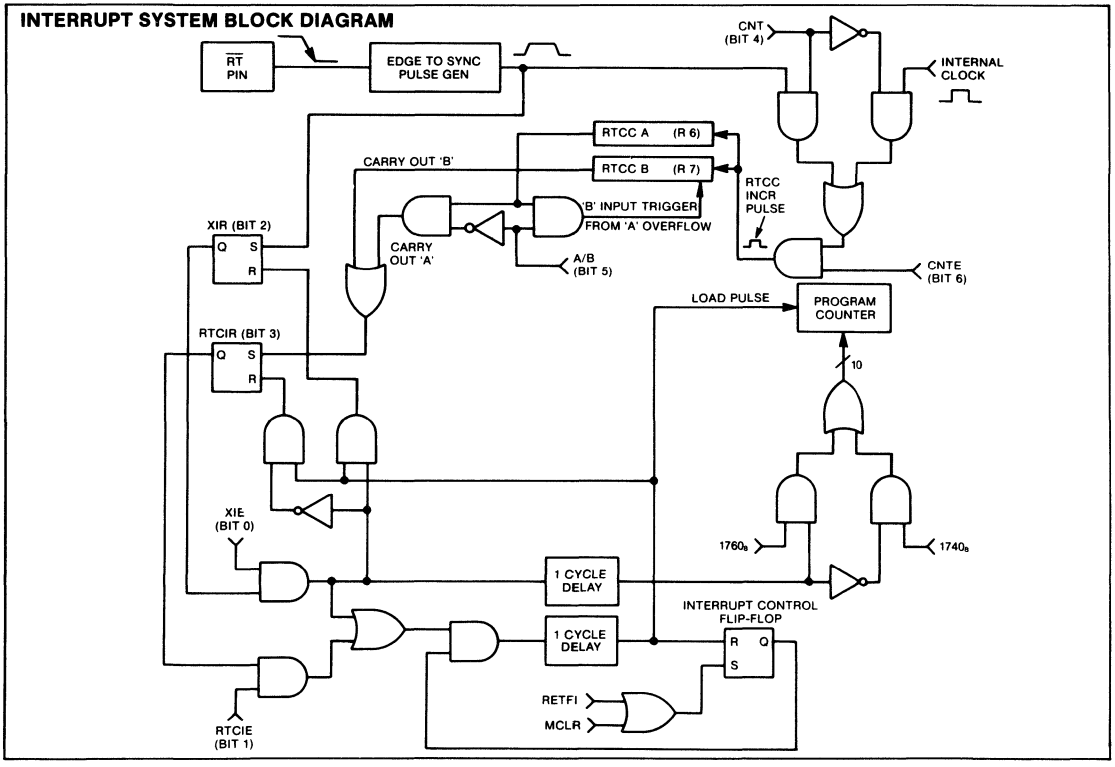
On any high to low transition of the $\overline{RT}$ pin the external interrupt request (XIR) bit will be set. This request will be serviced if the external interrupt enable (XIE) bit is set or if it is set at a later point in the program. The latter allows the processor to store a request (without interrupting) while a critical timing routine is being executed. Once external interrupt service is initiated, the processor will clear the XIR bit, delay one cycle (to execute the current instruction), then push the current program counter onto the stack and execute the instruction at location 1760_8. It takes three to four instruction cycles from the transition on the $\overline{RT}$ pin until the instruction at 1760_8 is executed. No new interrupts can be serviced until a return from interrupt (RETFI) instruction has been executed.

REAL-TIME CLOCK INTERRUPT

The real-time clock counter (RTCCA & RTCCB, file registers F6 and F7) have a similar mechanism of interrupt service. The RTCCA register will increment if the count enable (CNTE) bit is set. If this bit is not set the RTCCA & RTCCB will maintain their present contents and can therefore be used as general purpose RAM registers. The count source (CNTS) bit selects the clocking source for RTCCA. If CNTS is cleared to a '0', then RTCCA will use the internal instruction clock and increment at 1/8 the frequency present on the OSC pins. If CNTS is set to a '1', then RTCCA will increment on each high to low transition of the RT pin. RTCCB can only be incremented when RTCCA makes a transition from 377_8 to 0 and the A/B status bit is set. This condition links the two eight bit registers together to form one sixteen bit counter. An interrupt request under these conditions will occur when the combined registers make a transition from 177777_8 to 0. If, however, the A/B bit is not set, then RTCCA will be the only incrementing register and an interrupt request will occur when RTCCA makes a transition from 377_8 to 0. (In this setup the RTCCB register will not increment and can be used as a general purpose RAM register.) Once a request has come from the real-time clock counter, the real-time clock interrupt request (RTCIR) bit will be set. At this point, the request can either be serviced immediately if the real-time clock interrupt enable (RTCIE) bit is set or be stored if RTCIE is not set. The latter allows the processor to store a real-time clock interrupt while a critical timing routine is being executed. Once interrupt service is initiated, the processor will clear the RTCIR bit, delay one cycle (to execute the current instruction), then push the present program counter onto the stack and execute the instruction at location 1740_8 It takes three instruction cycles from when the RTCC (A or B) overflows until the instruction of 1740 is executed. No new interrupts can be serviced until a RETFI instruction has been executed.

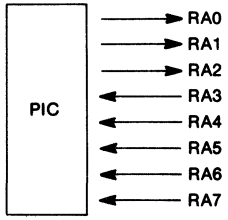
The RETFI instruction (00002_8) must be used to return from any interrupt service routine if any pending interrupts are to be serviced. External interrupts have priority over RTCC driven interrupt in the event both types occur simultaneously. Interrupts cannot be nested but will be serviced sequentially. The existence of any pending interrupts can be tested via the state of the XIR (bit 2) and RTCIR (bit 3) in the status word F5.

INTERRUPT SYSTEM BLOCK DIAGRAM



INPUT/OUTPUT CAPABILITY

The PIC1670 provides four complete quasi-bidirectional input/output ports. A simplified schematic of an I/O pin is shown below. The ports occupy address locations in the register file space of the PIC1670. Thus, any instruction that can operate on a general purpose register can operate on an I/O port. Two locations in the register file space are allocated for each I/O port. Port RA0-7 is addressable as either F10 or F11. Port RB0-7 is addressable as either F12 or F13. Port RC0-7 is addressable as either F14 or F15 and Port RD0-7 is addressable as either F16 or F17. AnI/O port READ on its odd-numbered location will interrogate the chip pins while an I/O port READ on its even-numbered location will interrogate the internal latch in that I/O port. This simplifies programming in cases where a portion of a single port is used for inputting only, while the remainder is used for outputing as illustrated in the following example.



Here, the low 3 bits of port RA are used as output-only, while the high 5 bits are used as input-only. During power on reset ($\overline{MCLR}$ low), the latches in the I/O ports will be set high, turning off all pull down transistors as represented by Q_2 in Figure 1. During program execution if we wish to interrogate an input pin, then, for example,

```
BTFSS 11,6
```

will test pin RA6 and skip the next instruction if that pin is set. If we wish to modify a single output, then, for example,

```
BCF 10,2
```

will force RA2 to zero because its internal latch will be cleared to zero. This will turn on Q_2 and pull the pin to zero.

The way this instruction operates internally is the CPU reads file 10 into the A.L.U., modifies the bit and re-outputs the data to file 10. If the pins were read instead, any input which was grounded externally would cause a zero to be read on that bit. When the CPU re-outputted the data to the file, that bit would be cleared to zero, no longer useful as an input until set high again.

During program execution, the latches in bits 3-7 should remain in the high state. This will keep Q_2 off, allowing external circuitry full control of pins RA3-RA7, which are being used here as input.

BIDIRECTIONAL INPUT-OUTPUT PORT

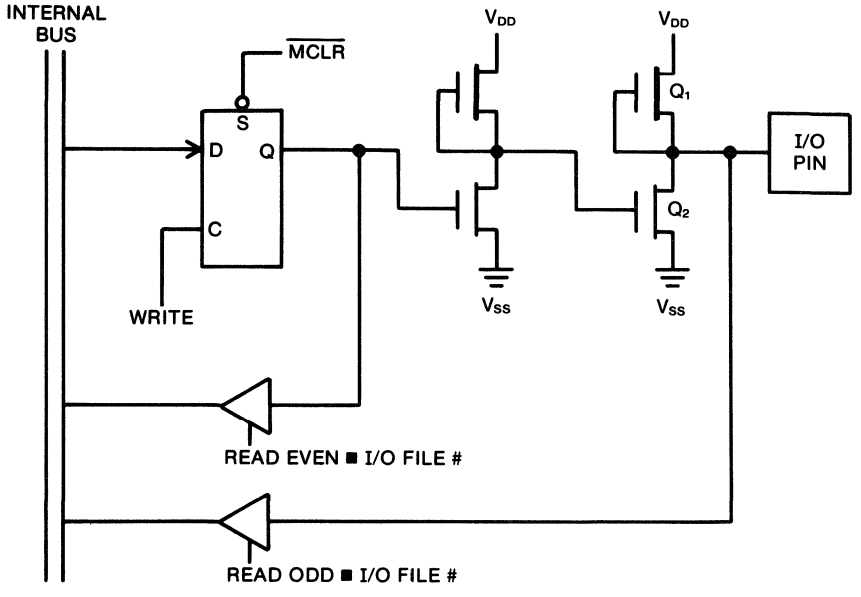


Figure 1

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient Temperature Under Bias .....−40°C to +85°C
Storage Temperature .....−55°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... −0.3V to +10.0V
Power Dissipation 1000mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	5.5	V	
Primary Supply Current	I_{DD}	—	—	100	mA	All I/O pins high
Input Low Voltage (except $\overline{MCLR}$ & $\overline{RT}$)	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RT}$, OSC1)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RT}$ OSC1)	V_{IH2}	V_{DD}−1	—	V_{DD}	V	
Output High Voltage	V_{OH}	2 4	—	V_{DD}	V	I_{OH} = −100μA provided by internal pullups (Note 2)
Output Low Voltage (I/O and CLK OUT)	V_{OL}	—	—	0.45	V	I_{OL} = 1 6mA
Input Leakage Current ($\overline{MCLR}$, $\overline{RT}$,OSC1)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−2.0	mA	V_{IL} = 0.4V, internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	—	mA	V_{IH} = 2.4V

†Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:
1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
2. Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total I_{OL} for all output pin (I/O ports plus CLK OUT) must not exceed 175mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

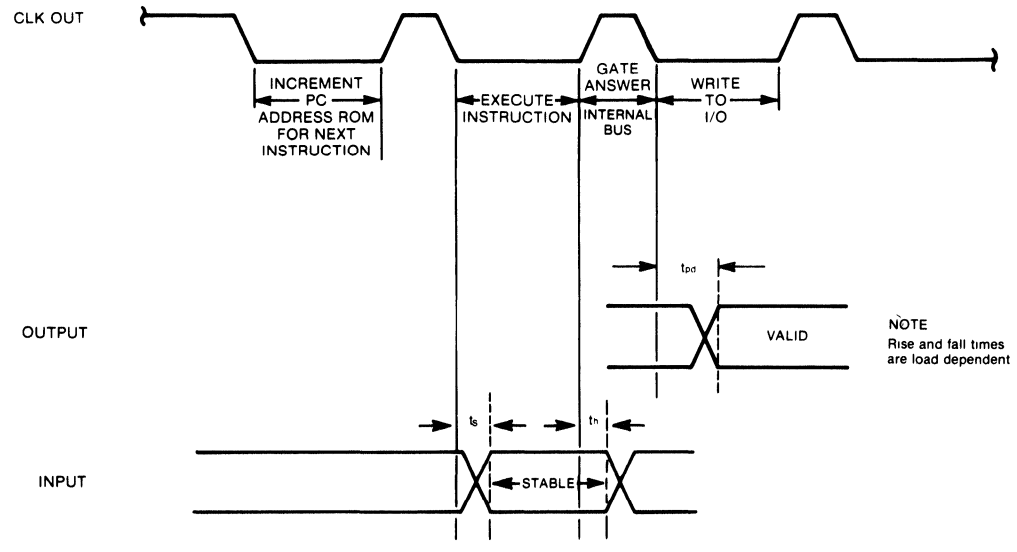
Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{cy}	2.0	—	8	μs	4MHz — 1MHz external time base (Note 1)
$\overline{RT}$ Input						(Note 2)
Period	t_{RT}	t_{cy}	—	—	—	
High Pulse Width	t_{RTH}	½t_{cy}	—	—	—	
Low Pulse Width	t_{RTL}	½t_{cy}	—	—	—	
I/O Ports						
Data Input Setup Time	t_S	—	—	¼t_{cy}−125	ns	
Data Input Hold Time	t_D	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	500	800	ns	Capacitive load = 50pF

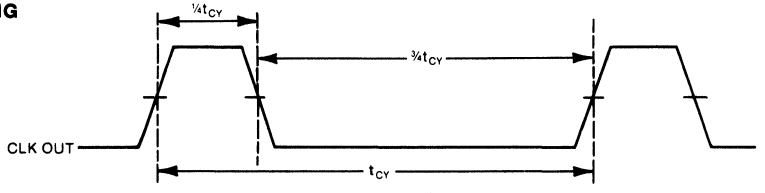
NOTES:
1. Instruction cycle period (t_{CY}) equals eight times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RT}$ input, CLK OUT may be directly tied to the $\overline{RT}$ input. The minimum times specified represent theoretical limits.

MICROCOMPUTER

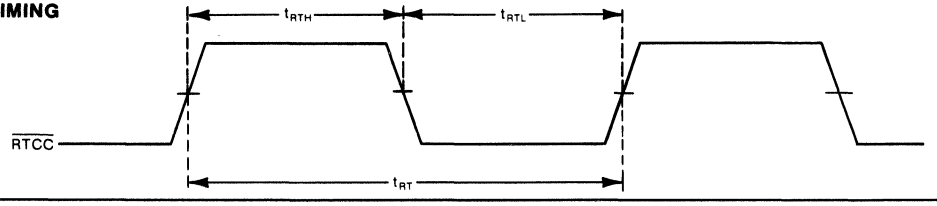
I/O TIMING



CLK OUT TIMING

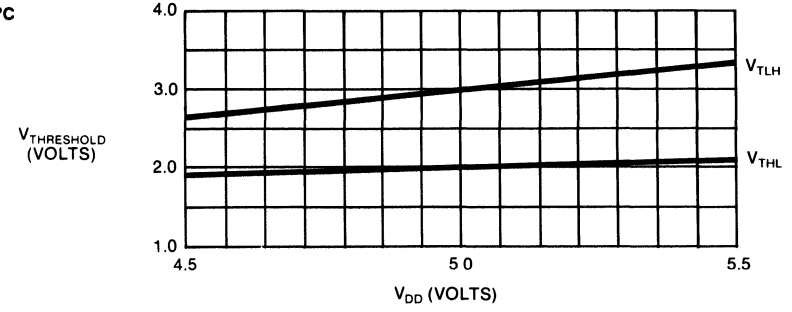


$\overline{\text{RTCC}}$ TIMING



SCHMITT TRIGGER CHARACTERISTICS (Typical)

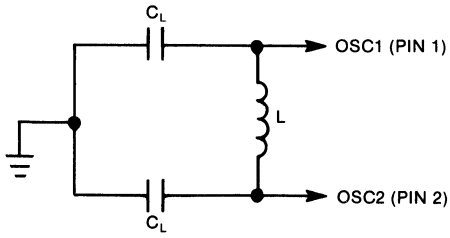
($\overline{\text{RT}}$, $\overline{\text{MCLR}}$) $T_A = 25°C$



MICROCOMPUTER

PIC1670 OSCILLATOR OPTIONS (TYPICAL CIRCUIT)

LC OPERATION

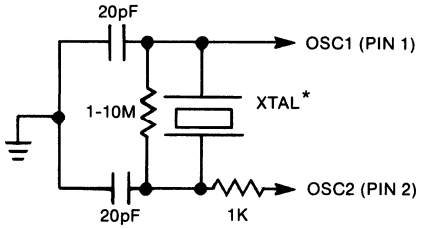


$$f_{OSC} \approx \frac{1}{2\pi\sqrt{L\,(C_L + C_{INT})}},$$

where $C_{INT} = 10pF$.

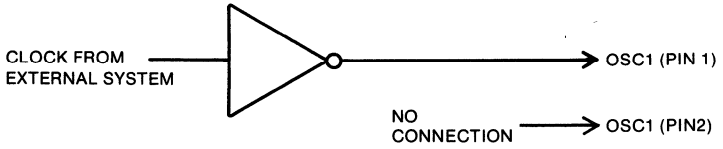
Typical values for 4MHz operation:
$L = 70\mu H$
$C_L = 10pF$

CRYSTAL INPUT OPERATION

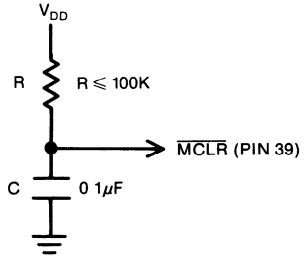


*or ceramic resonator, parallel resonant (0.8 - 5.0MHz)

EXTERNAL CLOCK INPUT OPERATION

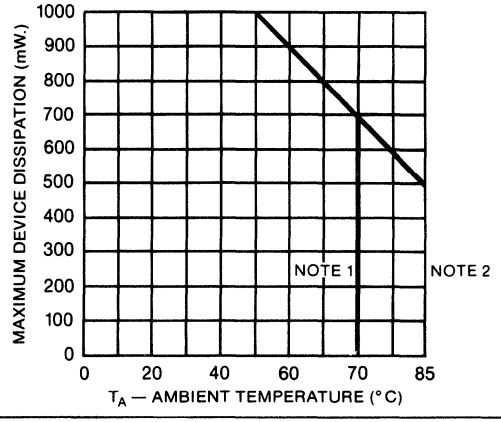


MASTER CLEAR (TYPICAL CIRCUIT)



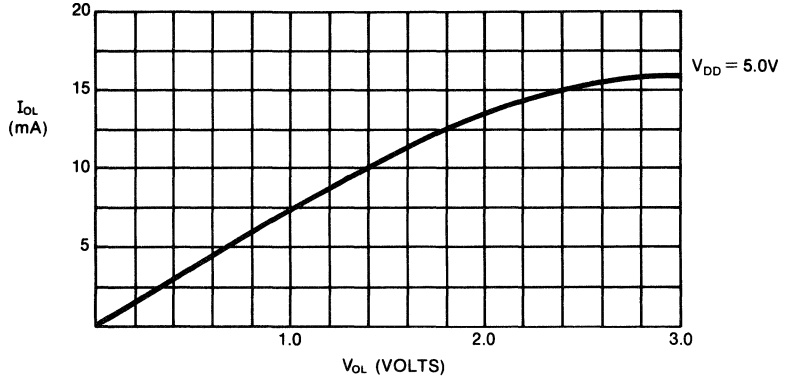
Master Clear requires 10ms delay (assuming a 4MHz crystal) before activation after power is applied to the V_{DD} pin, for the crystal to start up. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

POWER DISSIPATION DERATING GRAPH



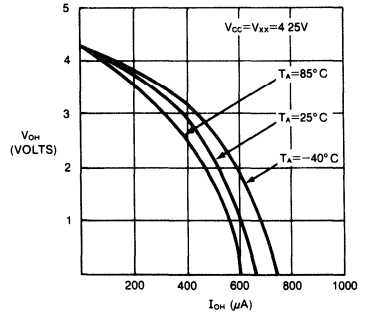
NOTES:
1. 70° C is the maximum operating temperature for standard parts.
2. 85° is the maximum operating temperature for "I" suffix parts

OUTPUT SINK CURRENT GRAPH



The Output Sink Current is dependent on the output load. This chart shows the typical curve used to express the output drive capability.

V_{OH} VS I_{OH} (I/O PORTS) (Typical)



MICROCOMPUTER

GENERAL INSTRUMENT

PIC Development Series

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
8 BIT DEVELOPMENT MICROCOMPUTER	PIC microcomputer without ROM and with addition of a HALT pin.	PIC1664	4-96
		PIC16C63	4-110
		PIC1665	4-121

8 Bit Development Microcomputer

FEATURES

- PIC microcomputer with ROM removed
- Useful for engineering prototyping of PIC applications
- PIC ROM address & data lines brought out to pins
- HALT pin for single stepping or stopping program execution
- MODE pin for selection of PIC1650A/1655A or PIC1656 emulation
- User programmable via external memory
- 32 8-bit RAM registers
- Arithmetic Logic Unit
- User defined TTL-compatible Input and Output lines
- Real Time Clock/Counter
- Self-contained oscillator
- Access to RAM registers inherent in instruction
- Wide power supply operating range (4.5V to 7.0V)

DESCRIPTION

The PIC1664 development microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit on a single chip.

The PIC1664 MOS/LSI is functionally identical to the PIC microcomputers except that the ROM is removed and the ROM address and data lines are brought out, requiring a 64-pin package. The addition of a HALT pin gives the user the ability to stop as well as single-step the chip. The logic level applied to a MODE pin determines whether the PIC1664 emulates a PIC1650A/1655A or a PIC1656.

The external ROM can contain a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications.

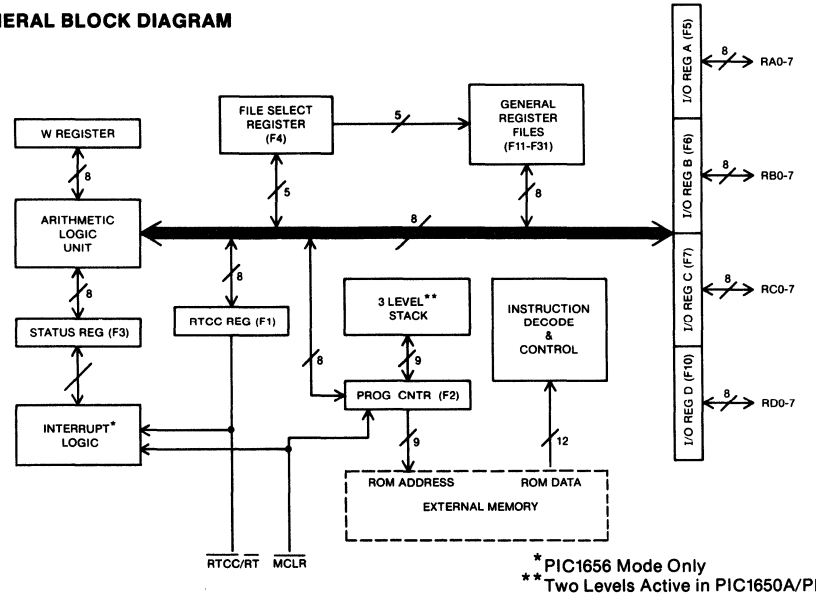
The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC Series is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Application notes and sample programs are used to develop programs which can then be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PFD Field Demo Systems are available containing a PIC1664 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with stand-alone emulation and debugging operation or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM.

MICROCOMPUTER

PIC1664 GENERAL BLOCK DIAGRAM



*PIC1656 Mode Only
**Two Levels Active in PIC1650A/PIC1655A Mode

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC1664 microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC1664 is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined external ROM composed of 512 program words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general register. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the MCLR input on power up initializes the external ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
MODE (input)	Mode input. Used to set the PIC1664 to emulate the PIC1650A/PIC1655A (logic "one") or the PIC1656 (logic "zero"). The mode must be selected before $\overline{MCLR}$ is brought high.
OSC1 (input) **OSC2 (output)**	Oscillator pins. When the MODE switch selects PIC1650A/1655A operation OSC1 becomes a single input clock using either RC control or a buffered crystal. When the PIC1664 is in the PIC1656 mode both OSC1 and OSC2 are used as a two input clock using either crystal, ceramic resonator or LC network.
$\overline{RT}$ (input)	Real Time Clock input. This pin increments the Real Time Clock Counter Register 1 on high to low transitions applied to this input. This pin has different modes of operation depending on the MODE input as well as the contents of F3, the Status Register. In PIC1650A/1655A mode this pin emulates the $\overline{RTCC}$ pin. In the PIC1656 mode this pin emulates the $\overline{RT}$ pin.
RA0-7, RB0-7, RC0-7, RD0-7 (input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program During emulation of the PIC1655A or PIC1656, Register D will become internal general purpose File Register 10; I/O lines RD0-7 will be undefined and must be left unconnected.
$\overline{MCLR}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O registers high (for PIC1650A/1655A) or I/O registers F6 and F7 low and F5 high (for PIC1656). Also clears bits 3-7 of status register (F3) (for PIC1656). This pin should be held low at least 1-10ms after the power supply is valid for the oscillator to start up. $\overline{MCLR}$ has no internal pullup resistor.
V_{DD}	Primary Power supply input.
V_{XX}	Output buffer power supply input. Used to increase current sinking capability when emulating the PIC1650A and PIC1655A. When emulating the PIC1656 this pin must be connected to V_{DD}.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing. The OSC frequency is divided by 4 for PIC1650A/1655A mode or by 16 for the PIC1656 mode.
HALT (input)	Halt. When high this input suspends execution of the next instruction. No data is lost and after HALT is brought low execution proceeds exactly as if no HALT signal had been applied.
HALT ACK (output)	Halt Acknowledge. This output is high when the PIC1664 is halted either due to an active HALT input or execution of the HALT instruction (0001_8). In the first case HALT ACK is brought back low when the PIC1664 begins execution when the HALT input is brought low; and in the second case it is brought low using $\overline{MCLR}$ or by first raising and then lowering the HALT input.
D0-D11 (input)	Data Input. These twelve lines accept twelve bit PIC instruction codes generated by an external source D0 is the LSB of the instruction.
A0-A8 (output)	Address Output. These nine lines represent the address of the next instruction to be executed by the PIC1664. A0 is the LSB of the address.

MODE PIN OPERATION

The mode pin is used to select either PIC1650A/1655A emulation or PIC1656 emulation.

With the MODE pin set high, the PIC1664 is set to emulate the PIC1650A/1655A. Specifically:

1. $\overline{MCLR}$ will force all I/O registers high.
2. OSC1 becomes a single clock input. The PIC1664 will execute instructions at one fourth the OSC frequency.
3. The interrupt system is disabled and the RTCC always counts on trailing edges.
4. Bits 3-7 of F3 are ones.

When the MODE input is low, the PIC1664 will emulate the PIC1656 circuit. Specifically:

1. MCLR will force I/O registers F6 and F7 low and F5 high.
2. OSC1 and OSC2 become a two input clock supporting crystals, ceramic resonators, or RC networks. The PIC1664 will execute instructions at one sixteenth the OSC frequency.
3. The interrupt system is connected and the interrupt/RTCC operation is as described in the PIC1656 data sheet.
4. Bits 3-7 of F3 are used for interrupt service.

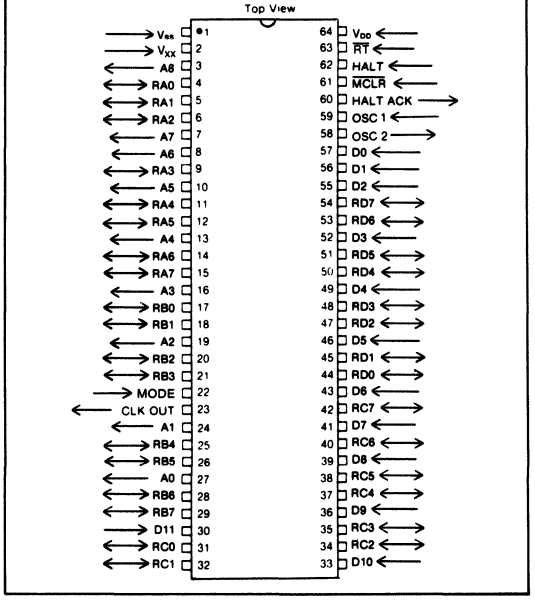
To insure proper chip operation, the Mode pin should be preset before $\overline{MCLR}$ is brought high at initialization. "Dynamic-type" switching of this pin during processor operation will result in undefined conditions and must be avoided.

PROGRAMMING CAUTIONS

The PIC1664 is designed as a development circuit for emulating the operation of the PIC1650A, PIC1655A and PIC1656. While all circuits in the PIC series have the same basic architecture and instruction set, there are differences which require attention on the part of the user to insure that all conditions are met for proper operation of the PIC1664 with respect to the target PIC circuit (either PIC1650A, PIC1655A, or PIC1656). The following checklist should be used to achieve proper emulation.

1. The MODE pin must be properly set (high for PIC1650A/PIC1655A or low for PIC1656).
2. With the MODE pin high OSC1 is a single clock input. A low on the MODE pin enables the two input clock.
3. For PIC1650A and PIC1655A emulation, bits 3-7 of F3 (the status register) should be considered undefined.
4. For PIC1655A and PIC1656 emulation bits 4-7 of F5 (the input only file) should be tied to V_{SS} (ground) as these bits are always read as low inputs.
5. For PIC1655A and PIC1656 emulation the pins corresponding to $F10_8$ (I/O port RD on the PIC1650A) should be left unconnected. In this way $F10_8$ will operate as an internal register as is appropriate for the PIC1655A and PIC1656.
6. The I/O Programming Caution on page 3-11 describing the I/O variations between the PIC1650A and the PIC1655A/PIC1656 must be carefully followed. The PIC1664 contains all bidirectional input/output ports as required for PIC1650A emulation. The I/O structure variation used in PIC1655A and PIC1656 require careful adherence to the cautions listed in the following pages.
7. The RETURN (0002_8) instruction is not supported by the PIC1650A and PIC1655A and should not be used when emulating these parts. The HALT instruction (0001_8) is not recognized by any PIC circuit other than the PIC1664.
8. For PIC1656 emulation the V_{XX} pin must be tied directly to V_{DD} as there is no V_{XX} pin on the PIC1656.

PIN CONFIGURATION
64 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to the contents of W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RT}$. However, if data are being stored in the RTCC register simultaneously with a negative transition on the RTCC pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer
F2	Program Counter (PC). The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2). The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
CNT	RTCR	IR	RTCE	IE	Z	DC	C

BIT 0: Carry (C) bit — For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.

For ROTATE instructions, this bit is loaded with either the high or low order bit of the source

BIT 1: Digit Carry (DC) bit — For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

BIT 2: Zero (Z) bit — Set if the result of an arithmetic operation is zero

BITS: 3-7 — Interrupt Service Flags (Cleared on $\overline{MCLR}$).

BIT 3: Interrupt Enable (IE) status bit. When set to a one, this bit enables the external interrupt to occur when and if the interrupt request (IR) status bit (bit 5) is also set. When reset to a zero, the external interrupt is disabled.

BIT 4. Real Time Clock Enable (RTCE) status bit. When set to a one, this bit enables the real-time clock/counter interrupt to occur when and if the real-time clock interrupt request (RTCR) status bit (bit 6) is also set. When reset to a zero, the interrupt is disabled.

BIT 5: Interrupt Request (IR) status bit. This bit is set by a high-to-low transition on the $\overline{RT}$ pin, generating an interrupt request. If and when the interrupt enable (IE) bit (bit 3) is also set, an interrupt will occur. This causes the current PC address to be pushed onto the stack and the processor to execute the instruction at location 760_8. The IR bit is then immediately cleared. Note that the IR bit can be set regardless of the state of the IE bit, thus requesting an interrupt which can be serviced or not at the programmer's option.

BIT 6: Real Time Clock/Counter Interrupt Request (RTCR) status bit This bit is set when the RTCC register (File 1) transitions from a full count (377_8) to a zero count (000_8). If and when the RTCE bit is also set, an interrupt will occur This causes the current PC address to be pushed onto the stack and the processor to execute the instruction at location 740_8. The RTCR bit is then immediately cleared. Note that the RTCR bit can be set regardless of the state of the RTCE bit, thus requesting an interrupt which can be serviced or not, at the programmer's option.

NOTE. Although the processor cannot be interrupted during an interrupt (i e , until the RETFI instruction is executed), (an) other interrupt(s) can be requested (status bits 5 and/or 6 can be set) This will cause the processor to reinterrupt immediately upon its return from the current interrupt assuming the interrupt(s) is (are) enabled (Pending external interrupts have priority over pending real-time clock/counter interrupts)

BIT 7: Count Select (CNT) status bit. When CNT bit is set to a one, the RTCC register will increment on each high-to-low transition at the $\overline{RT}$ pin. If the CNT bit is sent to a zero, the RTCC register will increment at the internal clock rate (1/16 of the frequency at the OSC pins).

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	Input Register A (A0-A3). A4-A7 defined as zeroes.
F6	Output Register B (B0-B7)
F7	I/O Register (C0-C7)
F10-F37	General Purpose Registers

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

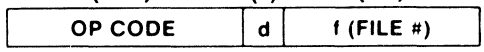
For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz for PIC1650A and PIC1655A (4MHz for PIC1656) the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

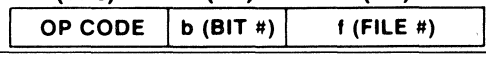
BYTE-ORIENTED FILE REGISTER OPERATIONS



For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1)

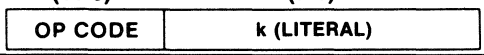
Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇋f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b) skip is set	None

LITERAL AND CONTROL OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 010 (0002)	Return from Interrupt	RETURN	—	Stack→PC	None
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

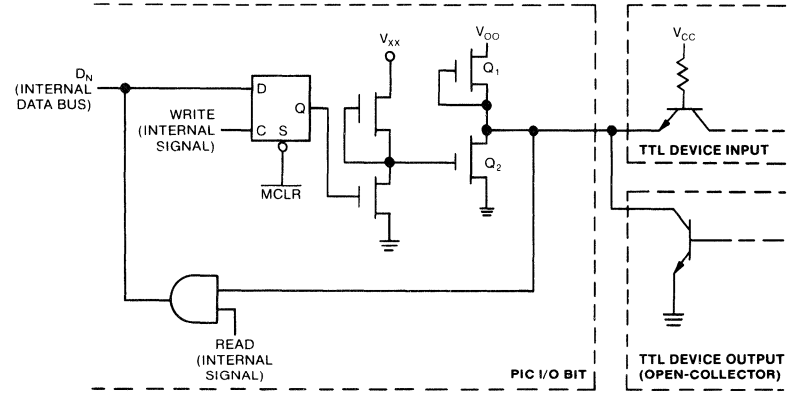
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation These rules must be carefully followed in the instruction sequences written for I/O operation

Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction The outputs are latched and remain unchanged until the output latch is rewritten **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high This principle is the same whether operating on individual bits or the entire port.

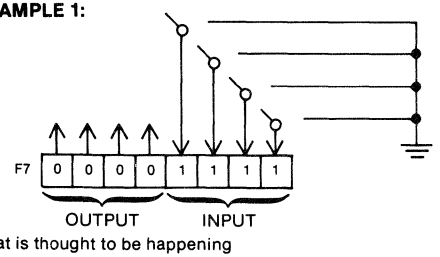
Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions.

As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the input/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



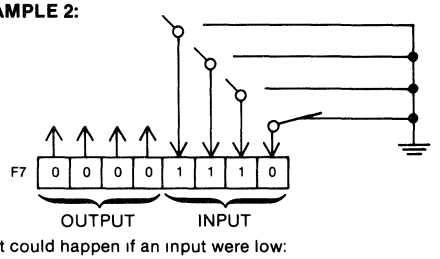
What is thought to be happening

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 7,5

Read into CPU	00001110
Set bit 5	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... −0.3V to +10.0V
Power Dissipation 1000mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS/PIC1664

Operating Temperature $T_A = 0°C$ to $+70°C$

Characteristics	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	55	mA	All I/O pins @ V_{DD}
Output Buffer Supply Current	I_{XX}	—	1	5	mA	All I/O pins @ V_{DD} (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RT}$ & OSC1)	V_{IH}	2.4	—	V_{DD}	V	
Input Low-to-High Threshold Voltage ($\overline{MCLR}$, $\overline{RT}$ & OSC1 in PIC1650A/55A mode)	V_{ILH}	$V_{DD}-1$	2.6	V_{DD}	V	
Output High Voltage	V_{OH}	2.4 3.5	— —	V_{DD} V_{DD}	V V	$I_{OH} = -100\mu A$ (Note 4) $I_{OH} = 0$
Output Low Voltage (I/O only)	V_{OL1}	— — — — —	— — — — —	0.45 0.90 0.90 1.20 2.0	V V V V V	$I_{OL} = 1.6mA$, $V_{XX} = 4.5V$ $I_{OL} = 5.0mA$, $V_{XX} = 4.5V$ $I_{OL} = 5.0mA$, $V_{XX} = 8.0V$ $I_{OL} = 10.0mA$, $V_{XX} = 8.0V$ $I_{OL} = 20.0mA$, $V_{XX} = 8.0V$ (Note 5)
Output Low Voltage A0-A8 CLK OUT HALT ACK	V_{OL2}	—	—	0.45	V	$I_{OL} = 1.6mA$ (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RT}$)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$ (note 6)
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	$V_{IL} = 0.4V$ internal pullup
Input High Current (all I/O ports)	I_{IH1}	−0.1	−0.4	−1.4	mA	$V_{IH} = 2.4V$
Input High Current (HALT)	I_{IH2}	—	50	200	μA	$V_{IH} = 2.4V$ internal pulldown
OSC Input (PIC1650/55 MODE)						
External Input Impedance High	R_{OSCH}	120	800	3500	Ω	$V_{OSC} = V_{DD} = 5V$. (Applies to external OSC drive only.)
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	$V_{OSC} = 0.4V$
OSC Input (PIC1656 MODE)						
OSC1 External Input Low Voltage	V_{IL} (OSC1)	−0.2	—	0.8	V	
OSC1 External Input High Voltage	V_{IH} (OSC1)	$V_{DD}-1$	—	—	V	

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(|I_{IL}|) + \Sigma (V_{DD} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.
6. Also applies to OSC1 pin in PIC1656 mode.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

Operating Temperature $T_A = 0°C$ to $+70°C$

Characteristics	Sym	Min	Typ†	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.2MHz — 1.0MHz external time base 1650A/1655A mode 0.8MHz —4.0MHz external time base 1656 mode (Note 1)
RT Input						
Period	t_{RT}	$t_{CY}+0.2\mu s$	—	—	—	
High Pulse Width	t_{RTH}	$\frac{1}{2}t_{RT}$	—	—	—	
Low Pulse Width	t_{RTL}	$\frac{1}{2}t_{RT}$	—	—	—	(Notes 2 and 3)
I/O Ports						
Data Input Setup Time	t_S	—	—	$\frac{1}{4}t_{CY}-125$	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	600	1000	ns	Capacitive load = 50pF
HALT ACK Output Propogation Delay	t_{HA}	—	200	—	ns	
A_0-A_8 Output Propogation Delay	t_{AD}	—	350	—	ns	
D_0-D_{11} Input Set-up Time	t_{DS}	0	—	—	ns	
D_0-D_{11} Input Hold Time	t_{DH}	200	—	—	ns	

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$.

NOTES:

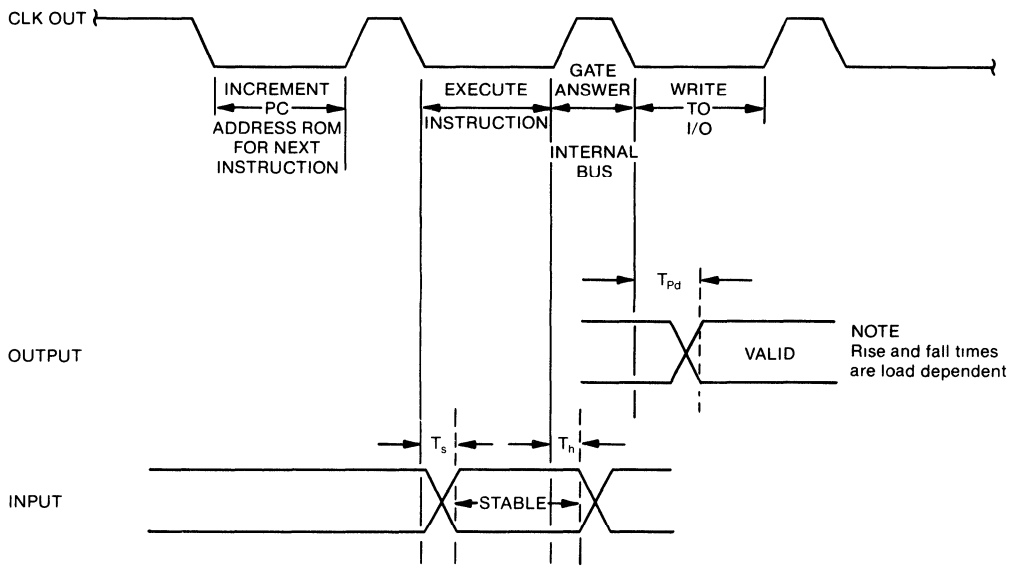
1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period for 1650A/1656A operation or sixteen times oscillator time base period for 1656 operation.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the RTCC input, CLK OUT may be directly tied to the $\overline{RT}/\overline{RTCC}$ input without any loss of counts.
3. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$$

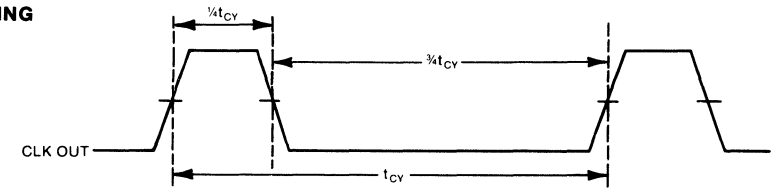
For example:

if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

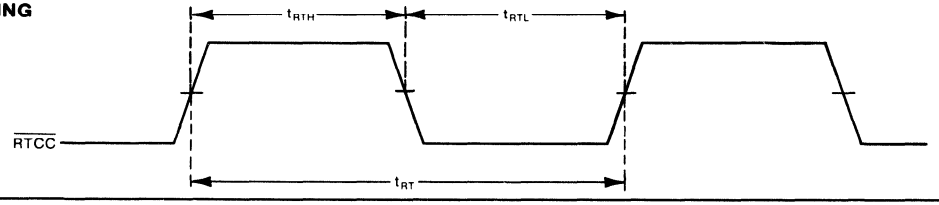
I/O TIMING



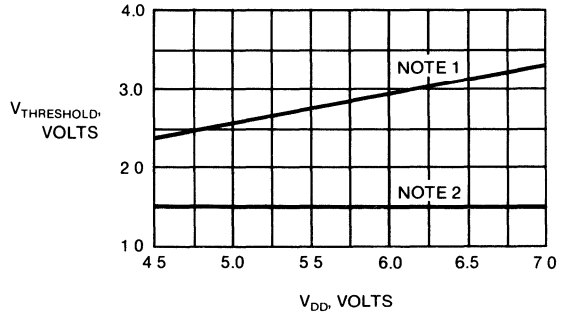
CLK OUT TIMING



$\overline{RT}$ TIMING



SCHMITT TRIGGER CHARACTERISTICS ($\overline{RTCC}$, $\overline{MCLR}$ and OSC PINS) T_A = 25°C (TYPICAL)

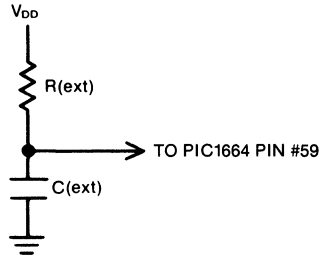


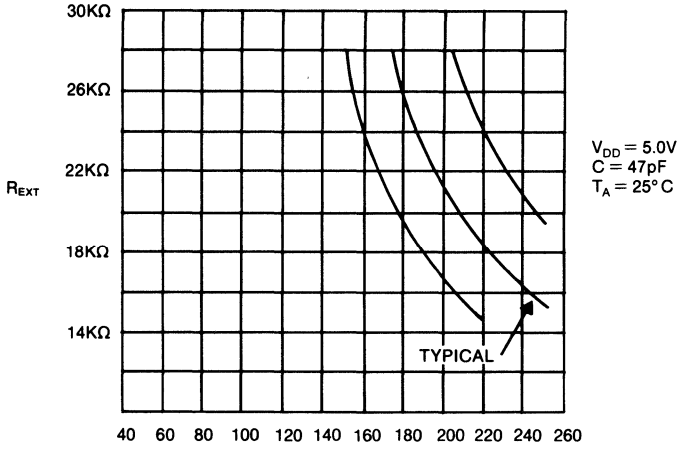
NOTES:
1. Low-to-High Threshold Voltage (V_{TLH}).
2. High-to-Low Threshold Voltage (V_{THL}).

MICROCOMPUTER

PIC1664 OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

RC OPTION OPERATION

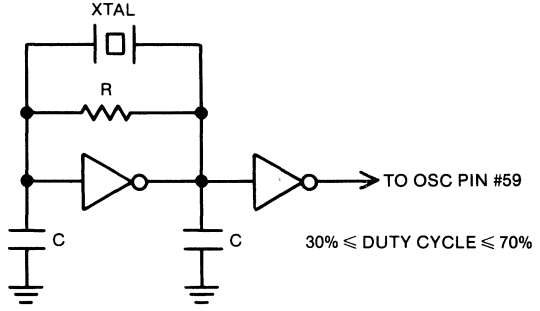




Oscillator Frequency With Typical Unit To Unit Variance

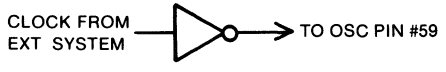
Unit to Unit Variation at V_{DD} = 5.0V, T_A = 25°C is ±25%
Variation from V_{DD} = 4.5V −7 0V referenced to 5V is −3%, +9%
Variation from T_A = 0°C −70°C referenced to 25°C is +3%, −5%

BUFFERED CRYSTAL INPUT OPERATION



The buffer must be capable of driving 120Ω, min. (800Ω, typ.) to 2 0V
However, it is recommended that the pull-down transistor on the OSC pin be removed (an option) if OSC is to be driven externally.

EXTERNAL CLOCK INPUT OPERATION



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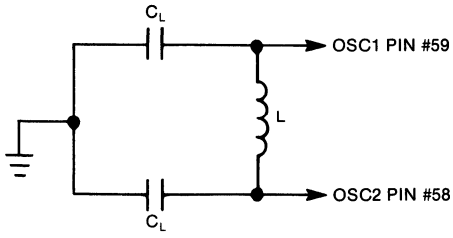
PIC1664 OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

LC INPUT OPERATION

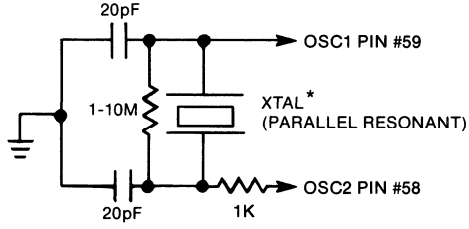


$$f_{OSC} \approx \frac{1}{2\pi \sqrt{L\,(C_L + C_{INT})}},$$

where $C_{INT} = 10pF$.

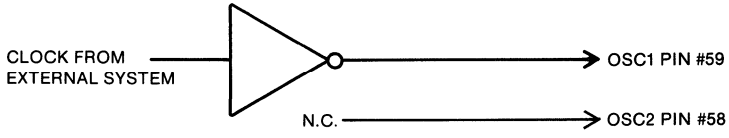
Typical values for 4MHz operation:
$L = 70\mu H$
$C_L = 10pF$

CRYSTAL INPUT OPERATION

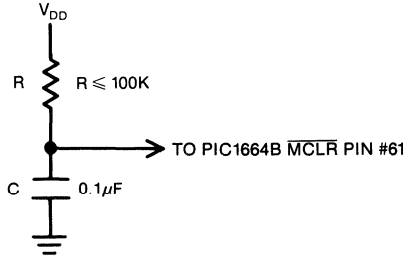


* or ceramic resonator

EXTERNAL CLOCK INPUT OPERATION

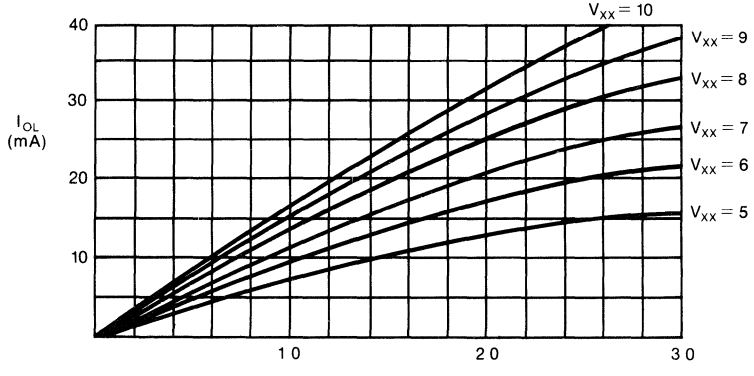


MASTER CLEAR (TYPICAL CIRCUIT)



Master Clear requires >1 0ms delay before activation after power is applied to the V_{DD} pin, for the oscillator to start up. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function)

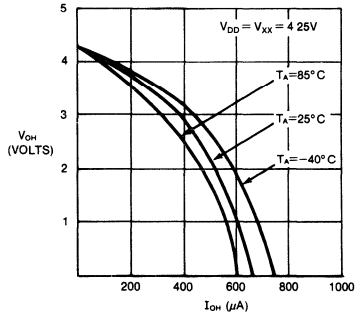
OUTPUT SINK CURRENT GRAPH



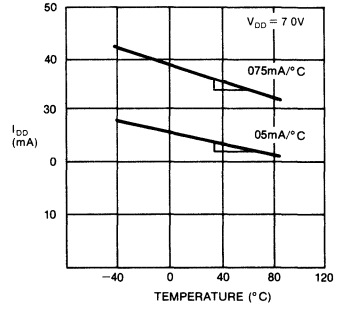
I_{OL} vs. V_{OL} TYP @ 25°C

The Output Sink Current is dependent on the V_{XX} supply and the output load This chart shows the typical curves used to express the output drive capability.

V_{OH} VS I_{OH} (I/O PORTS) (TYPICAL)



POWER SUPPLY CURRENT VS TEMPERATURE (TYPICAL LIMITS)



MICROCOMPUTER

PIC1650A/PIC1655A EMULATION CAUTIONS

When emulating a PIC1650A or PIC1655A using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1650A/PIC16655A mode. (Refer to PICES II Manual). The PIC1664 contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{MCLR}$ to force all I/O registers high.
2. The OSC1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 40 pin socket for the PIC1650A and the 28 pin socket for the PIC1655A module plugs.

E. Make sure that during an actual application that the $\overline{MCLR}$ input swings from a low to high level a minimum of 1 msec after the supply voltage is applied.

F. If an external oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC1664.

G. The cable length and internal variations may cause some parameter values to differ between the PICES II module and a production PIC1650A and PIC1655A.

PIC1656 EMULATION CAUTIONS

When emulating a PIC1656 using a PICES II development system certain precautions should be taken.

A. Be sure that the PICES II Module being used is programmed for the PIC1656 mode. (Refer to PICES II Manual). The PIC1664 contained within the module should have the MODE pin #22 set to a low state.

1. This causes the $\overline{MCLR}$ to force F5 register high and F6 and F7 low.
2. The OSC1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes enabled and the $\overline{RT}$ always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are used for interrupt servicing.

B. All three levels of stack can be used within the program. If interrupts are used, allow one level of the stack for interrupt servicing.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 28 pin socket for the module plug.

E. Make sure that during an actual application that the $\overline{MCLR}$ input swings from a low to high level a minimum of 1 msec after the supply voltage is applied.

F. The cable length and internal variations may cause some parameter values to differ between the PICES II module and a production PIC1656.

8 Bit Development Microcomputer

FEATURES

- PIC microcomputer with ROM removed
- Useful for engineering prototyping of PIC applications
- ROM address & data lines brought out to pins
- HALT pin for single stepping or stopping program execution
- 50/55 pin for selection of PIC16C50 or PIC16C55 emulation
- 32 8-bit RAM registers
- Arithmetic Logic Unit
- Real Time Clock/Counter
- Self-contained oscillator
- Access to RAM registers inherent in instruction
- Wide power supply operating range (2.5V to 6.0V)

DESCRIPTION

The PIC16C63 development microcomputer is a CMOS/LSI device containing RAM, I/O, and a central processing unit on a single chip.

The PIC16C63 CMOS/LSI device is functionally identical to the PIC16C55 microcomputer except that the ROM is removed and the ROM address and data lines are brought out, requiring a 64-pin package. The addition of a HALT pin gives the user the ability to stop as well as single-step the chip. The logic level applied to the $\overline{50}$/55 pin determines whether the PIC16C63 emulates a PIC16C50 or PIC16C55.

The external ROM can contain a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/ouput registers provide latched lines for interfacing to a limitless variety of applications.

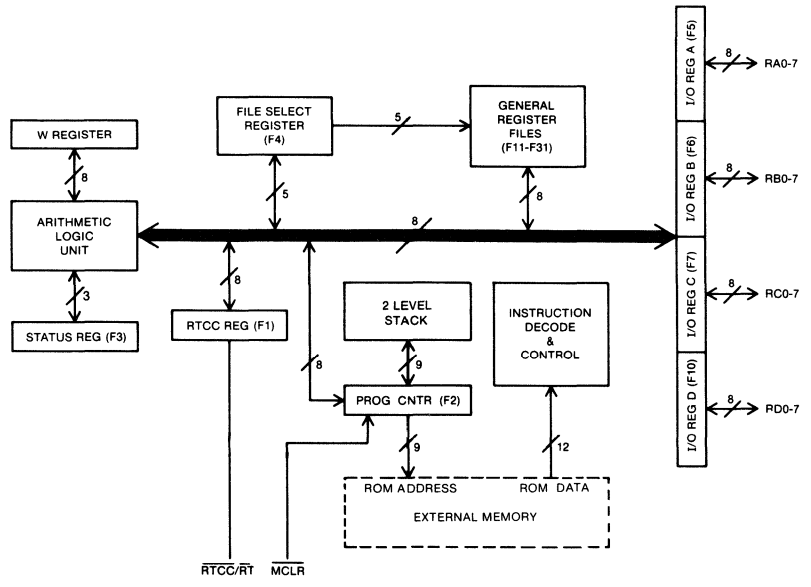
The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC Series is fabricated with complimentary MOS technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or crystal oscillator for greater accuracy) to establish the frequency.

Extensive hardware and software support is available to aid the user in developing this application program and to verify performance before committing to mask tooling. Application notes and sample programs are used to develop programs which can then be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PFD Field Demo Systems are available containing a PIC16C63 with sockets for erasable CMOS PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with stand-alone emulation and debugging operation or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM.

MICROCOMPUTER

PIC16C63 GENERAL BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC16C63 microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC16C63 is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined external ROM composed of 512 program words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general register. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the MCLR input on power up initializes the external ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
50/55 (input)	Used to set the PIC16C63 to emulate the PIC16C55 (logic "one") or the PIC16C50 (logic "zero"). The mode must be selected before $\overline{MCLR}$ is brought high. This pin has an internal pullup.
OSC1 (input), OSC2	Oscillator pins. Both OSC 1 and OSC 2 are used as a two pin oscillator clock using either crystal, ceramic resonator or RC network or OSC 1 can be driven by an external clock signal.
$\overline{RTCC}$ (input)	Real Time input. This pin increments the Real Time Clock Counter Register 1 on high to low transitions applied to this input.
RA0-7, RB0-7, RC0-7, RD0-7 (input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program. During emulation of the PIC16C55, Register D will become internal general purpose File Register 10; Register B will become an output only file. Any instruction involving a read (all instructions except literal and control operations, NOP, MOVWF, CLRW and CLRF) will not read the pin but will read data from the output latch.
$\overline{MCLR}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and to latch all I/O registers into tri-state mode This pin should be held low at least 1ms after the power supply is valid. $\overline{MCLR}$ has no internal pullup resistor.
V_{DD}	Primary Power supply input.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing. The OSC frequency is divided by 5.
HALT (input)	Halt. When high this input suspends execution of the next instruction. No data is lost and after HALT is brought low execution proceeds exactly as if no HALT signal has been applied.
HALT ACK (output)	Halt Acknowledge. This output is high when the PIC16C63 is halted either due to an active HALT input or execution of the HALT insruction (0001_8). In the first case HALT ACK is brought back low when the PIC 16C63 begins execution when the HALT input is brought low; and in the second case it is brought low using $\overline{MCLR}$ or by first raising and then lowering the HALT input.
D0-D11 (input)	Data input. These 12 lines accept 12 bit PIC instruction codes generated by an external source. D0 is the LSB of the instruction.
A0-A8 (output)	Address Output. These 9 lines represent the address of the next instruction to be executed by the PIC16C63. A0 is the LSB of the address.

MODE PIN OPERATION

The mode pin is used to select either PIC16C50 emulation or PIC16C55 emulation.

With the $\overline{50}$/55 pin set high, the PIC16C63 is set to emulate the PIC16C55. Specifically:

1. I/O port RD is general purpose register.
2. I/O port RB is output only.

When the MODE input is low, the PIC16C63 will emulate the PIC16C50 circuit. Specifically:

1. All ports will be I/O.

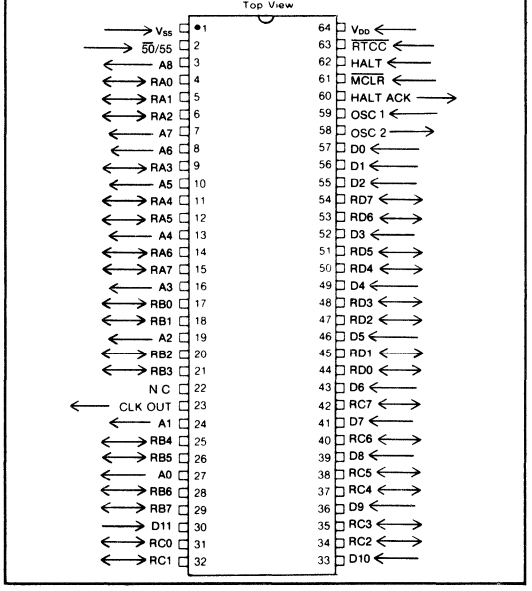
To insure proper chip operation, the $\overline{50}$/55 pin should be preset before $\overline{MCLR}$ is brought high at initialization. "Dynamic-type" switching of this pin during processor operation will result in undefined conditions and must be avoided.

PROGRAMMING CAUTIONS

The PIC16C63 is designed as a development circuit for emulating the operation of the PIC16C50 and PIC16C55. While all circuits in the PIC series have the same basic architecture and instruction set, there are differences which require attention on the part of the user to insure that all conditions are met for proper operation of the PIC16C63 with respect to the target PIC circuit (either PIC16C50 or PIC16C55). The following checklist list should be used to achieve proper emulation.

1. The $\overline{50}$/55 pin must be properly set (high for PIC16C55 or low for PIC16C50).
2. For PIC16C55 emulation bits 4-7 of F5 (the input only file) should be tied to V_{SS} (ground) as these bits are always read as low inputs
3. For PIC16C55 emulation the pins corresponding to $F10_8$ (I/O port RD on the PIC16C50) should be left unconnected. In this way $F10_8$ will operate as an internal register as is appropriate for the PIC16C55.
4. The HALT instruction (0001_8) is not recognized by any PIC circuit other than the PIC16C63.

PIN CONFIGURATION
64 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of a pulse on the $\overline{RTCC}$ pin. However, if data are being stored in the RTCC register simultaneously with a negative transition on the $\overline{RTCC}$ pin, the RTCC register will contain the new stored value and the external transition will be ignored by the microcomputer.
F2	Program Counter (PC). The PC is automatically incremented and each instruction cycle can be written into under program control e.g., MOVWF F2. The PC is nine bits wide, but only the low order 8 bits can be read under program control.
F3	Status Word Register. When F3 is the destination register the status flags are overwritten.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

BIT 0: Carry (C) bit — For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant. For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

BIT 1: Digit Carry (DC) bit — For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

BIT 2: Zero (Z) bit — Set if the result of an ALU operation is zero.

BITS: 3-7 — These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	I/O Register A (A0-A7)
F6	I/O Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10	I/O Register D (D0-D7)
F11-F37	General Purpose Registers

Basic Instruction Set Summary

Each PIC instruction is 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

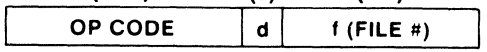
For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1 MHz the instruction execution time is 5 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 10 μsec.

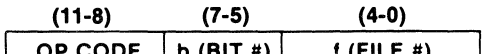
BYTE-ORIENTED FILE REGISTER OPERATIONS



For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

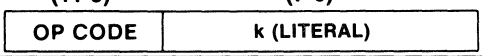
Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 off fff (0000)	Tri-state port f	TRIS	f	W→Tristate status f	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d [f+$\overline{W}$+1→d]	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\overline{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1), f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇆f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b). skip is set	None

LITERAL AND CONTROL OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 010 (0002)	Return	RETURN	—	Stack→PC	None
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.
3. TRIS f (where f=6 or 7 for PIC16C55 or 5, 6, 7, 10 for PIC16C50) causes the contents of W to be written to the tri-state latches of the specified file. A one forces the pin to tri-state the output buffer to a high impedance state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

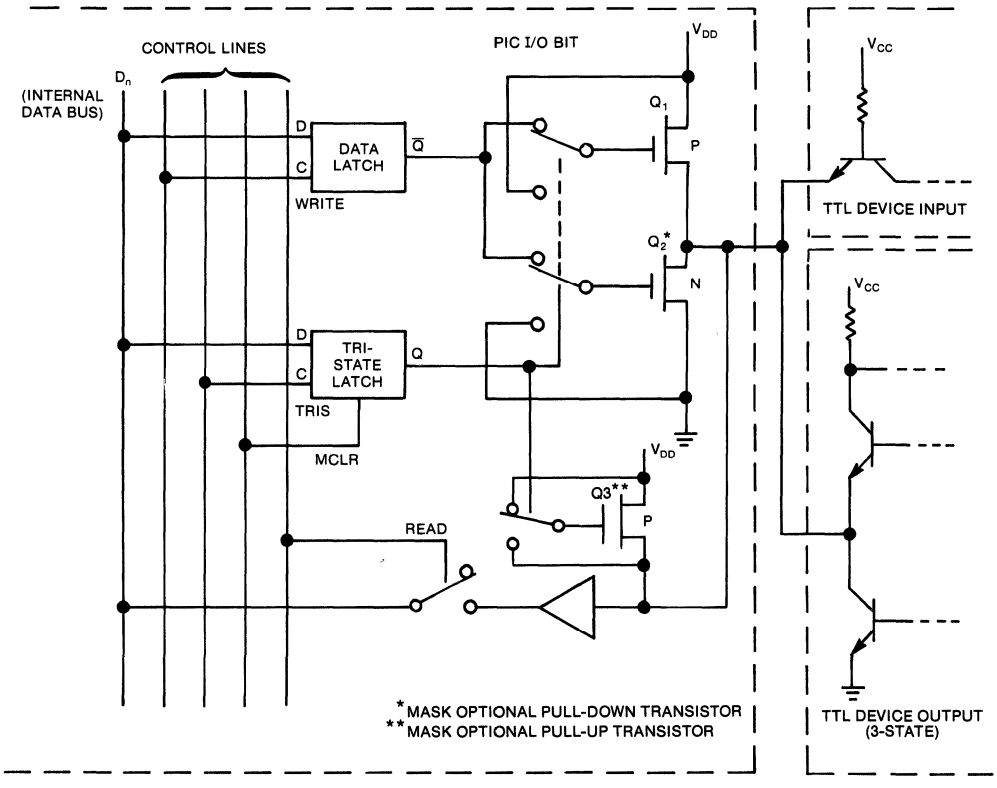
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of a tri-state TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port must first be set to the high impedance state under program control. This turns off Q_1 and Q_2 and turns on Q_3 (if present), allowing the TTL tri-state device to drive the pin.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE
(shown in active I/O state)



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation. (Note that for an output only port the latch, not the pin is read.)

Bidirectional I/O Ports

The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. For use as an input port the output must be set to the high impedance state via the tri-state latch. Thus the external device inputs to the PIC circuit by forcing the input line high or low. If the input lines are not tri-stated then refer to PIC1650A programming cautions. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $^1/_{st_{cy}}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient Temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any Pin with Respect to V_{SS} (Note 1) ..... −0.3V to V_{DD} +0.3V
Power Dissipation (Note 5) 300mW
Voltage on V_{DD} with Respect to V_{SS} ..... −0.3V to +6.5V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristics	Sym	Min	Typ†	Max	Units	Conditions
Supply Voltage	V_{DD}	2.5	—	6.0	V	
Supply Current	I_{DD}	— —	— —	2 5	mA mA	V_{DD} = 4V, V_{DD} = 6V } All I/O pins tri-state, t_{CY} = 4μsec
Input Low Voltage	V_{IL}	V_{SS}	—	0.2V_{DD}	V	
Input High Voltage	V_{IH}	0.8V_{DD}	—		V	
Output High Voltage (RB0-7, RC0-7)	V_{OH}	V_{DD} −0.4 V_{DD} −0.4	— —	— —	V V	I_{SOURCE} = 0.2mA, V_{DD} = 4.75V I_{SOURCE} = 80μA, V_{DD} = 2.5V
Output Low Voltage (RB0-7, RC0-7) (Note 1)	V_{OL}	—	—	0.4	V	I_{SINK} = 0.2mA, V_{DD} = 2.5V I_{SINK} = 1.6mA, V_{DD} = 4.75V
Input Low Current (RA0-3, RC0-7) (Note 2)	I_{IL}	—	—	250	μA	V_{DD} = 6V, V_{IN} = 0.4V
Input High Current (RA0-3, RC0-7) (Note 2)	I_{IH}	2	—	—	μA	V_{IN} = V_{DD} −0.4V
Leakage Current (Note 3)	I_{LC}	−1	—	1	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$
Input Low Current (HALT)	I_{IL}	15	—	—	μA	V_{IL} = 0.4V, V_{DD} = 5V ±5%
Input High Current (HALT)	I_{IH}	— —	— —	250 40	μA μA	V_{IH} = V_{DD} − 0.4V, V_{DD} = 5V ±5% V_{IH} = 2.1V, V_{DD} = 2.5V

†Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. The output pull-down transistor can be removed via a mask option to facilitate interfacing with external circuitry which has signal swings below V_{SS}. If this is the case, the maximum voltage permitted to be applied to the pin is −12V with respect to V_{DD}.
2. Current is being sourced by the internal pull-up resistors which are available as a mask option on ports RA0-3 and RC0-7. (RC0-7 have their pull-ups turned off when selected as outputs.)
3. This applies to ports RA0-3 and RC0-7 without the mask optional internal pull-up resistors, port RB0-7 and RC0-7 in the high impedance state, $\overline{RTCC}$, $\overline{MCLR}$ and OSC 1.
4. Total output sink current for all output pins (including CLK OUT) must not exceed 50mA. Total output source current must not exceed 20mA. Maximum output sink or source current for each individual output must not exceed 10mA.
5. Total power dissipation should not exceed 300mW for the package. Power dissipation is calculated as follows:
   $P_{DIS} = V_{DD} [(I_{DD}) - \Sigma (I_{IN} + I_{OH})] + \Sigma (V_{DD} - V_{IN}) (I_{IN}) + \Sigma (V_{DD} - V_{OH}) (I_{OH}) + \Sigma (V_{OL}) (I_{OL})$

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

Operating Temperature $T_A = 0°C$ to $+70°C$, $V_{DD} = 2.5 - 6.0V$ except as noted.

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Oscillator Frequency	f_{OSC}	25	—	1000	kHz	$V_{DD} = 2.5V$
	f_{OSC}	25	—	1250	kHz	$V_{DD} = 3.2V$
	f_{OSC}	25	—	1650	kHz	$V_{DD} = 5.0V$
	f_{OSC}	25	—	1800	kHz	$V_{DD} = 6.0V$
CLOCK OUT						
Period (Instruction Cycle Time)	t_{CY}	—	$5/f_{OSC}$	—	μs	(Note 1)
Pulse Width	t_{CLKH}	—	$1/f_{OSC}$	—	μs	
Rise/Fall Time	t_r/t_f	—	—	200	ns	1 TTL Load + 60pF $V_{DD} = 5V$
RTCC Input						
Period	t_{RT}	$t_{CY}+0.2\mu s$	—	—	—	(Notes 2 and 3)
Pulse Width (High or Low Level)	t_{pw}	500	—	—	ns	
I/O Ports						
Data Input Setup Time	t_S	—	—	$1/5t_{CY}-300$	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	—	1.6	μs	60pF + 2.2K to $0.8V_{DD}$
HALT ACK Output Propogation Delay	t_{HA}	—	—	600	ns	$V_{DD} = 5V \pm 5\%$, 1 TTL + 60pF load
A_0-A_8 Output Propogation Delay	t_{AD}	—	—	1	μs	$V_{DD} = 5V \pm 5\%$, $10\mu A$ + 60pF load
D_0-D_{11} Input Set-up time	t_{DS}	30	—	—	ns	$V_{DD} = 5V \pm 5\%$
D_0-D_{11} Input Hold Time	t_{DH}	300	—	—	ns	$V_{DD} = 5V \pm 5\%$

†Typical data is at $T_A = 25°C$, $V_{DD} = 5.0V$

NOTES:

1. Instruction cycle period (t_{CY}) equals five times the input oscillator time base period
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RTCC}$ input, CLK OUT may be directly tied to the $\overline{RTCC}$ input.
3. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows:

$$f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$$

For example:

if $t_{CY} = 4\mu s$, $f_{(max)} = \frac{1}{4.2\mu s} = 238KHz$.

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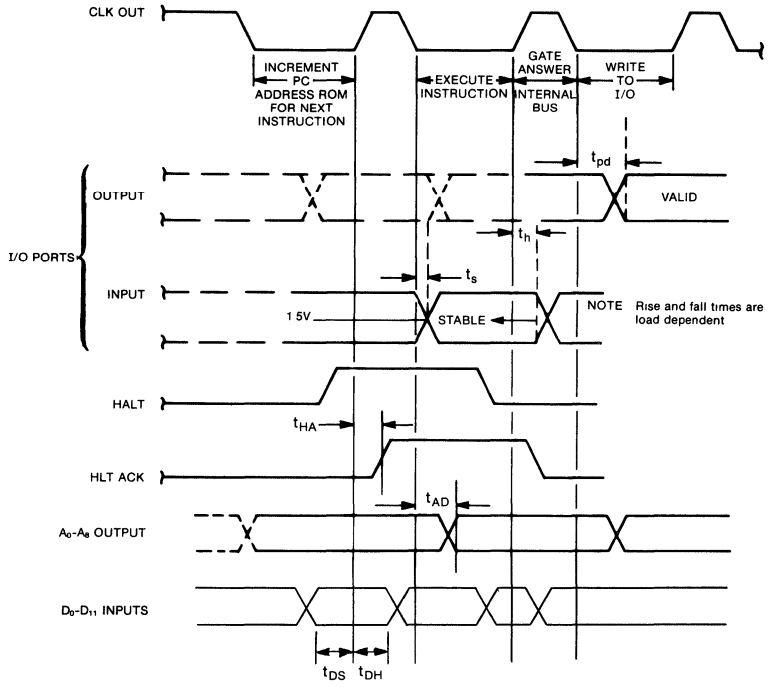
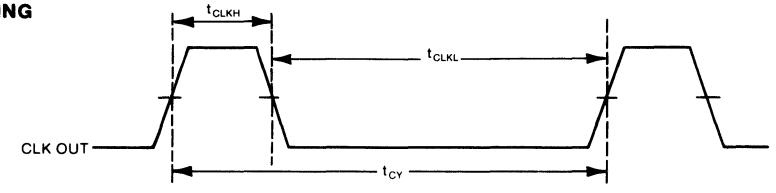
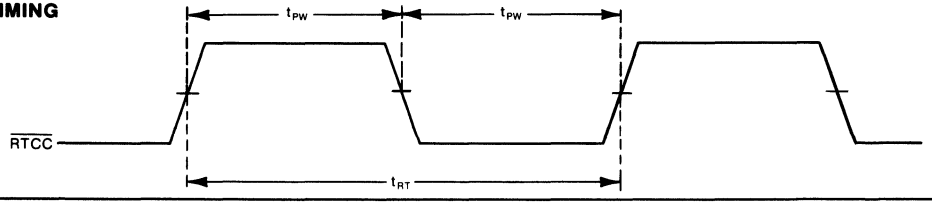
I/O TIMING



CLK OUT TIMING



$\overline{\text{RTCC}}$ TIMING



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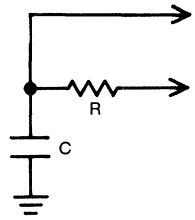
PIC16C63 EMULATION OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

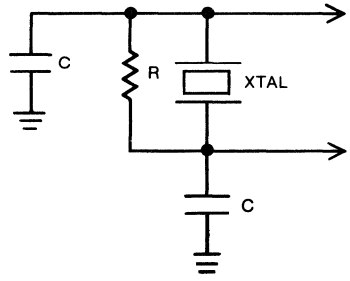
RC OPTION OPERATION



$10K \leq R \leq 1M$.

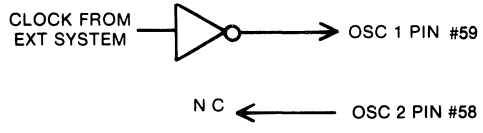
TYPICAL VALUES
$R \geq 10K$
$C \geq 100pF$

CRYSTAL INPUT OPERATION

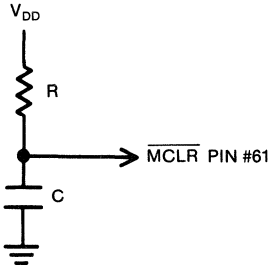


TYPICAL VALUES
R = 1M
C = −20pF

EXTERNAL CLOCK INPUT OPERATION



MASTER CLEAR



TYPICAL VALUES
R = 1M
C = 0.1μF

Master Clear may require up to a 75ms delay before activation after power is applied to the V_{DD} pin for a 1MHz crystal to start up. To achieve this an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function). The RC oscillator option, shown above, should start up in less time.

8 Bit Development Microcomputer

FEATURES

- PIC1670 microcomputer with ROM removed
- Useful for engineering prototyping of PIC applications
- PIC ROM address & data lines brought out to pins
- HALT pin for single stepping or stopping program execution
- User programmable via external memory
- 64 8-bit RAM registers
- Arithmetic Logic Unit
- User defined TTL-compatible Input and Output lines
- Real Time Clock/Counter
- Self-contained oscillator
- Access to RAM registers inherent in instruction
- Power supply operating range (4.5V to 5.5V)

DESCRIPTION

The PIC1665 development microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit on a single chip.

The PIC1665 MOS/LSI device is functionally identical to the PIC1670 microcomputer except that the ROM is removed and the ROM address and data lines are brought out, requiring a 64-pin package. The addition of a HALT pin gives the user the ability to stop as well as single-step the chip.

The external ROM can contain a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/ouput registers provide latched lines for interfacing to a limitless variety of applications.

The 13-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC1665 is fabricated with N-Channel Si-gate technology resulting in a high performance product with proven reliability and production history. Only a single power supply is required for operation, and an on-chip oscillator provides the operating clock with an external crystal, ceramic resonator or LC network to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing this application program and to verify performance before committing to mask tooling. Application notes and sample programs are used to develop programs which can then be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PFD1020 Field Demo System is available containing a PIC1665 with sockets for erasable PROMs. Finally, the PICES II (PIC In-Circuit Emulation System) provides the user with stand-alone emulation and debugging operation or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM.

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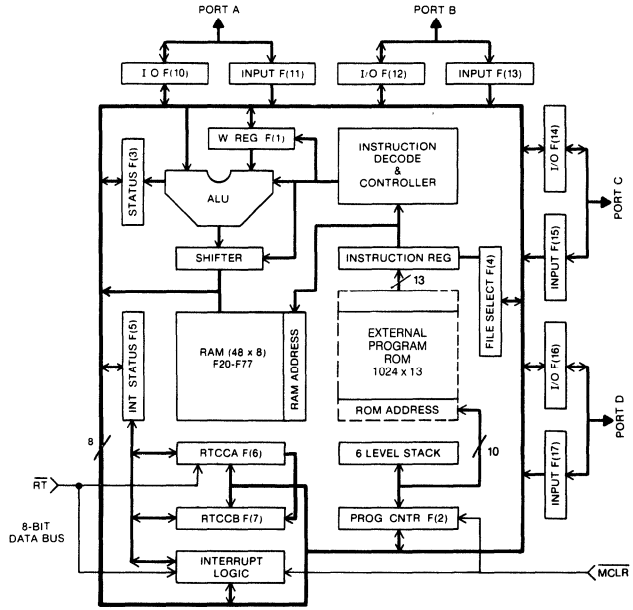
PIC1665 BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC1665 microcomputer is based on a register file concept with simple yet powerful instruction commands designed to optimize the code for bit, byte, and register transfer operations. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the functional blocks of the PIC1665 are connected by an 8-bit bidirectional bus: the 64 8-bit registers of which the first 16 are special purpose, an Arithmetic Logic Unit, and a user defined external PROM composed of 1024 x 13 bit words. The register file is divided into two functional groups: operational registers and general purpose registers. The first sixteen are the operational registers and they include the Real Time Clock/Counters A and B, four I/O registers, two Status registers, a Program Counter and a File Select Register. The general purpose registers are used for data and control information under command of the instructions.

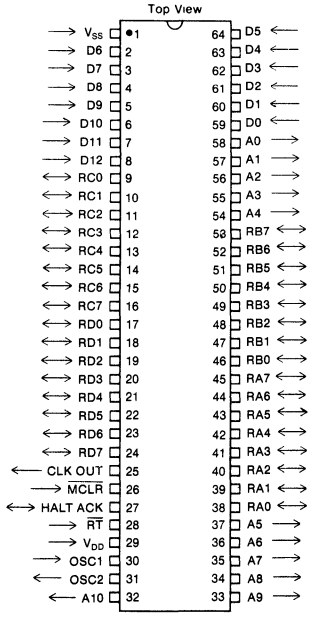
The Arithmetic Logic Unit contains one temporary working register (W Register), an adder, and hardware for decimal adjust. Manipulation between data in the working register and any other register can be performed.

The external PROM contains the user defined application program and is supported by an instruction decoder and instruction register. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. The Program Counter is modified by bit test, jump, call or branch instructions and the lower 8-bits can be modified for computed addresses by file register instructions. (Note: The upper 2 bits are not affected.) In addition, an on-chip six level stack is employed to push and pull the contents of the program counter. This provides easy to use subroutine nesting. Activating the $\overline{MCLR}$ input on power-up initializes the external ROM program to address 1777_8.

PIN FUNCTIONS

Signal	Function
OSC 1 (Input) OSC 2 (Output)	Oscillator pins. The on-board oscillator can be driven by an external crystal, an RC network, or an external clock via these pins.
$\overline{RT}$ (Input)	Real Time input. Negative transitions on this pin increments the RTCC (F6) register. This pin can also be used for an interrupt input. This pin uses a Schmitt trigger input. There is no internal active pull-up device.
RA0-RA7, RB0-RB7, RC0-RC7, RD0-RD7	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program.
$\overline{MCLR}$ (Input)	Master Clear. Used to initialize the internal ROM program to address 1777_8, latch all I/O registers high, and disable the interrupt system. This pin uses a Schmitt trigger input. There is no internal active pull-up device.
V_{DD}	Power supply pin.
V_{SS}	Ground pin.
CLKOUT	Clock Output. A signal derived from the internal oscillator. May be used by external circuitry to synchronize with PIC1665 timing.
HALT/ACK	Halt/Halt Acknowledge. This is a bidirectional I/O pin used in conjunction with CLKOUT. The pin is an input when CLKOUT is low, and an output when CLKOUT is high. Inputting a high when CLKOUT is low will suspend execution of the next instruction. No data is lost and after HALT/ACK is brought low execution proceeds exactly as if no halt signal had been applied. This pin can also be used to restart the PIC1665 after a HALT instruction (00001_8) has been executed. During the time CLKOUT is high, the pin will have an open drain output configuration and therefore requires an external pullup resistor. The output is high whenever the PIC1665 is halted either due to an active input to the HALT/ACK pin or the execution of the HALT instruction. HALT/ACK will output a low when the PIC1665 resumes execution of the program. This pin must be grounded when it is not used.
D0-D12 (Input)	Data input. These thirteen lines accept the thirteen bit PIC instruction codes generated by an external source. D0 is the LSB of the instruction.
A0-A10 (Output)	Address Output. These eleven lines represent the address of the next instruction to be executed by the PIC1665. They are capable of addressing up to 2048 words of memory. A0 is the LSB of the address.

PIN CONFIGURATION
64 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File Octal	Function
F0	Not a physical register. F0 calls for the contents of the FSR (F4) to be used to select a file register. F4 is used as an indirect address pointer.
F1	W Register — The working register.
F2	Program Counter — Points to the next program ROM address to be executed.
F3	Arithmetic Status Register 7 6 5 4 3 2 1 0 0 X A9 A8 OV Z DC C Bit 0 (C) — Bit 0 is the carry flag which is usually the carry from the A.L.U. It is also used as a borrow in subtract instructions. Bit 1 (DC) — Bit 1 is the half carry (decimal carry) and is used to indicate a carry from bit 3 in the A.L.U. as the result of an addition (byte). This bit is used in the decimal adjust instruction to allow B.C.D. decimal addition. Bit 2 (Z) — Bit 2 is the zero flag and is set to a one if the results of the previous operation was identically zero. Bit 3 (OV) — Bit 3 is the overflow flag, and is set to a one by operations which cause a signed two's complement arithmetic overflow. The bit is set when the carry from the MSB in the A.L.U. is opposite to the carry from the MSB-1 bit. Bit 4 (A8) — Bit 4 is the 9th bit of the program counter. This bit is a read only bit. Bit 5 (A9) — Bit 5 is the 10th bit of the program counter. This bit is a read only bit.
F4	File Select Register — The FSR is used in generating effective file register addresses under program control.
F5	Interrupt Status Register — Used to control interrupts and F6 and F7. X | CNTE | A/B | CNTS | RTCIR | XIR | RTCIE | XIE
F6,F7	RTCCA and RTCCB — Real Time Clock Counters A & B respectively can be arranged as two 8 bit registers, a single 16 bit register or two general purpose registers when no external counting is required. The RTCC registers can be loaded and read by the program, as well as count negative transitions on the RT pin or count at 1/8 the frequency of the oscillator. If data are being stored into RTCCA simultaneously with a negative transition on the RT pin (and CNTE = 1 and CNTS = 1), RTCCA will contain the new stored value and the external transition will be ignored by the microcomputer. (See the section "Real-Time Clock Interrupt" for further details about the RTCC registers.)
F10,11	I/O Port A
F12,13	I/O Port B
F14,15	I/O Port C
F16,17	I/O Port D
F20,77	General Purpose Registers—Used for temporary and general purpose storage during program execution time.

NOTE: F10, 12, 14 & 16 are the I/O registers and F11, 13, 15 & 17 are used for reading the actual pin levels.

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INTERRUPT SYSTEM

The interrupt system of the PIC1665 is comprised of an external interrupt and a real-time clock counter interrupt. These have different interrupt vectors, enable bits and status bits. Both interrupts are controlled by the status register (F5)** shown below.

NOT USED	CNTE	A/B	CNTS	RTCIR	XIR	RTCIE	XIE
7*	6	5	4	3	2	1	0

*Bit 7 is unused and is read as zero

**Register 5 will power up to all zeroes

EXTERNAL INTERRUPT

On any high to low transition on the $\overline{RT}$ pin the external interrupt request (XIR) bit will be set. This request will be serviced if the external interrupt enable (XIE) bit is set or if it is set at a later point in the program. The latter allows the processor to store a request (without interrupting) while a critical timing routine is being executed. Once external interrupt service is initiated, the processor will clear the XIR bit, delay one cycle (to execute the current instruction), then push the current program counter on to the stack and execute the instruction at location 1760_8. It takes three to four instruction cycles from the transition on the $\overline{RT}$ pin until the instruction at 1760_8 is executed. No new interrupts can be serviced until a return from interrupt (RETFI) instruction has been executed.

REAL-TIME CLOCK INTERRUPT

The real-time clock counter (RTCCA & RTCCB, file registers F6 and F7) have a similar mechanism of interrupt service. The RTCCA register will increment if the count enable (CNTE) bit is set. If this bit is not set the RTCCA & RTCCB will maintain their present contents and can therefore be used as general purpose RAM registers. The count source (CNTS) bit selects the clocking source for RTCCA. If CNTS is cleared to a '0', then RTCCA will use the internal instruction clock and increment at 1/8 the frequency present on the OSC pins. If CNTS is set to a '1', then RTCCA will increment on each high to low transition of the RT pin. RTCCB can only be incremented when RTCCA makes a transition from 377_8 to 0 and the A/B status bit is set. This condition links the two eight bit registers together to form one sixteen bit counter. An interrupt request under these conditions will occur when the combined registers make a transition from 177777_8 to 0. If, however, the A/B bit is not set, then RTCCA will be the only incrementing register and an interrupt request will occur when RTCCA makes a transition from 377_8 to 0. (In this setup the RTCCB register will not increment and can be used as a general purpose RAM register). Once a request has come from the real-time clock counter, the real-time clock interrupt request (RTCIR) bit will be set. At this point, the request can either be serviced immediately if the real-time clock interrupt enable (RTCIE) bit is set or be stored if RTCIE is not set. The latter allows the processor to store a real-time clock interrupt while a critical timing routine is being executed. Once interrupt service is initiated, the processor will clear the RTCIR bit, delay one cycle (to execute the current instruction), then push the present program counter on to the stack and execute the instruction at location 1740_8. It takes three instruction cycles from when the RTCC (A or B) overflows until the instruction at 1740_8 is executed. No new interrupts can be serviced until a RETFI instruction has been executed.

The RETFI instruction (00002_8) must be used to return from any interrupt service routine if any pending interrupts are to be serviced. External interrupts have priority over RTCC driven interrupt in the event both types occur simultaneously. Interrupts cannot be nested but will be serviced sequentially. The existence of any pending interrupts can be tested via the state of the XIR (bit 2) and RTCIR (bit 3) in the status word F5.

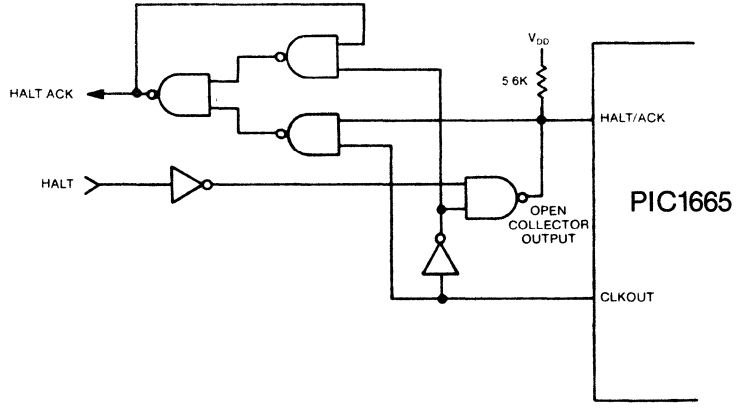
HALT OPERATION

Program execution in the PIC1665 can be suspended in two ways. The first is by applying a logic high input level on the HALT/ACK pin when CLKOUT is low The operation of the PIC1665 will be suspended until the HALT/ACK pin is brought low. At that point program execution will begin with the next instruction present on the Data Lines. Program execution can also be suspended using the HALT instruction. In order to restart the PIC1665 after execution of a HALT instruction, the $\overline{MCLR}$ pin must be brought low, or the HALT/ACK pin must be brought high for one complete cycle and then low again.

In both cases, when CLKOUT is high, the HALT/ACK pin will output a high level whenever the PIC1665 is in the halt mode provided an external pullup resistor is used.

When the PIC1665 is in the halt mode the RTCCA and RTCCB registers cannot be incremented by the internal clock, or by high to low transitions on the $\overline{RT}$ pin. If a high to low transition occurs on the $\overline{RT}$ pin, then the XIR bit (Bit 2 of file 5) will be set. If the XIE bit (bit 0 of file 5) is set, then an interrupt will occur immediately after program execution begins.

TYPICAL HALT CIRCUIT



MICROCOMPUTER

Basic Instruction Set Summary

Each PIC instruction is a 13-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator The file register designator specifies which one of the PIC file registers is to be utilized by the instruction The destination designator specifies where the result of the operation performed by the instruction is to be placed If "d" is zero, the result is placed in the PIC W register If "d" is one, the result is returned to the file register specified in the instruction

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located

For literal and control operations, "k" represents an eight or nine bit constant or literal value

For an oscillator frequency of 5MHz the instruction execution time is 2.0μsec, unless a conditional test is true or the program counter is changed as a result of an instruction In these two cases, the instruction execution time is 4.0 μsec.

BYTE ORIENTED FILE REGISTER OPERATIONS

(12-7)	(6)	(5-0)
OP CODE	d	f (FILE #)

Instruction—Binary (Octal)					Name	Mnemonic,	Operands	Operation	Status Affected
0 000	000	000	100	(00004)	Decimal adjust W	DAW	—	(Note 1)	C
0 000	001	fff	fff	(00100)	Move W to file	MOVWF	f	W→f	—
0 000	1d	fff	fff	(00200)	Subtract W from file w/borrow	SUBBWF	f,d	f+$\overline{W}$+c →d	OV,C,DC,Z
0 000	10d	fff	fff	(00400)	Subtract W from file	SUBWF	f d	f+$\overline{W}$ + 1→d	OV,C,DC,Z
0 000	11d	fff	fff	(00600)	Decrement file	DECF	f d	f - 1→d	OV,C,DC,Z
0 001	00d	fff	fff	(01000)	Inclusive or W with file	IORWF	f,d	WVf→d	Z
0 001	01d	fff	fff	(01200)	And W with file	ANDWF	f,d	W•f→d	Z
0 001	10d	fff	fff	(01400)	Exclusive OR W with file	XORWF	f d	W⊕f→d	Z
0 001	11d	fff	fff	(01600)	Add W with file	ADDWF	f,d	W+f→d	OV,C,DC,Z
0 010	00d	fff	fff	(02000)	Add W to file with carry	ADCWF	f d	W+f+c→d	OV,C,DC,Z
0 010	01d	fff	fff	(02200)	Complement file	COMPF	f d	$\overline{f}$→d	Z
0 010	10d	fff	fff	(02400)	Increment file	INCF	f d	f+1→d	OV,C,DC,Z
0 010	11d	fff	fff	(02600)	Decrement file, skip if zero	DECFSZ	f,d	f - 1→ d, skip if zero	—
0 011	00d	fff	fff	(03000)	Rotate file right thru carry	RRCF	f,d	f(n)→d(n−1), c→d(7), f(0)→c	C
0 011	01d	fff	fff	(03200)	Rotate file left thru carry	RLCF	f d	f(n)→d(n+1), c→d(0), f(7)→c	C
0 011	10d	fff	fff	(03400)	Swap upper and lower nibble of file	SWAPF	f d	f(0-3)⇌(4-7)→d	—
0 011	11d	fff	fff	(03600)	Increment file, skip if zero	INCFSZ	f d	f+1 →d, skip if zero	—

(12-6)	(5-0)
OP CODE	f (FILE #)

Instruction—Binary (Octal)				Name	Mnemonic,	Operands	Operation	Status Affected
1 000	000	fff	fff	(10000)	Move file to W	MOVFW	f	f→W	Z
1 000	001	fff	fff	(10100)	Clear file	CLRF	f	0→f	Z
1 000	010	fff	fff	(10200)	Rotate file right/no carry	RRNCF	f	f(n)→d(n−1), f(0), →f(7)	—
1 000	011	fff	fff	(10300)	Rotate file left/no carry	RLNCF	f	f(n)→d(n+1), f(7), →f(0)	—
1 000	100	fff	fff	(10400)	Compare file to W, skip if F < W	CPFSLT	f	f - W, Skip if C = 0	—
1 000	101	fff	fff	(10500)	Compare file to W, skip if F = W	CPFSEQ	f	f - W, Skip if Z = 1	—
1 000	110	fff	fff	(10600)	Compare file to W, skip if F > W	CPFSGT	f	f - W, Skip if $\overline{Z}$ • C = 1	—
1 000	111	fff	fff	(10700)	Move file to itself	TESTF	—	f→f	Z

BIT ORIENTED FILE REGISTER OPERATIONS

(12-9)	(8-6)	(5-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction—Binary (Octal)				Name	Mnemonic,	Operands	Operation	Status Affected
0 100	bbb	fff	fff	(04000)	Bit clear file	BCF	f,b	0→f(b)	—
0 101	bbb	fff	fff	(05000)	Bit set file	BSF	f,b	1→f(b)	—
0 110	bbb	fff	fff	(06000)	Bit test, skip if clear	BTFSC	f,b	Bit Test f(b) skip if clear	—
0 111	bbb	fff	fff	(07000)	Bit test, skip if set	BTFSS	f b	Bit Test f(b) skip if set	—

LITERAL AND CONTROL OPERATIONS

(12-8)	(7-0)
OP CODE	k (LITERAL)

Instruction—Binary (Octal)				Name	Mnemonic,	Operands	Operation	Status Affected
0 000	000	000	000	(00000)	No Operation	NOP	—	—	—
0 000	000	000	001	(00001)	Halt in PIC1665	HALT	—	—	—
0 000	000	000	010	(00002)	Return from Interrupt	RETFI	—	Stack → PC	—
0 000	000	000	011	(00003)	Return from Subroutine	RETFS	—	Stack → PC	—
1 001	0kk	kkk	kkk	(11000)	Move Literal to W	MOVLW	k	k→W	—
1 001	1kk	kkk	kkk	(11400)	Add Literal to W	ADDLW	k	k+W→W	OV,C,DC,Z
1 010	0kk	kkk	kkk	(12000)	Inclusive OR Literal to W	IORLW	k	kVW→W	Z
1 010	1kk	kkk	kkk	(12400)	And Literal and W	ANDLW	k	k•W→W	Z
1 011	0kk	kkk	kkk	(13000)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z
1 011	1kk	kkk	kkk	(13400)	Return and load literal in W	RETLW	k	k→W, Stack →PC	—

(12-10)	(9-0)
OP CODE	k (LITERAL)

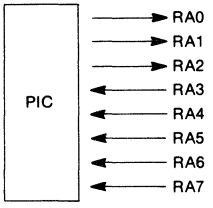
Instruction—Binary (Octal)				Name	Mnemonic,	Operands	Operation	Status Affected
1 10k	kkk	kkk	kkk	(14000)	Go to address	GOTO	k	k→PC	—
1 11k	kkk	kkk	kkk	(16000)	Call Subroutine	CALL	k	PC+1→Stack, k→PC	—

Note 1:
DAW: Decimal Adjust W
This instruction adjusts the eight bit number in the W register to form two valid BCD (binary coded decimal) digits,one in the lower and one in the upper nibble (The results will only be meaningful if the number in W to be adjusted is the result of adding together two valid two digit BCD numbers.)

The adjustment obeys the following two step algorithm.
1. If the lower nibble is greater than 9 or the digit carry flag (DC) is set, 06 is added to the W register.
2. Then, if the upper nibble is greater than 9 or the carry from the original or step 1 addition is set, 60 is added to the W register. The carry bit is set if there is a carry from the original, step 1 or step 2 addition

INPUT/OUTPUT CAPABILITY

The PIC1665 provides four complete quasi-bidirectional input/output ports. A simplified schematic of an I/O pin is shown below. The ports occupy address locations in the register file space of the PIC1665. Thus, any instruction that can operate on a general purpose register can operate on an I/O port. Two locations in the register file space are allocated for each I/O port. Port RA0-7 is addressable as either F10 or F11. Port RB0-7 is addressable as either F12 or F13. Port RC0-7 is addressable as either F14 or F15 and Port RD0-7 is addressable as either F16 or F17. An I/O port READ on its odd-numbered location will interrogate the chip pins while an I/O port READ on its even-numbered location will interrogate the internal latch in that I/O port. This simplifies programming in cases where a portion of a single port is used for inputting only, while the remainder is used for outputting as illustrated in the following example.



Here, the low 3 bits of port RA are used as output-only, while the high 5 bits are used as input-only. During power on reset ($\overline{MCLR}$ low), the latches in the I/O ports will be set high, turning off all pull down transistors as represented by Q_2 in Figure 1. During program execution if we wish to interrogate an input pin, then, for example,

```
BTFSS 11,6
```

will test pin RA6 and skip the next instruction if that pin is set. If we wish to modify a single output, then, for example,

```
BCF 10,2
```

will force RA2 to zero because its internal latch will be cleared to zero. This will turn on A_2 and pull the pin to zero.

The way this instruction operates internally is the CPU reads file 10 into the A.L.U., modifies the bit and re-outputs the data to file 10. If the pins were read instead, any input which was grounded externally would cause a zero to be read on that bit. When the CPU re-outputted the data to the file, that bit would be cleared to zero, no longer useful as an input until set high again.

During program execution, the latches in bits 3-7 should remain in the high state. This will keep A_2 off, allowing external circuitry full control of pins RA3-RA7, which are being used here as input.

BIDIRECTIONAL INPUT-OUTPUT PORT

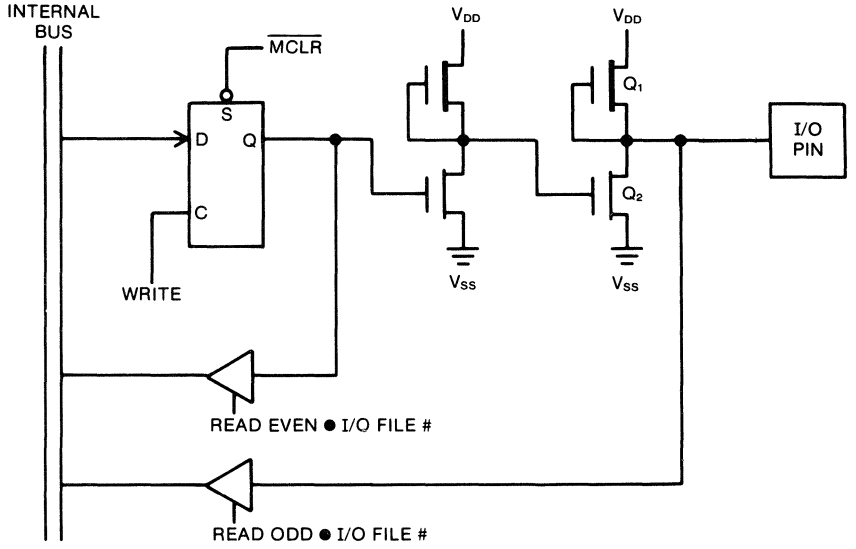


Figure 1

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Ambient Temperature Under Bias ..... 70°C
Storage Temperature ..... −55°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... −0.3V to +10.0V
Power Dissipation 1000mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ†	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	5.5	V	
Primary Supply Current	I_{DD}	—	—	100	mA	All I/O pins high
Input Low Voltage (except $\overline{MCLR}$ & $\overline{RT}$)	V_{IL}	0.2	—	0.8	V	
Input High Voltage (except MCLR, RT, OSC1)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RT}$, OSC1)	V_{IH2}	$V_{DD}-1$	—	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	I_{OH} = −100μA provided by internal pullups (Note 2)
Output Low Voltage (I/O, A0-A9, HALT ACK, CLK OUT)	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Input Leakage Current ($\overline{MCLR}$, $\overline{RT}$,OSC1)	I_{LC}	−5	—	+5	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Input Low Current (all I/O ports)	I_{IL}	0.2	0.6	−2.0	mA	V_{IL} = 0.4V, internal pullup
Input High Current (all I/O ports)	I_{IH}	0.1	0.4	—	mA	V_{IH} = 2.4V

† Typical data is at T_A = 25°C, V_{DD} = 5.0V.

NOTES:

1. Total power dissipation for the package is calculated as follows:
   $P_D = (V_{DD})(I_{DD}) + \Sigma (V_{DD} - V_{IL})(I_{IL}) + \Sigma (V_{DD} - V_{OH})(I_{OH}) + \Sigma (V_{OL})(I_{OL})$.
2. Positive current indicates current into pin. Negative current indicates current out of pin.
3. Total I_{OL} for all output pin (I/O ports plus CLK OUT) must not exceed 175mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

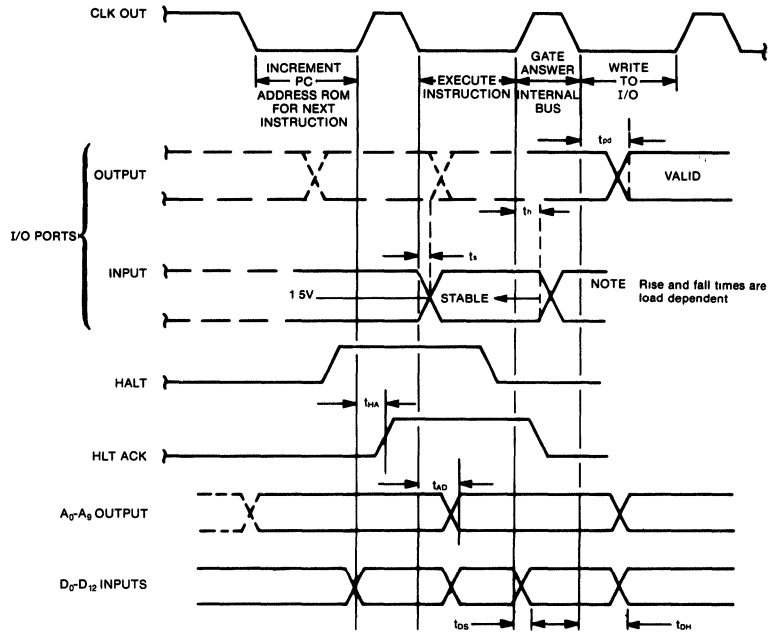
Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{cy}	2.0	—	8	μs	4MHz—.1MHz external time base (Note 1)
$\overline{RT}$ Input						(Note 2)
Period	t_{RT}	t_{CY}+0.2μs	—	—	—	(Notes 2 and 3)
High Pulse Width	t_{RTH}	½t_{RT}	—	—	—	
Low Pulse Width	t_{RTL}	½t_{RT}	—	—	—	
I/O Ports						
Data Input Setup Time	t_s	—	—	¼t_{cy}−125	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	500	800	ns	Capacitive load = 50pF
HALT ACK Output Propagation Delay	t_{HA}	—	200	—	ns	
A0-A9 Output Propagation Delay	t_{AD}	—	350	—	ns	
D0-D12 Input Set-Up Time	t_{DS}	0	—	—	ns	
D0-D12 Input Hold Time	t_{DH}	200	—	—	ns	

NOTES:

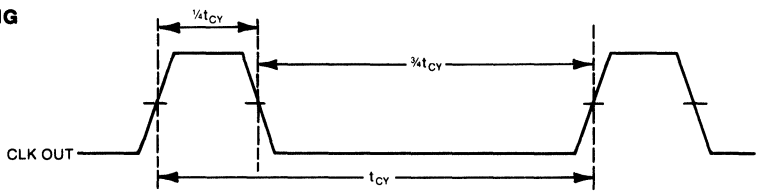
1. Instruction cycle period (t_{cy}) equals eight times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RT}$ input, CLK OUT may be directly tied to the $\overline{RT}$ input. The minimum times specified represent theoretical limits.
3. The maximum frequency which may be input to the $\overline{RTCC}$ pin is calculated as follows: $f_{(max)} = \frac{1}{t_{RT\,(min)}} = \frac{1}{t_{CY\,(min)} + 0.2\mu s}$
   For example: if t_{CY} = 4μs, $f_{(max)} = \frac{1}{4.2\mu s}$ = 238KHz.

MICROCOMPUTER

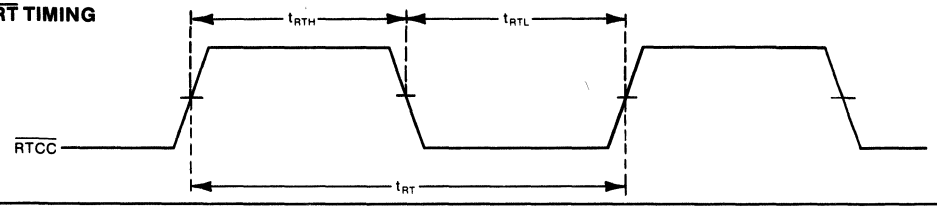
I/O TIMING



CLK OUT TIMING

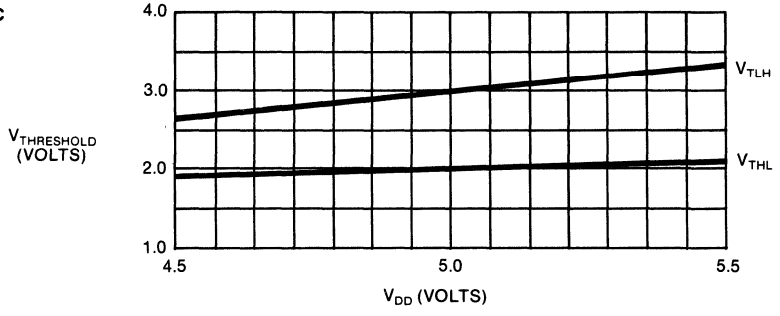


$\overline{RTCC}$/$\overline{RT}$ TIMING



SCHMITT TRIGGER CHARACTERISTICS (Typical)

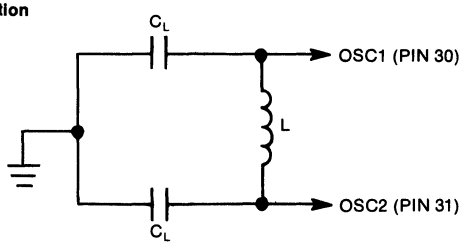
($\overline{RT}$, $\overline{MCLR}$) T_A = 25°C



MICROCOMPUTER

PIC1665 OSCILLATOR OPTIONS (Typical Circuits)

LC Operation

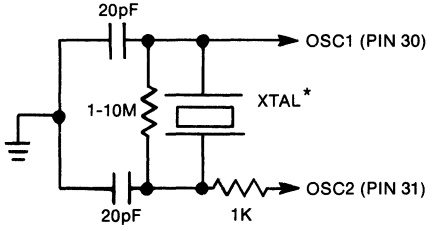


$$f_{OSC} \approx \frac{1}{2\pi \sqrt{L\,(C_L + C_{INT})}},$$

where $C_{INT} = 10pF$.

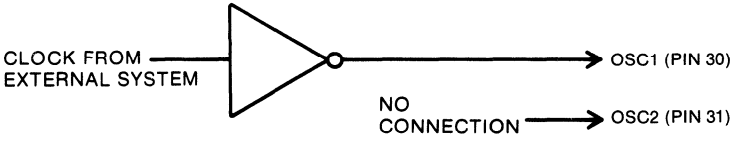
Typical values for 4MHz operation:
$L \approx 70\mu H$
$C_L = 10pF$

CRYSTAL INPUT OPERATION

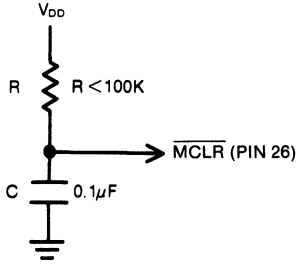


* or ceramic resonator, parallel resonant (0.8 - 5.0MHz).

EXTERNAL CLOCK INPUT OPERATION

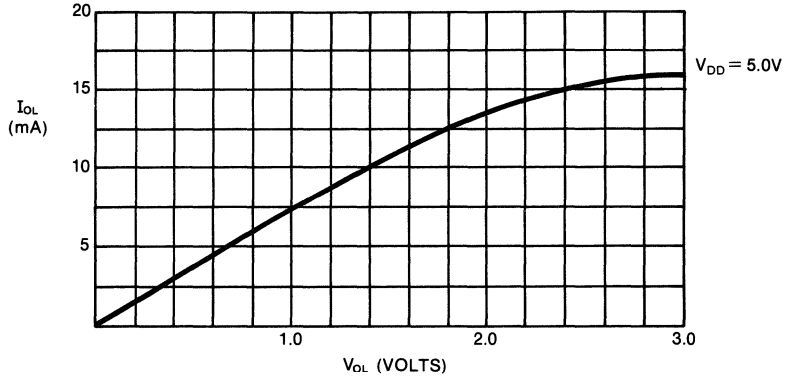


MASTER CLEAR (Typical Circuit)



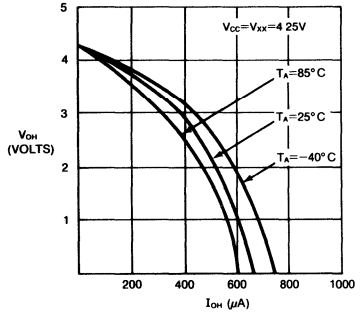
Master Clear requires 10ms delay (assuming a 5MHz crystal) before activation after power is applied to the V_{DD} pin, for the crystal to start up. To achieve this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

OUTPUT SINK CURRENT GRAPH



The Output Sink Current is dependent on the output load. This chart shows the typical curve used to express the output drive capability.

V_{OH} VS I_{OH} (I/O PORTS)



GENERAL INSTRUMENT

PICAL/PICES II

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
PIC ASSEMBLER	Converts symbolic source programs for PIC series into object code.	PICAL	4-132
PIC DEVELOPMENT SYSTEM	In-circuit emulation and debug system—stand alone or peripheral.	PICES II	4-134

PIC Cross Assembler

FEATURES

- Symbolic machine operation codes (opcodes, mnemonics)
- Symbolic address assignment and reference
- Relative addressing
- Data creation statements
- Storage reservation statements
- Assembly listing control statements
- Character codes may be specified as ASCII or EBCDIC
- Addresses can be generated as constants
- Comments and remarks may be encoded for documentation
- Cross reference table listing

DESCRIPTION

The PICAL Cross Assembler is used for the General Instrument family of microcomputers including the PIC1650A, 1654, 1655A, 16C55, 1656, 1670, 1671 and 1672. The function of this Cross Assembler program is to translate the Symbolic Code into the machine code required by the actual processors. The assembler program is written in Fortran IV to achieve compatibility with most computer systems, including those manufactured by DEC, Data General, Hewlett-Packard, Xerox, and others. It is modular and may be executed in an overlay mode should memory restrictions make that necessary. The program is approximately 3850 Fortran card images in length, 20% of which are comments. The program is written in ANSI standard Fortran IV and no facility peculiar to one machine was utilized. This was done in order to eliminate Fortran compatibility problems.

The mnemonic Operation Codes are identical to those used in other PIC literature and in other software products. This has been done to eliminate any possible problems of program compatibility and to obviate the necessity of learning new assembly languages. In addition, several directives and features are implemented and described in the PICAL Users Manual.

The assembler is a two pass program that builds a symbol table, issues helpful error messages, produces an easily read program listing and symbol table, and creates an object and symbol table module.

The assembler features macro capability, symbolic and relative addressing, forward references, complex expression evaluation, cross reference listing and a versatile set of directives.

The assembler program, written in Fortran, is usually supplied as 9 track, 1600 BPI, 80 column card image records, unblocked and unlabeled magnetic tapes in either EBCDIC or ASCII code. The label on the tape reel will clearly specify the information.

The program is also supplied in compiled version for appropriate media and machines, including the Data General/μNova® system.

ASSEMBLER LANGUAGE

An assembly language program is written in symbolic machine language. It is comprised of statements. A statement is either a symbolic instruction, a directive statement, a macro statement, or a comment.

The symbolic machine instruction is a written specification for a particular machine operation expressed by symbolic operation codes and sometimes symbolic addresses or operands.

A directive statement is a statement which is not translated into a machine instruction, but rather is interpreted as a directive to the assembler program.

Statements are always written in a particular format. This format is depicted below.

LABEL FIELD	OPERATION FIELD	OPERAND FIELD	COMMENT FIELD

SYNTAX

The Assembler Language is a language like any other. That is, it has a character set, vocabulary, rules of grammar, and allows for individuals to define new words or elements. The rules that describe the language are termed the syntax of the language.

For an expression or statement in assembler language to be translated by the assembly program it must be written correctly in accord with the rules of syntax.

A **symbol** is a sequence of characters. The first character in a symbol must be alphabetic or the special characters ?, $, or &. Special characters except for the above three may not be used in a symbol. Imbedded blanks are not permitted. The user is cautioned not to use symbols that start with the ? character as the assembler generates "local" symbols starting with this character.

Only the first six characters of a symbol are used by the Assembler to define that symbol; the remaining characters are for documentation. The parameter that dictates the number of characters used to define a symbol may be changed in the Fortran Source code.

A **constant** is an invariant quantity. It may be an arithmetic value or a character code. There are several ways of specifying constants in this assembler language.

Octal constants may be defined as a sequence of numeric characters optionally preceded by a plus sign or a minus sign. If unsigned, the value is assumed to be positive. Decimal constants are defined in the same manner but preceded by a decimal point.

In most cases constants must be contained in one 8 bit word. A constant can contain an unsigned number with a value from 0 to 255. When a constant is negative its equivalent two's complement representation is generated and placed in the field specified. An eight bit two's complement number can range from −128 to +127. Whenever an attempt is made to place a constant in a field for which it is too large, an error message is generated by the assembler.

An **expression** is a sequence of one or more symbols, constants, or other expressions separated by the arithmetic operators +, −, *, /. Parentheses are used in the normal manner to establish the correct order of the arithmetic operators. Expressions are evaluated left to right with multiplication and division being performed before addition and subtraction.

The expression must resolve to a single unique value. All expressions are evaluated modulo 65536 and hence are all 16 bit quantities. In most cases the value of the final expression must be contained in a 12 bit word.

DIRECTIVES

The directives or pseudo-operations are written as ordinary statements in the assembler language, but rather than being translated into equivalent machine language, they are interpreted as commands to the assembler itself.

Through use of these directives, the Assembler will reserve memory space, define bytes of data, control the listing, assign values to symbols, etc.

The directives are:

ORG	Set Program Origin
END	End of Assembly
EQU	Equate a Symbol to an Expression
SET	Set a Symbol equal to an Expression
DATA	Data Definition
RES	Reserve Storage
ZERO	Reserve Storage and fill with zeros
PAGE	Advance Listing Form to next page
SPAC	Space lines on listing
TITLE	Set Program Heading
LIST	List the Elements Specified
OPTION	Set Program Options (same as LIST)
NLIST	Suppress listing of the Elements Specified
IF	Conditional Assembly Statement
ELSE	Conditional Assembly Statement Converse
ENDIF	End Conditional Assembly Code

MACROS

A macro is a sequence of instructions that can be inserted in the assembly source text by encoding a single instruction, the macro call. The macro definition is written only once and can be called any number of times. The macro definition may contain parameters which can be changed for each call. The macro facility simplifies the coding of programs, reduces the chance of programmer error, and makes programs easier to understand as the source code need only be changed in one location, the macro definition.

A macro definition consists of three parts: a heading, a body, and a terminator. This definition must precede any macro call. A macro may be redefined at any time with the latest definition of a macro name applying to a macro call. A standard assembler mnemonic (e.g. CLRF) may also be redefined by defining a macro with the name CLRF. In this case all subsequent uses of the CLRF instruction in the program will cause the macro to be expanded.

The PIC assembler which is precompiled for the Intel MDS® does not have a MACRO capability due to the possibly limited memory space available.

USING THE ASSEMBLER

The Assembler is written entirely in Fortran and is comprised of a main program and several subroutines. The main program appears first on the tape and the last subroutine is followed by a tape mark. The Assembler may be compiled from the tape.

The Assembler should be compiled and its object module stored on some secondary storage device. If desired, the Assembler may be compiled and linked to perform in the overlay mode. Communications between subprograms is via blank common and subroutine call parameters.

The Assembler is a two pass Assembler wherein the source code is scanned twice. During the first pass the labels are examined and placed into a symbol table. Certain errors may be detected during Pass One; these will be displayed on the output listing.

During Pass Two, the object code is completed, symbolic addresses resolved, a listing and object module are produced. Certain errors, not detected during Pass One may be detected and displayed on the listing.

At the end of the Assembly process a symbol table or cross reference table may be displayed.

The following steps are taken to assemble a source program:

1. Write a program utilizing the instruction mnemonics of the PIC Instruction Set and directives. Encode the argument fields with constants, labels, symbolic addresses, etc.
2. Transfer the source program to some computer readable medium; cards, tape, etc. This medium should correspond to the input device expected by the Assembler. On some systems device assignments may be changed during the course of an assembly by utilizing proper system control cards.
3. Load the source code.
4. Execute the Assembler Program.
5. Get listing and object module as output.

During Pass Two of the assembly process a program listing is produced. The listing displays all information pertaining to the assembled program, both assembled data and the users original source statements.

The listing may be used as a documentation tool through the inclusion of the comments and remarks that describe the function of the particular program segment.

The main purpose of the listing is to convey all pertinent information about the assembled program, i.e. the memory addresses and their contents. The load module, also produced during Pass Two, contains the address and content information but in a format that can be read by people only with great effort.

TYPICAL ASSEMBLER LISTING

```
LINE    ADDR   B1    B2       TEST CHECKSUM

   1                            TITLE  'TEST CHECKSUM'
   2                            LIST   P=1655,X,E
   3  000000  0000          START  NOP
   4  000001  0000  0000          MOV    F0
*** OPCODE ERROR
   5  000003  0070                MOVWF  30
   6  000004  0041          START2 MOVWF  1
   7  000005                START3
   8  000005  0043                MOVWF  3
   9                            ORG    20
  10  000020  0001  0002          DATA   1,2,3
  11  000022  0003
  12  000023                      RES    2
  13  000025                      ZERO   3
  14                              IF     START
  15                              IORWF  FA
  16                              ADDWF  F10
  17                              ELSE
  18  000030  0551                ANDWF  F9
  19                              ENDIF
  20  000031  0041                MOVWF  1
  21  000032  0043                MOVWF  3
  22  000033  0044                MOVWF  4
  23  000034  5002                GOTO   START+2
  24                              ORG    30
  25  000030  5030                GOTO   1
  26  000031  6031                MOVLW  1
  27  000032  0041                MOVWF  1
  28  000033  0042                MOVWF  2
  29  000034  0043                MOVWF  3
  30  000035  0044                MOVWF  4
  31  000036  0045                MOVWF  5
*** INVALID FILE REGISTER
  32  000037  0047                MOVWF  7
  33  000040  0050                MOVWF  10
  34
  35  000041  1005                MOVF   5,W
  36  000042  1006                MOVF   6,W
*** INVALID FILE REGISTER
  37  000043  1047                MOVF   7
  38  000044  1010                MOVF   10,F
  39
  40  000045  3345                BTFSC  5,7
  41  000046  3005                BTFSC  5,0
  42  000047  3006                BTFSC  6,0
*** INVALID FILE REGISTER
  43  000050  3346                BTFSC  6,7
*** INVALID FILE REGISTER
  44  000051  3007                BTFSC  7,0
  45  000052  3347                BTFSC  7,7
  46  000053  3010                BTFSC  10,0
  47  000054  3350                BTFSC  10,7
  48
  49
  50                              ORG    777
  51  000777  5000                GOTO   START
  52
  53
  54  001000                      END

  ASSEMBLER ERRORS =    5
```

USERS MANUAL

A complete description of the PICAL Cross Assembler program with detailed explanations of how it is used is contained in the PICAL Users Manual.

PIC In-Circuit Emulation System

FEATURES

- Complete in-circuit emulation and debug capability
- Multiple system configurations to match user requirements
- Standard serial interface for system integration
- Powerful 16-bit microprocessor for system control
- Multiple breakpoints, single step, program trace and editing capabilities
- On-board diagnostics for system hardware troubleshooting

DESCRIPTION

The PICES II is an in-circuit emulation and debug system designed to provide the user with a complete tool for testing, troubleshooting, and modifying both the software program for the PIC circuit as well as the total system application. The PICES II is a self-contained unit which can operate in a stand-alone configuration or as a peripheral device to a host processor.

ARCHITECTURE

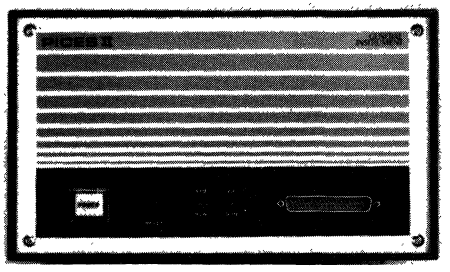
The PICES II system contains two processors. The User Processor is a ROM-less PIC microcomputer with external RAM. With the RAM loaded with the user's application program, the ROM-less PIC emulates the operation of the entire PIC family. An 18, 28 or 40 pin in-circuit emulation cable attaches the ROM-less PIC to the application system. The Control Processor is a CP1600 sixteen bit microprocessor with 12K of program ROM and 2K of RAM. This processor controls the functions of the PICES II including I/O interfacing, manipulation of the User Processor and interpretation and execution of the PICES II command set.

OPERATION

STAND-ALONE MODE: The PICES II is attached directly to a serial I/O device; typically a teletype. The user program is entered either using the paper tape reader/punch unit on the teletype or by manually setting each location in the PIC program memory to the desired value. Once the program memory is loaded, all PICES II emulation and debug commands can be issued on the teletype keyboard and PICES II responses are returned on the teletype printer. The serial interface can be either RS232C or current loop and the baud rate is switch selectable.

PERIPHERAL MODE: The PICES II can be configured such that the unit itself is peripheral to another computer system. The PICES II can be attached as an additional peripheral device or in series with the system TTY or CRT device. In this mode the user's computer facility can become a one station total development system. The computer text editor is used to develop the PIC source code. The Fortran PIC cross assembler will translate this source code into PIC machine code; the machine code is then downloaded into the PICES II. All PICES II commands are entered through the system terminal. Minor modifications can be done directly to the PICES II. Major changes require re-editing the source code, re-assembling and loading of the PICES II.

PIC IN-CIRCUIT EMULATION SYSTEM

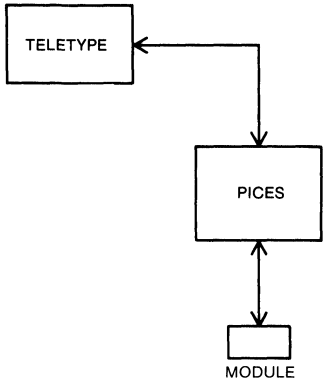


DATA MANUAL

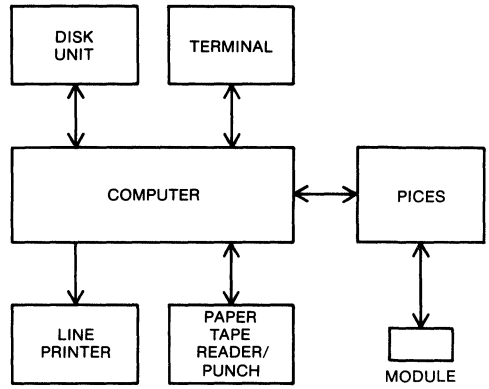
A detailed PICES II Data Manual is available. This manual describes the installation and operation of the PICES II system. Included in the manual are explanations of the command set with examples for illustration.

PICES II CONFIGURATIONS

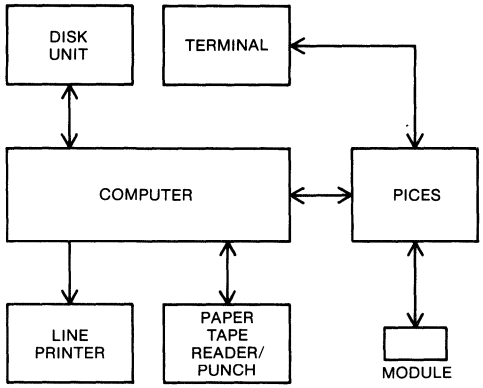
STAND ALONE MODE



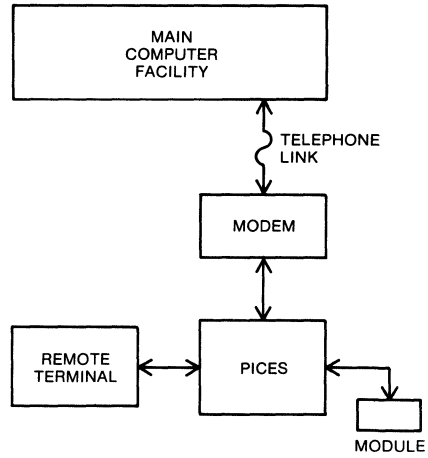
PERIPHERAL CONFIGURATION A



PERIPHERAL CONFIGURATION B



PERIPHERAL CONFIGURATION C



MICROCOMPUTER

GENERAL INSTRUMENT

PIC Field Demo Systems

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
PIC FIELD DEMO SYSTEMS	Contains PIC microcomputer, PROMs and provisions for on-board RC oscillator or external clock.	PFD Systems	4-138

PIC Field Demo Systems

FEATURES

- Single +5V operation
- On-board clock
- Optional external clock and reset
- Program storage in EPROM
- Dimensions: 4" x 4⅜"
- In circuit emulation cable length: 14"

DESCRIPTION

The PIC Field Demo Systems provide the user with a compact and portable method of evaluating and demonstrating application performance before the commitment is made to ROM masking of the PIC circuit. The PFD systems consist of a single printed circuit module containing a ROM-less PIC microcomputer with external Erasable/Programmable Read Only Memory (EPROM) attached. The EPROM contains the user's application program. An 18, 28 or 40 lead ribbon cable attaches to the PFD Module terminating with a DIP plug providing emulation of the PIC circuit in the application.

Provision for jumper options on the PFD Series module allows the user to select various modes of operation as appropriate to the application. Internal or external clock and power supply is available.

ORDERING INFORMATION

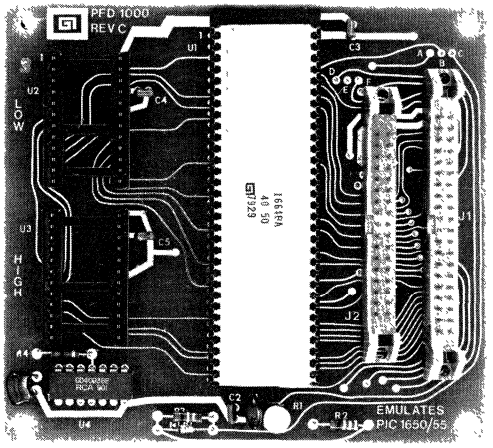
The PFD Module comes complete with a ROM-less PIC microcomputer. EPROMs and an in-circuit-emulation cable. Order the module to emulate the particular PIC circuit to be emulated.

TARGET MICROCOMPUTER	PFD SYSTEM
PIC1650	PFD1000
PIC1654	PFD1007
PIC1655	PFD1000
PIC1656	PFD1010
PIC16C55	PFD2010
PIC1670	PFD1020

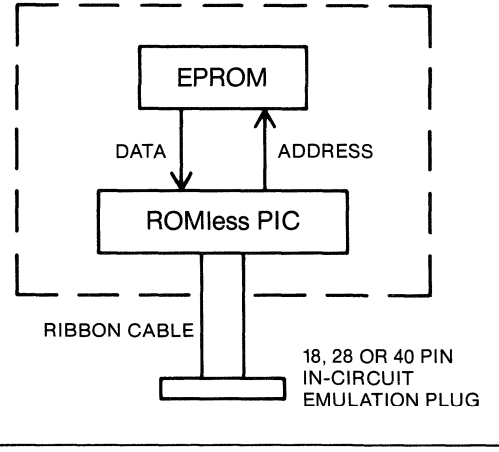
DATA MANUAL

A complete description of the PFD systems are contained in the PIC Field Demo Systems Data Manual.

PIC FIELD DEMO SYSTEM



PFD1000 (TYPICAL)



MICROCOMPUTER

EXTENDED TEMPERATURE RANGE

PIC series microcomputers are available in two temperature ranges. The preceding data sheets describe the commercial grade device, 0°C to 70°C centigrade. An industrial/automotive temperature range version is available. The −40° to 85° centigrade option is specified with the addition of a suffix, I, to the part number.

The specifications for these devices differ from their commercial grade counterparts in a few electrical parameters, typically interface voltage/current levels. Refer to the data sheets for details.

OPEN DRAIN OPTIONS

PIC1650A, PIC1670

Open-Drain I/O Ports

Any or all of the I/O lines may be specified by the customer to be open drain, that is, the internal pull-up device will be removed. This enables the outputs to be pulled up to +10.0V maximum with an external pull-up resistor, allowing easy interface to external devices requiring a logic one level greater than V_{DD} of the PIC. In the logic one state, the leakage current of the I/O port is ± 5μA, maximum.

The customer shall specify on the "PIC Series Order Form" the pin number and port name (e.g., "RB3") of each port required to be open drain.

PIC1655A, PIC1656

Open Drain I/O, Input and Output Ports

Any or all of the I/O, input only or output only lines may be specified by the customer to be open drain, that is, the internal pull-up device will be removed. This enables the outputs to be pulled up to +10.0V maximum with an external pull-up register, allowing easy interface to external devices requiring a logic one level greater than V_{DD} of the PIC. In the logic one state, the leakage current of the I/O port is ±5μA, maximum.

The customer shall specify on the "PIC Series Order Form" the pin number and port name (e.g., "RB3") of each port required to be open drain.

PIC16C55

Input-only, Output-only and I/O Ports

Any or all of the input-only and I/O lines may be specified to have an internal pull-up resistor inserted via a mask option. This allows easy interface to an external transistor or switch without the need for an external pull-up resistor. Furthermore, any or all of the output-only or I/O pull-down transistors can be specified to be removed via a mask option. This facilitates interfacing with external circuitry which has signal swings below V_{SS}. In this case the maximum voltage permitted to be applied to the pin is −12V with respect to V_{DD}.

PIC1654

Optional Internal Connection to RTCC

A mask option will allow an internal clock signal whose period is equal to the instruction execution time to drive the real time clock/counter register. In this mode, transitions in the $\overline{RTCC}$ pin will be disregarded.

PIC1655XT

Prescaler Division Ratio

A mask option will allow the division ratio of the RTCC prescaler to be selected as 1, 2, 4, 8 or 16. Consult the data sheet for the details.

GENERAL INSTRUMENT

PIC SERIES ORDER FORM

Customer Name _____

Address _____

City _____ State _____ Zip _____ Country _____

Telephone Number _____ Ext. _____

Customer Contact _____ Title _____ Date _____

PIC PART NUMBER _____

CUSTOMER MARKING REQUIREMENT: STANDARD ☐ SPECIAL ☐ _____

PIC TEMPERATURE RANGE SELECTION:

0°C to 70°C ☐ −40°C to 85°C ☐

OPEN DRAIN OPTION:

Are any pins to have their internal pull-up resistor removed? (In the case of PIC16C55, are any input-only or I/O pins to have an internal pull-up resistor inserted?) YES ☐ NO ☐

In the case of the PIC16C55, are any output-only or I/O pins to have the internal pull-down transistor removed. YES ☐ NO ☐

If the answer to any of the above questions is yes, please complete the chart below for all I/O pins. YES ☐ NO ☐

PIN NUMBER	FILE/ BIT	NO INTERNAL PULL-UP RESISTOR	NO INTERNAL PULL-DOWN TRANSISTOR (PIC16C55 ONLY)	STD.	PIN NUMBER	FILE/ BIT	NO INTERNAL PULL-UP RESISTOR	NO INTERNAL PULL-DOWN TRANSISTOR (PIC16C55 ONLY)	STD.

MICROCOMPUTER

PIC1650A and PIC1655A ONLY

Oscillator Pull-Down Transistor: Normal Operation ☐ External Clock (Transistor Removed) ☐

PIC1655XT ONLY

Mask Programmable Prescaler: 1 ☐ 2 ☐ 4 ☐ 8 ☐ 16 ☐

PIC1654 ONLY

Internal RTCC-CLK OUT Connection: Yes ☐ No ☐

PROGRAM ROM PATTERN MEDIA: Paper Tape _____ Prom _____

Customer Purchase Order Number _____

Customer Signature _____

Audio 5

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
		Speech Synthesis	
NARRATOR™ SPEECH PROCESSOR	Natural speech, stand alone operation, wide operating voltage, expandable ROM, simple interface.	SP0256	5-5
		SP0256-AL2	5-9
		SP0232	5-9
		SPR000	5-9
VOICE SYNTHESIS MODULE	Complete speech system, 16 seconds of speech, custom vocabularies, simple interface, 5V operation.	VSM2032	5-10
SPEECH SYNTHESIZER	High quality speech, programmable filter, 5V operation, simple interface, double buffered input	SP0250	5-12
SPEECH FIELD DEVELOPMENT BOARD	5V operation, expandable EPROM, multiple speech synthesis, on-board oscillator.	SFD2000	5-15
		Sound Generation	
PROGRAMMABLE SOUND GENERATOR	Full software control, 5V operation, simple interface, triple analog output, general purpose I/O ports.	AY-3-8910	5-18
		AY-3-8912	5-18
		AY-3-8913	5-18
TUNES SYNTHESIZER	Produces musical tunes from pre-programmed microcomputer.	AY-3-1350	5-26

AUDIO

Speech Synthesis

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
NARRATOR™ SPEECH PROCESSOR	Natural speech, stand alone operation, wide operating voltage, expandable ROM, simple interface.	SP0256	5-5
		SP0256-AL2	5-9
		SP0232	5-9
		SPR000	5-9
VOICE SYNTHESIS MODULE	Complete speech system, 16 seconds of speech, custom vocabularies, simple interface, 5V operation.	VSM2032	5-10
SPEECH SYNTHESIZER	High quality speech, programmable filter, 5V operation, simple interface, double buffered input.	SP0250	5-12
SPEECH FIELD DEVELOPMENT BOARD	5V operation, expandable EPROM, multiple speech synthesis, on-board oscillator.	SFD2000	5-15

Narrator™ Speech Processor

FEATURES

- Natural Speech
- Stand Alone Operation with Inexpensive Support Components
- Wide Operating Voltage
- Word, Phrase, or Sentence Library, ROM Expandable
- Expandable to 491K of ROM Directly
- Simple Interface to Most Microcomputers or Microprocessors
- Supports L.P.C. Synthesis: Formant Synthesis: Allophone Synthesis

GENERAL DESCRIPTION

The SP0256 (Speech Processor) is a single chip N-Channel MOS LSI device that is able, using its stored program, to synthesize speech or complex sounds.

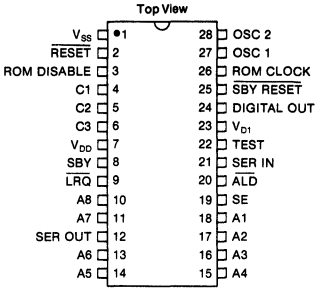
The achievable output is equivalent to a flat frequency response ranging from 0 to 5KHz, a dynamic range of 42dB, and a signal to noise ratio of approximately 35dB.

The SP0256 incorporates four basic functions:

- A software programmable digital filter that can be made to model a VOCAL TRACT.
- A 16K ROM which stores both data and instructions (THE PROGRAM).
- A MICROCONTROLLER which controls the data flow from the ROM to the digital filter, the assembly of the "word strings" necessary for linking speech elements together, and the amplitude and pitch information to excite the digital filter.
- A PULSE WIDTH MODULATOR that creates a digital output which is converted to an analog signal when filtered by an external low pass filter.

PIN CONFIGURATION

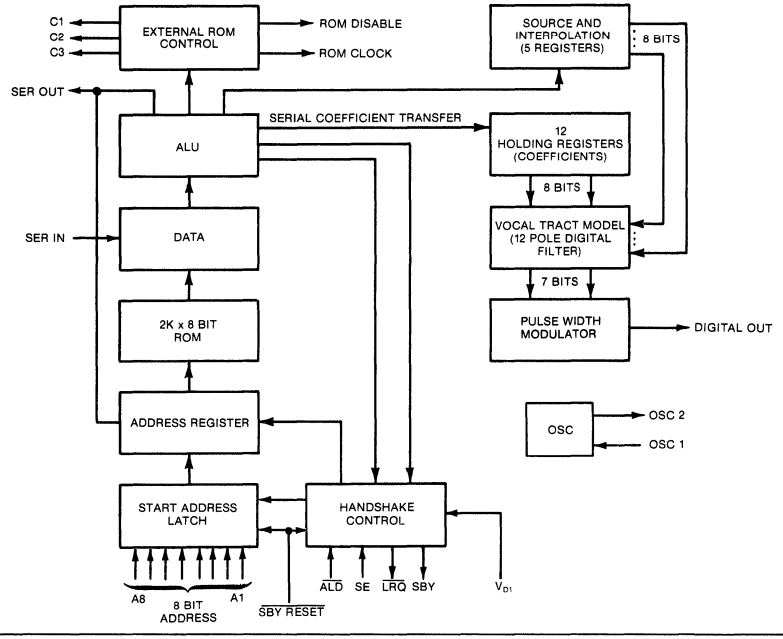
28 LEAD DUAL IN LINE



APPLICATIONS

- Telecommunications
- Appliances
- Computer Peripherals
- Automotive
- Personal Computers
- Toys/Games
- Educational Aids
- Warning Systems
- Security Systems
- Electronic Musical Instruments
- Aids to the Blind
- Narrow Bandwidth
- Communication Systems

SP0256 BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{D1}, V_{DD} ..... −0.3V to +12V
Storage Temperature ..... −25°C to +125°C

Clock

Crystal Frequency 3.12MHz

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.6	—	7	V	
Standby Supply Voltage	V_{D1}	4.6	—	7	V	
Primary Supply Current	I_{DD}	—	—	90	mA	V_{D1}, V_{DD} = 7.0V, T_A = 25°C
Standby Supply Current	I_{D1}	—	—		mA	V_{SS} = 0.0V, T_A = 25°C
Inputs A1-A8, $\overline{ALD}$, SER IN, TEST, SE Logic 0	V_{IL}	0	—	0.6	V	
Logic 1	V_{IH}	2.4	—	V_{D1}	V	
Capacitance	C_{IN}	—	—	10	pf	
Leakage	I_{LC}	—	—	±10	μA	
$\overline{RESET}$, $\overline{SBY\ RESET}$ Logic 0	V_{IL1}	0	—	0.6	V	
Logic 1	V_{IH1}	3.6	—	V_{D1}	V	
Oscillator Leakage OSC 1	—	1.0	—	10	μA	No Load, OSC1 = 7.0V
Outputs SBY, DIGITAL OUT, C1, C2, C3, $\overline{LRQ}$, ROM DISABLE, ROM CLOCK, SER OUT Logic 0	V_{OL}	0	—	0.6	V	0.72mA (2 LS TTL Loads)
Logic 1	V_{OH}	3.5	—	V_{D1}	V	−50μA (2 LS TTL Loads)

AC CHARACTERISTICS

Operating Temperature: T_A = 0°C to +70°C

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Clock Frequency	—	—	3 120	—	MHz	Crystal
$\overline{Reset}$, $\overline{SBY\ Reset}$	t_{pw1}	100	—	—	μs	
$\overline{ALD}$ (<800ns)	t_{pw2}	200	—	800	ns	
A1-A8 Set Up	t_{s2}	160	—	—	ns	
A1-A8 Hold	t_{h2}	160	—	—	ns	
$\overline{ALD}$ (≥800ns)	t_{pw3}	800	—	—	ns	
A1-A8 Set Up	t_{s3}	0	—	—	ns	
A1-A8 Hold	t_{h3}	1200	—	—	ns	
$\overline{LRQ}$	t_{pd0}	—	—	640	ns	
SBY	t_{pd0}	—	—	640	ns	

AUDIO

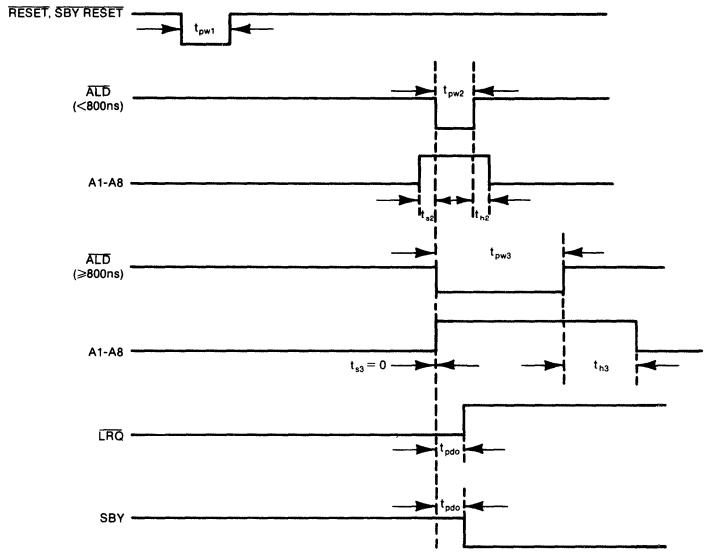


Fig. 1 TIMING DIAGRAM

PIN FUNCTIONS

Pin Number	Name	Function
1	V_{SS}	Ground
2	$\overline{\text{RESET}}$	A logic 0 resets the SP. Must be returned to a logic 1 for normal operation.
3	ROM DISABLE	For use with an external serial speech ROM. A logic 1 disables the external ROM.
4,5,6	C1,C2,C3	Output control lines used by an external serial speech ROM.
7	V_{DD}	Primary power supply.
8	SBY	STANDBY. A logic 1 output indicates that the SP is inactive (i.e., not talking) and V_{DD} can be powered down externally to conserve power. When the SP is reactivated by an address being loaded, SBY will go to a logic 0
9	$\overline{\text{LRQ}}$	$\overline{\text{LOAD REQUEST}}$. $\overline{\text{LRQ}}$ is a logic 1 output whenever the input buffer is full. When $\overline{\text{LRQ}}$ goes to a logic 0, the input port is loaded by placing the 8 address bits on A1-A8 and pulsing the $\overline{\text{ALD}}$ input.
10,11,13,14, 15,16,17,18	A8,A7,A6,A5, A4,A3,A2,A1	8-bit address which defines any one of 256 speech entry points.
12	SER OUT	SERIAL ADDRESS OUT. This output transfers a 16-bit address serially to an external speech ROM.
19	SE	STROBE ENABLE. Normally held in a logic 1 state. When tied to ground, ALD is disabled and the SP will automatically latch in the address on the input bus approximately 1μs after detecting a logic 1 on any address line.
20	$\overline{\text{ALD}}$	$\overline{\text{ADDRESS LOAD}}$. A negative pulse on this input loads the 8 address bits into the input port. The leading edge of this pulse causes $\overline{\text{LRQ}}$ to go high.
21	SER IN	SERIAL IN. This is an 8-bit serial data input from an external speech ROM.
22	TEST	A logic 1 places the SP in test mode. This pin should normally be grounded.
23	V_{D1}	Standby power supply for the interface logic and controller.
24	DIGITAL OUT	Pulse width modulated digital speech output which, when filtered by a 5kHz low pass filter and amplified, will drive a loudspeaker.
25	$\overline{\text{SBY RESET}}$	$\overline{\text{STANDBY RESET}}$. A logic 0 resets the interface logic. Normally should be a logic 1.
26	ROM CLOCK	1.56MHz clock for an external serial speech ROM.
27	OSC 1	XTAL IN. Input connection for a 3.12MHz crystal.
28	OSC 2	XTAL OUT. Output connection for a 3.12MHz crystal.

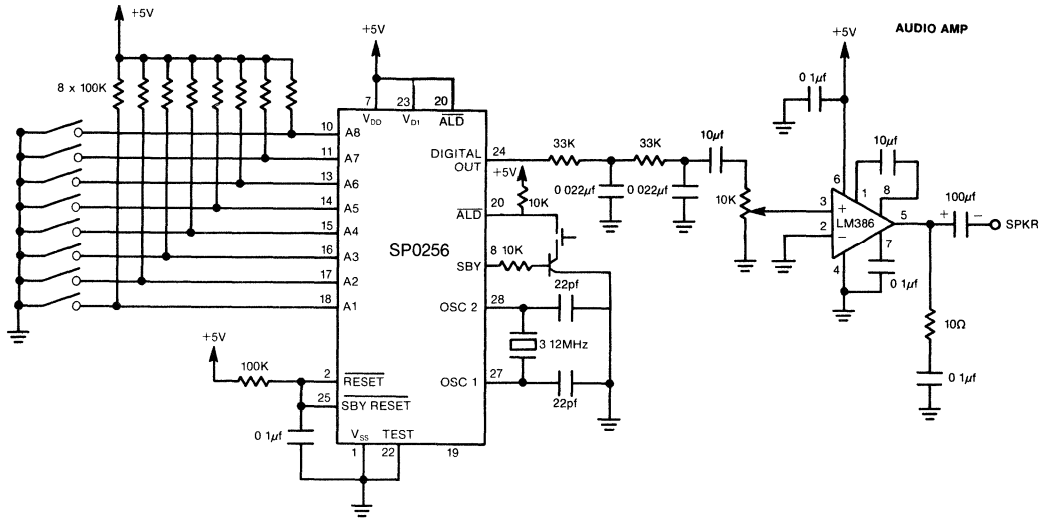


Fig. 2 TYPICAL APPLICATION STAND ALONE CONFIGURATION

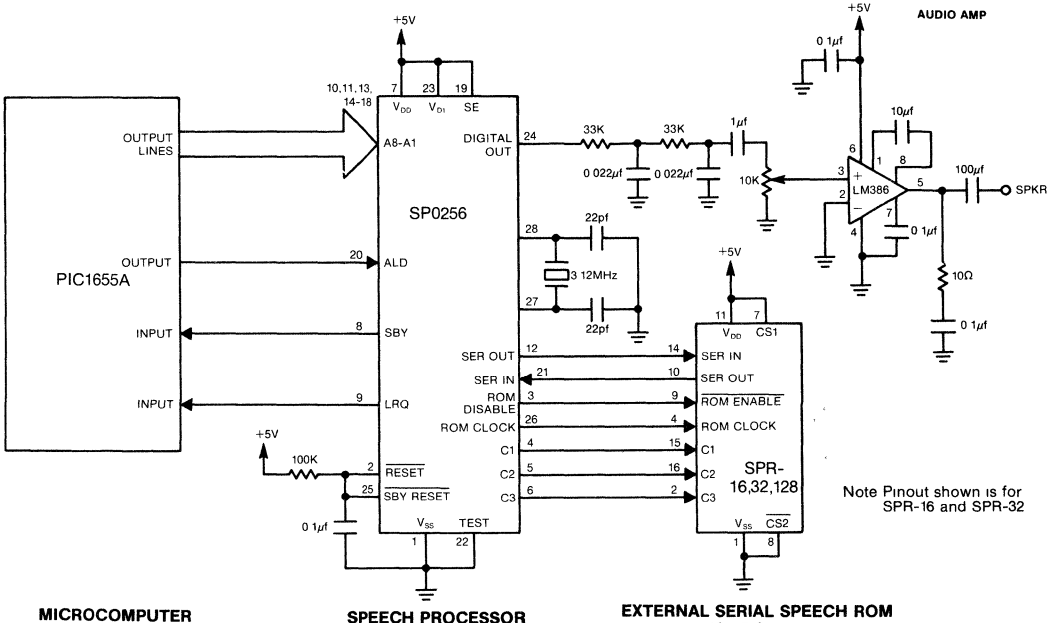


Fig. 3 TYPICAL APPLICATION MICROCOMPUTER INTERFACE

AUDIO

GENERAL INSTRUMENT

SP0256-AL2

Allophone Based Speech Processor

DESCRIPTION

This product is the SP0256 Speech Processor preprogrammed with a standard ROM Pattern containing 64 allophones. Through the concatenation of selected allophones the user can construct any word in the English language, thereby providing an unlimited vocabulary at a data rate of less than 100 bits/second.

DATA MANUAL

A complete description of the SP0256-AL2 is contained in the Allophone Speech Synthesis Manual.

GENERAL INSTRUMENT

†SP0232

32K Speech Processor

DESCRIPTION

This product is pin for pin compatible with the SP0256 Speech Processor. This enhanced version of the SP0256 contains 32K of internal ROM

†For future release.

GENERAL INSTRUMENT

SPR000

Speech Interface Chip

DESCRIPTION

The SPR000 is designed to interface a standard ROM, PROM, or EPROM to the SP0256 Speech Processor to provide a large amount of vocabulary expansion. This interface contains all the logic necessary to allow data communication under control of the Speech Processor. Two chip selects are provided, (CS1 and CS2), for use in systems where it is desirable to bank blocks of memory under external control With the capability of addressing 64K bytes of memory the SPR000 is ideal for applications such as SP0256 testing, and speech ROM emulation.

Voice Synthesis Module

FEATURES

- Complete Speech System
- Stores Approximately 16 Seconds of Speech
- Custom Vocabularies Available
- Simple Digital Interface (TTL)
- 5 Volt Power Supply (±5%)
- Audio Output: 200mw
- Operating Temperature 0° to 55°C
- Dimensions: 3.25" x 5.0"

DESCRIPTION

The VSM2032 utilizes latest state-of-the-art technology to synthesize speech. The module contains three MOS/LSI devices fabricated with N-Channel Ion Implant Processing resulting in a high performance product with proven reliability and production history.

The module can be easily interfaced to any digital system; eight TTL compatible signals are used to select the spoken phrase. Once selected, the VSM2032 requires no support from the user's circuit. It enunciates the phrase and signals when complete.

INTERFACE

The VSM2032 is interfaced using a 15-pin card edge connector (Amphenol 225-21521-401 (117) or equivalent). The phrase to be spoken is selected with a 7-bit address (S_0-S_6). This data is strobed into the module using $\overline{\text{STROBE}}$. The module will drive the busy line ($\overline{\text{BUSY}}$) low while it is speaking. During this time, new data will not be accepted.

The module is initialized by applying two low pulses to the $\overline{\text{RESET}}$ pin.

The audio output is available on both the card edge connector and on the module. It is designed to drive an 8Ω load with 200 mw of power.

VOCABULARY

The standard VSM2032 can enunciate the thirty-two words and syllables listed below. Alternate vocabularies are available (contact regional sales office for information).

Numbers less than one billion can be enunciated using this phrase set. For example, 1214.1 would be generated by concatenating the following phrases:

ONE		THOUSAND		TWO		HUNDRED		FOUR		TEEN		POINT		ONE
1_8		16_8		2_8		15_8		4_8		24_8		32_8		1_8

Addresses 40_8-177_8 are not used with this phrase set. The VSM2032 will lock up if invalid addresses are used.

DATA MANUAL

Complete detailed instructions and description are contained in the VSM2032 application manual.

	ADDRESS							
Octal	S_6	S_5	S_4	S_3	S_2	S_1	S_0	Phrase
0	0	0	0	0	0	0	0	ZERO
1	0	0	0	0	0	0	1	ONE
2	0	0	0	0	0	1	0	TWO
3	0	0	0	0	0	1	1	THREE
4	0	0	0	0	1	0	0	FOUR
5	0	0	0	0	1	0	1	FIVE
6	0	0	0	0	1	1	0	SIX
7	0	0	0	0	1	1	1	SEVEN
10	0	0	0	1	0	0	0	EIGHT
11	0	0	0	1	0	0	1	NINE
12	0	0	0	1	0	1	0	TEN
13	0	0	0	1	0	1	1	ELEVEN
14	0	0	0	1	1	0	0	TWELVE
15	0	0	0	1	1	0	1	HUNDRED
16	0	0	0	1	1	1	0	THOUSAND
17	0	0	0	1	1	1	1	MILLION

	ADDRESS							
Octal	S_6	S_5	S_4	S_3	S_2	S_1	S_0	Phrase
20	0	0	1	0	0	0	0	TWEN
21	0	0	1	0	0	0	1	THIR
22	0	0	1	0	0	1	0	FIF
23	0	0	1	0	0	1	1	TY
24	0	0	1	0	1	0	0	TEEN
25	0	0	1	0	1	0	1	PLUS
26	0	0	1	0	1	1	0	MINUS
27	0	0	1	0	1	1	1	TIMES
30	0	0	1	1	0	0	0	OVER
31	0	0	1	1	0	0	1	EQUALS
32	0	0	1	1	0	1	0	POINT
33	0	0	1	1	0	1	1	ERROR
34	0	0	1	1	1	0	0	IT IS
35	0	0	1	1	1	0	1	AM
36	0	0	1	1	1	1	0	PM
37	0	0	1	1	1	1	1	OH

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 100°C
Storage Temperature ..... −55° to +100°C
Voltage on any Pin with Respect to GND ..... −0.3V to +12.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):
Operating Temperature $T_A = 0°C$ to $+55°C$

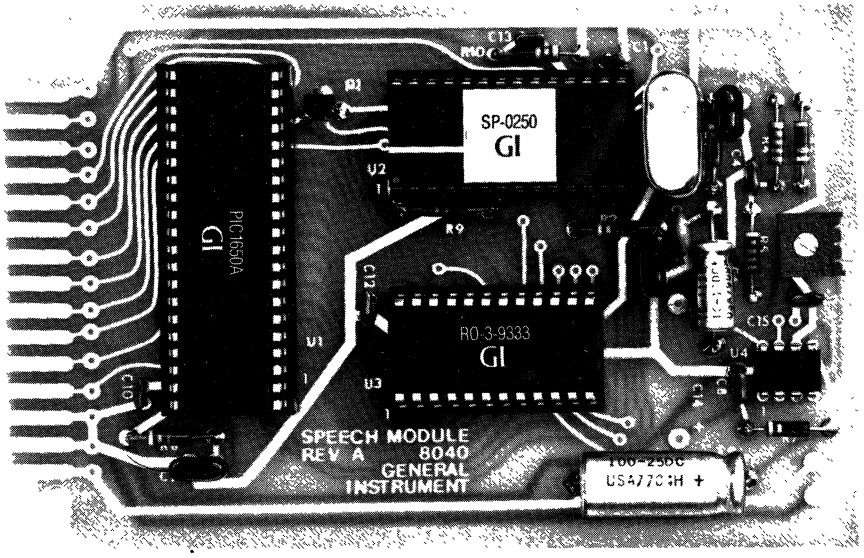
DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage	V_p	4.75	—	5.25	V	
Supply Current	I_p	—	190	280	mA	Audio Off
S_0-S_6 Low Voltage	V_{IL1}	−0.2	—	0.8	V	
S_0-S_6 High Voltage	V_{IH1}	2.4	—	V_p	V	
$\overline{RESET}$ & $\overline{STROBE}$ Low Voltage	V_{IL2}	−0.2	—	0.8	V	
$\overline{RESET}$ & $\overline{STROBE}$ High Voltage	V_{IH2}	V_{p-1}	—	V_p	V	
$\overline{BUSY}$ Output Low Voltage	V_{OL}	—	—	0.8	V	$I_{OL} = 1.6mA$ (NOTE 1)
$\overline{BUSY}$ Output High Voltage	V_{OH}	2.4	—	V_p	V	$I_{OH} = -100\mu A$
Input Low Current	I_{IL}	−0.2	−0.6	−1.6	mA	
Input High Current	I_{IH}	−0.1	−0.4	—	mA	$V_{IH} = 2.4V$
Audio Output	A_p	—	—	200	mW	8Ω LOAD

NOTE:
1. Positive current indicates current into module. Negative current indicates current out of module.

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
$\overline{RESET}$ Low Time	t_{RL}	5	—	—	μs	Two resets are required
$\overline{RESET}$ High Time	t_{RH}	200	—	500	μs	
Data Hold Time	t_{DH}	50	—	—	μs	
Data Setup Time	t_{DS}	0	—	—	ns	
$\overline{BUSY}$ Response Time High	t_{BRH}	—	—	40	μs	
$\overline{STROBE}$ Setup Time	t_{SS}	0	—	—	ns	
$\overline{STROBE}$ Low Time	t_{SL}	5	—	—	μs	
$\overline{BUSY}$ Response Time Low	t_{BRL}	—	—	—	—	Determined by Length of Phrase



AUDIO

Speech Synthesizer

FEATURES

- High Quality Speech Synthesizer/Programmable Digital Filter
- Single +5 Volt Supply
- Simple Interface to a Microcomputer or Microprocessor Based System
- TTL Compatible 8 Bit Bus Interface
- Handshaking
- Double Buffered Input
- On Chip Pulse Width Modulator

DESCRIPTION

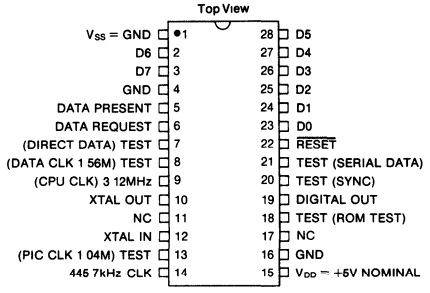
The SP0250 speech synthesizer is an N-channel MOS LSI device capable of generating high quality speech with the natural inflection and emphasis of the original speaker. Operation requires one or more ROMs to store speech data and a microcomputer/processor such as the General Instrument PIC1650A.

The microcomputer fetches a data block from the ROM, formats it into a 15 x 8 bit speech data frame and transfers it to the SP0250 8-bit port using two handshaking signals. This speech data frame, which includes such information as pitch period, amplitude, voiced/unvoiced, number of repetitions and filter coefficients "programs" the synthesizer to produce one frame of speech output.

The achievable output has a frequency response of 100Hz to 5kHz, a dynamic range of 42dB and a signal to noise ratio of approximately 35dB.

PIN CONFIGURATION

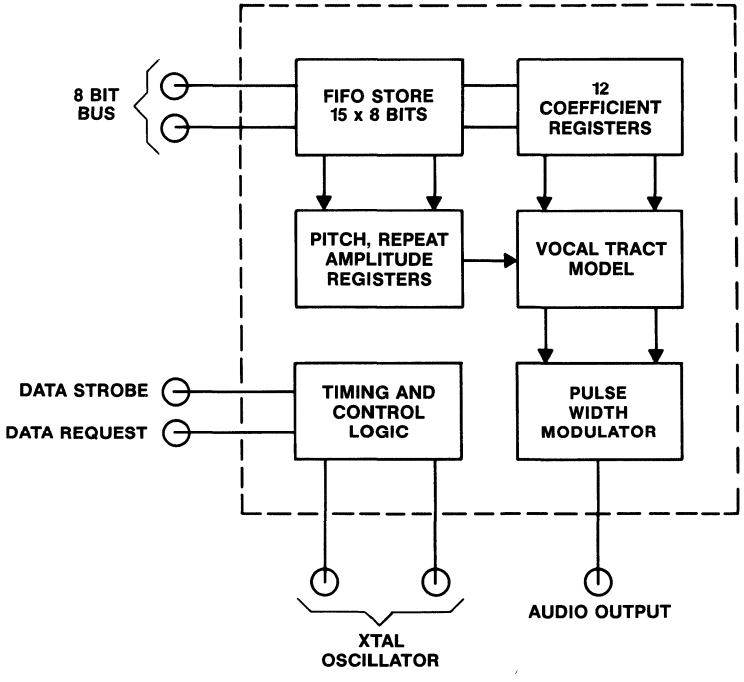
28 LEAD DUAL IN LINE



The SP0250 is controlled by 15 programmable eight bit parameter registers which hold the following information: voiced/unvoiced, pitch period, repeat count, amplitude and 12 digital filter coefficients.

Bit six of the repeat register is used to select either voiced or unvoiced source operation. If voiced mode is selected, the pitch

BLOCK DIAGRAM OF SP0250



AUDIO

period register determines the spacing between the scaled unit impulses applied to the digital filter. The repeat register indicates the number of full pitch periods which will be synthesized before the 15 parameter registers are updated. The amplitude register in both voiced and unvoiced mode controls the gain of the source.

Data request and Data present are the handshaking signals used by the SP0250 and the microcomputer to transfer speech data. The SP0250 drives the Data Request line high when it is ready to accept a 15 x 8 speech frame (Data Request stays high until the entire frame has been input). When the microcomputer sees a logic 1 on Data Request, it will begin to send speech data. The microcomputer outputs 8 bits to the SP0250 followed by a Data Present pulse. This procedure is repeated until the entire 15 byte frame has been transferred.

PIN FUNCTIONS

Pin Number	Name	Function
15	V_{DD}	Positive Power Supply
1	V_{SS}	Ground
Clock		
12	XTAL IN	3.12MHz crystal and associated circuitry are connected here.
10	XTAL OUT	
Inputs		
22	$\overline{\text{Reset}}$	Two high to low transitions on this input resets the chip.
23-28, 2, 3	D0-D7 Data Bus	Input 8 bit data bus.
5	Data Present	Input strobe for 8 bit data bus.
4, 16, 7, 18		Must be grounded for proper chip operation.
Outputs		
6	Data Request	This output requests data be sent to the chip.
19	Digital Out	Chip output. Open collector, requires a pull-up.
9	3.120MHz CPU Clock	Buffered push-pull output.
14	0.4457MHz GROM Clock	Buffered push-pull output with a 3:4 high to low ratio.

TEST PINS

Pin Number	Name	Function
Test Inputs		
7	Direct Data Mode	A logic 1 on this input causes the data bus to be loaded directly into the source register in the chip.
18	ROM Test	A logic 1 on this input causes the ROM outputs to appear on the SERIAL DATA Pin.
Test Outputs		
20	SYNC	Buffered push-pull test output. 640ns positive pulse with 312 clock duty cycle.
21	Serial Data	Buffered push-pull test output. Monitors the internal data bus.
8	1.56MHz Data Clock	Buffered push-pull square wave output.
13	1.04MHz PIC Clock	Buffered push-pull output. 3:4 high to low ratio.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} ..... −0.3V to +12V
Storage Temperature ..... −25°C to +125°C
Lead Temp (Soldering) ..... 10Sec @ +330°C

Standard Conditions (unless otherwise stated)
V_{CC} = +4.6V to +5.5V
Operating Temperature = 0°C to +55°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

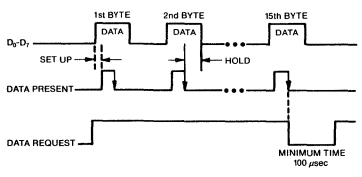
Data labeled "typical" is presented for design guidance only and is not guaranteed.

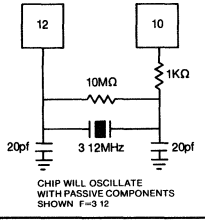
DC CHARACTERISTICS

Characteristic	Min	Typ	Max	Units	Conditions
10 Inputs:					
Reset D0-D7, Data Present					
Logic 0	0	—	0.6	V	
Logic 1	2.4	—	V_{CC}	V	
Leakage	—	—	10	μA	5.5V
1 Clock Input:					
Logic 0	0	—	0.6	V	
Logic 1	4	—	V_{CC}	V	
Leakage	—	—	10	μA	5.5V
2 Test Inputs					
Direct Data Mode, ROM Test					
Logic 0	0	—	0.6	V	
Logic 1	2.4	—	V_{CC}	V	
Capacitance	—	—	10	pf	
Leakage	—	—	10	μA	5.5V
3 P/P Outputs					
Data Request, CPU Clock, GROM Clock					
Logic 0	0	—	0.6	V	.72mA
Logic 1	3.5	—	V_{CC}	V	−50μA
1 O/C Output					
Digital Out					
Logic 0	0	—	0.6	V	2.2K
Logic 1	—	—	10	μA	5.0V Source
Power on $V_{DD} = I_{CC}$	—	50	75	mA@ 25°C	V_{DD}=5.5 V_{SS}=0.0 No Loads

AC CHARACTERISTICS

Characteristic	Min	Typ	Max	Units	Conditions
Clock Frequency	—	3.12	—	MHz	Square Wave
Clock Period	—	320	—	ns	
Data Present					
Logic 1	1.5	—	—	μs	
Logic 0	10	—	—	μs	
Reset D0-D7	1000	—	—	μs	
Set Up	1.5	—	—	μs	
Hold	1.5	—	—	μs	
P/P Test Output					
Serial Data					
Logic 0	0	—	0.6	V	
Logic 1	3.5	—	V_{CC}	V	No Load





AUDIO

Speech Field Development Board

FEATURES

- 5 Volts ±5%, Single Supply Operation
- Expandable to 256K Bits of EPROM
- Supports LPC Synthesis, Formant Synthesis, and Allophone Synthesis
- On Board Crystal Oscillator
- Dimensions: 4" x 6.25"
- Cable Length: 14"

DESCRIPTION

The Speech Field Development System is an EPROM based version of the SP0256 Speech Processor and speech ROMs. It is used to demonstrate and test synthetic speech or complex sounds before they are committed to masked ROM. The SFD2000 emulates up to 256K bits of expansion ROM.

The address, DAC output and control signals are made available on a 28 pin header/cable that connects to the board. Power (V_{D1} and V_{DD}) for the module is supplied via a 3 pin connector or can be strapped for internal operation. The voltage input to V_{D1} and V_{DD} lines must be limited to 5 Volts ±5%.

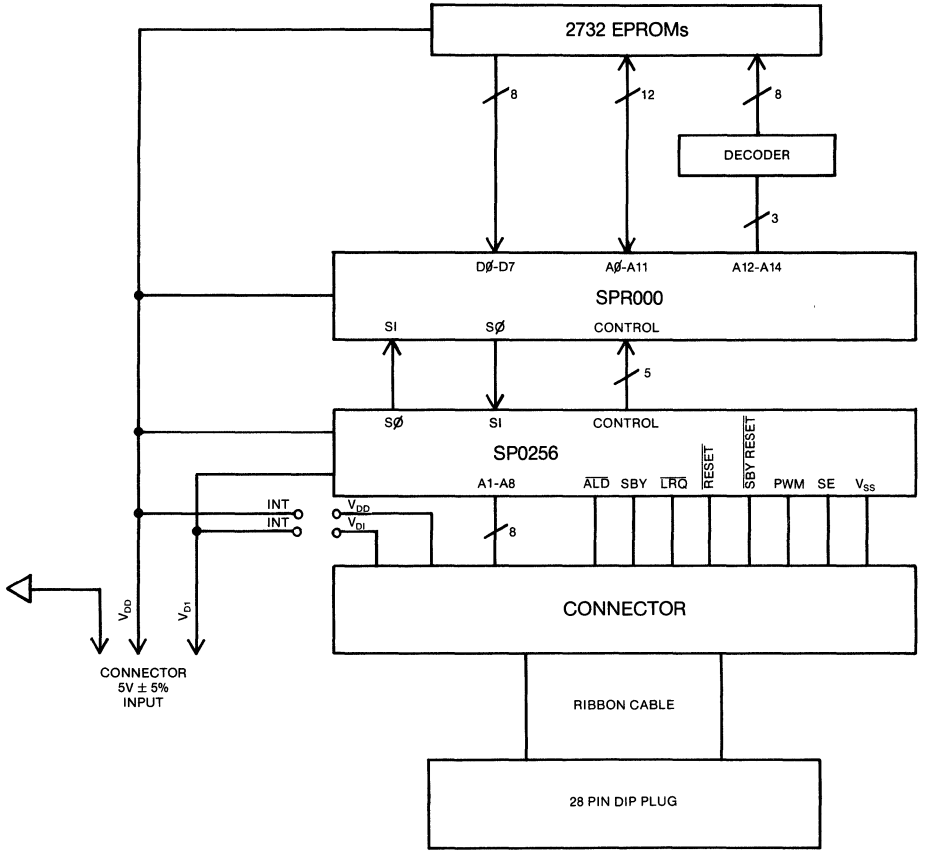
The SP0256 Speech Processor executes the 8 bits of data and modifies the appropriate parameters of the Vocal Tract Model (VTM) to create the desired sound sequence.

The SFD module comes complete with an SP0256, SPR000 and sockets for eight 2732 EPROMs. A cable is provided to interface the SFD2000 to the user's system.

DATA MANUAL

A complete description of the SFD2000 system is contained in the Speech Field Development Data Manual.

SFD2000 BLOCK DIAGRAM



AUDIO

GENERAL INSTRUMENT

Sound Generation

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
PROGRAMMABLE SOUND GENERATOR	Full software control, 5V operation, simple interface, triple analog output, general purpose I/O ports.	AY-3-8910	5-18
		AY-3-8912	5-18
		AY-3-8913	5-18
TUNES SYNTHESIZER	Produces musical tunes from pre-programmed microcomputer.	AY-3-1350	5-26

Programmable Sound Generator

FEATURES

- Full Software Control of Sound Generation
- Interfaces to Most 8-Bit and 16-Bit Microprocessors
- Three Independently Programmed Analog Outputs
- Two 8-Bit General Purpose I/O Ports (AY-3-8910)
- One 8-Bit General Purpose I/O Port (AY-3-8912)
- Single +5 Volt Supply

DESCRIPTION

The AY-3-8910/8912/8913 Programmable Sound Generator (PSG) is a LSI Circuit which can produce a wide variety of complex sounds under software control The AY-3-8910/8912/8913 is manufactured in the General Instrument N-Channel Ion Implant Process Operation requires a single +5V power supply, a TTL compatible clock, and a microprocessor controller such as the General Instrument 16-bit CP1610 or one of the PIC1650 series of 8-bit microcomputers

The PSG is easily interfaced to any bus oriented system Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling and FSK modems The analog sound outputs can each provide 4 bits of logarithmic digital to analog conversion, greatly enhancing the dynamic range of the sounds produced

In order to perform sound effects while allowing the processor to continue its other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable channels available in the PSG

All of the circuit control signals are digital in nature and intended to be provided directly by a microprocessor/microcomputer This means that one PSG can produce the full range of required sounds with no change in external circuitry Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections

Since most applications of a microprocessor/PSG system would also require interfacing between the outside world and the microprocessor, this facility has been designed into the PSG The AY-3-8910 has two general purpose 8-bit I/O ports and is supplied in a 40 lead package the AY-3-8912 has one port and 28 leads the AY-3-8913 has no ports and 24 leads

PIN FUNCTIONS

DA7--DA0 (input/output/high impedance) pins 30--37 (AY-3-8910)
Data/Address 7--0: pins 21--28 (AY-3-8912)
pins 4--11 (AY-3-8913)

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG In the data mode, DA7--DA0 correspond to Register Array bits B7--B0 In the address mode, DA3--DA0 select the register number ($0--17_8$) and a DA7--DA4 in conjunction with address inputs $\overline{A9}$ and A8 for the high order address (chip select)

A8 (input) pin 25 (AY-3-8910)
pin 17 (AY-3-8912)
pin 23 (AY-3-8913)

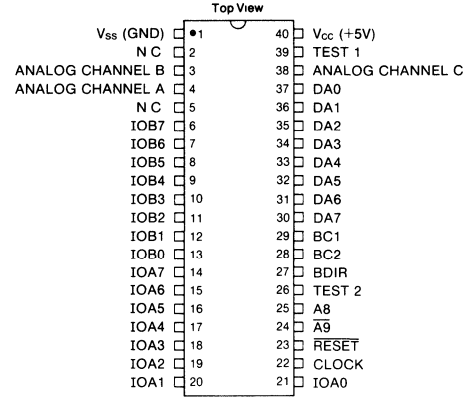
$\overline{\text{A9}}$ (input) pin 24 (AY-3-8910)
pin 22 (AY-3-8913)
(not provided on AY-3-8912)

Address 9, Address 8

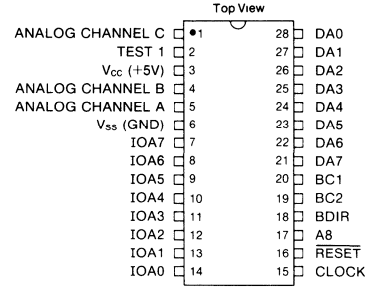
These "extra" address bits are made available to enable the positioning of the PSG (assigning a 16 word memory space) in a total 1,024 word memory area rather than in a 256 word memory area as defined by address bits DA7--DA0 alone If the memory size does not require the use of these extra address lines they may be left unconnected as each is provided with either an on-chip pull down ($\overline{A9}$) or pull-up (A8) resistor In "noisy" environments, however, it is recommended that $\overline{A9}$ and A8 be tied to an external ground and +5V, respectively, if they are not to be used

PIN CONFIGURATIONS

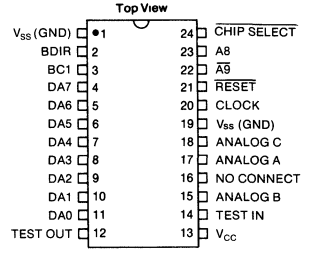
40 LEAD DUAL IN LINE
AY-3-8910



28 LEAD DUAL IN LINE
AY-3-8912



24 LEAD DUAL IN LINE



AUDIO

RESET (input) pin 23 (AY-3-8910) pin 21 (AY-3-8913)
pin 16 (AY-3-8912)

For initialization/power-on purposes, applying a logic "0" (ground) to the Reset pin will reset all registers to "0" The Reset pin is provided with an on-chip pull-up resistor.

CLOCK (input) pin 22 (AY-3-8910) pin 20 (AY-3-8913)
pin 15 (AY-3-8912)

This TTL-compatible input supplies the timing reference for the Tone, Noise and Envelope Generators

BDIR, BC2, BC1 (inputs) pins 27,28,29 (AY-3-8910)
pins 18,19,20 (AY-3-8912) pins 2, 3 (No BC2 on AY-3-8913 see below).

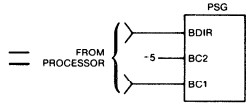
Bus DIRection, Bus Control 2,1

These bus control signals are generated directly by the CP1610 series of microprocessors to control all external and internal bus operations in the PSG When using a processor other than the CP1610, these signals can be provided either by comparable bus signals or by simulating the signals on I/O lines of the processor. The PSG decodes these signals as illustrated in the following

BDIR	BC2	BC1	CP1610 FUNCTION	PSG FUNCTION
0	0	0	NACT	INACTIVE See 010 (IAB).
0	0	1	ADAR	LATCH ADDRESS See 111 (INTAK)
0	1	0	IAB	INACTIVE. The PSG/CPU bus is inactive DA7--DA0 are in a high impedance state
0	1	1	DTB	READ FROM PSG This signal causes the contents of the register which is currently addressed to appear on the PSG/CPU bus DA7--DA0 are in the output mode
1	0	0	BAR	LATCH ADDRESS See 111 (INTAK)'
1	0	1	DW	INACTIVE See 010 (IAB)
1	1	0	DWS	WRITE TO PSG This signal indicates that the bus contains register data which should be latched into the currently addressed register DA7--DA0 are in the input mode
1	1	1	INTAK	LATCH ADDRESS This signal indicates that the bus contains a register address which should be latched in the PSG. DA7--DA0 are in the input mode

While interfacing to a processor other than the CP1610 would simply require simulating the above decoding, the redundancies in the PSG functions vs bus control signals can be used to advantage in that only four of the eight possible decoded bus functions are required by the PSG. This could simplify the programming of the bus control signals to the following, which would only require that the processor generate two bus control signals (BDIR and BC1, with BC2 tied to +5V) This is the case with the AY-3-8913 with BC2 pulled high internally

BDIR	BC2	BC1	PSG FUNCTION
0	1	0	INACTIVE
0	1	1	READ FROM PSG
1	1	0	WRITE TO PSG
1	1	1	LATCH ADDRESS



ANALOG CHANNEL A, B, C (outputs) pins 4, 3, 38 (AY-3-8910)
pins 5, 4, 1 (AY-3-8912) pins 17, 15, 18 (AY-3-8913)

Each of these signals is the output of its corresponding D/A Converter, and provides an up to 1V peak-peak signal representing the complex sound waveshape generated by the PSG.

IOA7--IOA0 (input/output) pins 14--21 (AY-3-8910)
pins 7--14 (AY-3-8912) (not provided on AY-3-8913)

IOB7--IOB0 (input/output) pins 6--13 (AY-3-8910)
(not provided on AY-3-8912) (not provided on AY-3-8913)

Input/Output A7--A0, B7--B0

Each of these two parallel input/output ports provides 8 bits of parallel data to/from the PSG/CPU bus from/to any external devices connected to the IOA or IOB pins Each pin is provided with an on-chip pull-up resistor, so that when in the "input" mode, all pins will read normally high Therefore, the recommended method for scanning external switches would be to ground the input bit.

TEST 1: pin 39 (AY-3-8910) pin 14 (AY-3-8913) pin 2 (AY-3-8912)
TEST 2: pin 26 (AY-3-8910) pin 12 (AY-3-8913)
(not connected on AY-3-8912)

These pins are for General Instrument test purposes only and should be left open—do not use as tie-points.

V_{CC}: pin 40 (AY-3-8910) pin 13 (AY-3-8913) pin 3 (AY-3-8912)
Nominal +5Volt power supply to the PSG

V_{SS}: pin 1 (AY-3-8910) pin 19 (AY-3-8913) pin 6 (AY-3-8912)
Ground reference for the PSG

CHIP SELECT (Input) Pin 24 (AY-3-8913 only)

This input signal goes low to enable the PSG to read data on the data bus or write data from the data bus to one of the internal registers. For these above operations to occur, this signal must be true in addition to the current bus address being a valid PSG address This signal must be valid for all read and write operations The pin has an internal pull down to V_{SS}.

ARCHITECTURE

The AY-3-8910/8912/8913 is a register oriented Programmable Sound Generator (PSG) Communication between the processor and the PSG is based on the concept of memory-mapped I/O Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values.

All functions of the PSG are controlled through the 16 registers which once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks

REGISTER ARRAY

The principal element of the PSG is the array of 16 read/write control registers These 16 registers look to the CPU as a block of memory and as such occupy a 16 word block out of 1,024 possible addresses The 10 address bits (8 bits on the common data/address bus, and 2 separate address bits A8 and $\overline{A9}$) are decoded as follows

* $\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	0	0	0	0

THRU

0	1	0	0	0	0	1	1	1	1

HIGH ORDER (Chip Select) LOW ORDER (Register No.)

* $\overline{A9}$ is not provided on the AY-3-8912

The four low order address bits select one of the 16 registers (R0--$R17_8$). The six high order address bits function as "chip selects" to control the tri-state bidirectional buffers (when the high order address bits are "incorrect", the bidirectional buffers are forced to a high impedance state). High order address bits $\overline{A9}$, A8 are fixed in the PSG design to recognize a 01 code, high order address bits DA7--DA4 may be mask-programmed to any 4-bit code by a special order factory mask modification. Unless otherwise specified, address bits DA7--DA4 are programmed to recognize only a 0000 code. A valid high order address latches the register address (the low order 4 bits) in the Register Address Latch/Decoder block A latched address will remain valid until the receipt of a new address, enabling multiple reads and writes of the same register contents without the need for redundant re-addressing

Conditioning of the Register Address Latch/Decoder and the Bidirectional Buffers to recognize the bus function required (inactive, latch address, write data, or read data) is accomplished by the Bus Control Decode block.

SOUND GENERATING BLOCKS

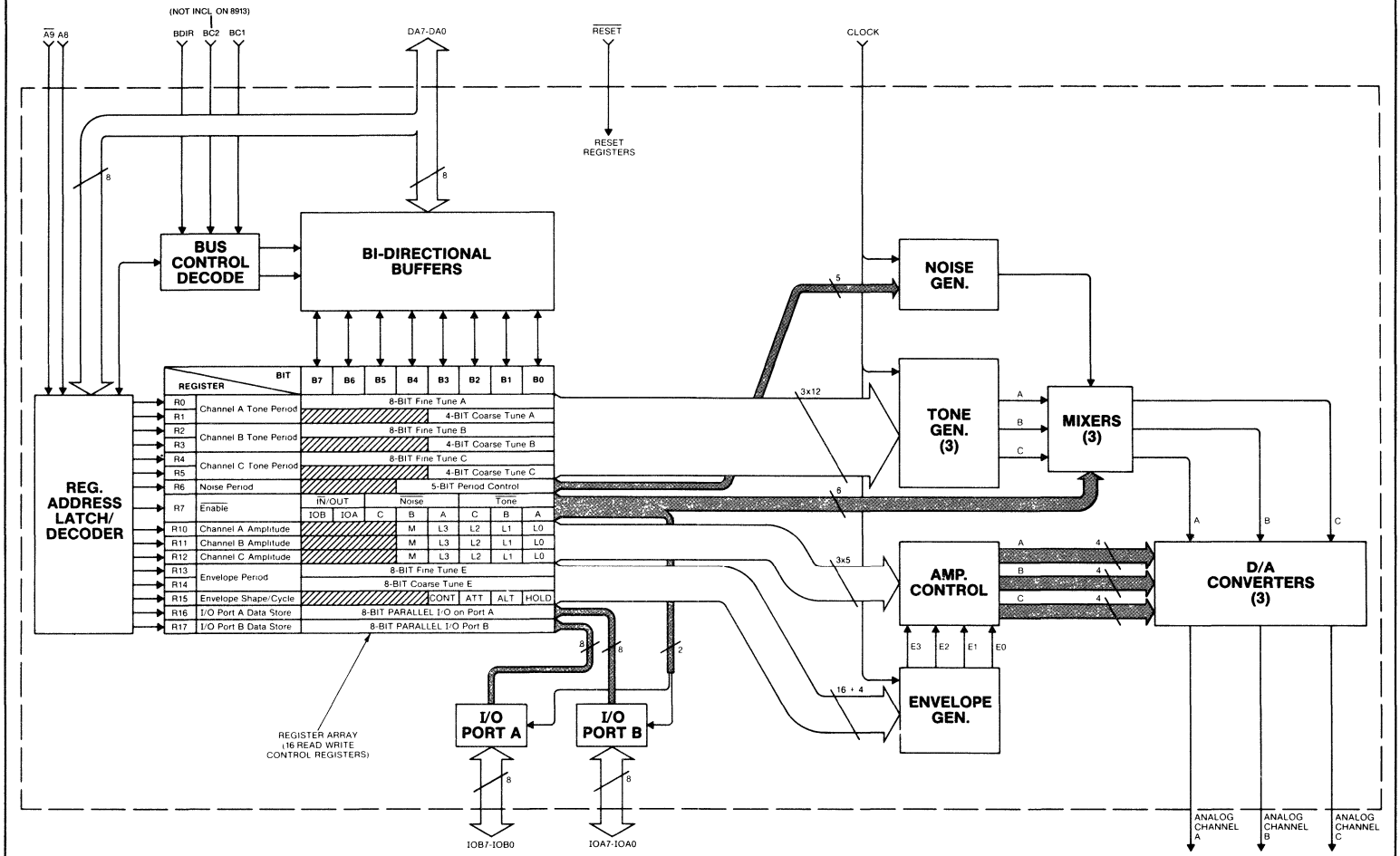
The basic blocks in the PSG which produce the programmed sounds include:

Tone Generators	produce the basic square wave tone frequencies for each channel (A,B,C)
Noise Generator	produces a frequency modulated pseudo random pulse width square wave output
Mixers	combine the outputs of the Tone Generators and the Noise Generator One for each channel (A,B,C)
Amplitude Control	provides the D/A Converters with either a fixed or variable amplitude pattern The fixed amplitude is under direct CPU control; the variable amplitude is accomplished by using the output of the Envelope Generator
Envelope Generator	produces an envelope pattern which can be used to amplitude modulate the output of each Mixer
D/A Converters	the three D/A Converters each produce up to a 16 level output signal as determined by the Amplitude Control

I/O PORTS

Two additional blocks are shown in the PSG Block Diagram which have nothing directly to do with the production of sound—these are the two I/O Ports (A and B) Since virtually all uses of microprocessor-based sound would require interfacing between the outside world and the processor, this facility has been included in the PSG. Data to/from the CPU bus may be read/written to either of two 8-bit I/O Ports without affecting any other function of the PSG. The I/O Ports are TTL-compatible and are provided with internal pull-ups on each pin. Both Ports are available on the AY-3-8910; only I/O Port A is available on the AY-3-8912; no ports are available on the AY-3-8913

AUDIO



PSG BLOCK DIAGRAM

OPERATION

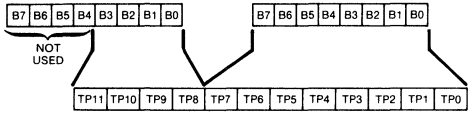
Since all functions of the PSG are controlled by the processor via a series of register loads, a detailed description of the PSG operation can best be accomplished by relating each PSG function to the control of its corresponding register The function of creating or programming a specific sound or sound effect logically follows the control sequence listed:

Operation	Registers	Function
Tone Generator Control	R0--R5	Program tone periods
Noise Generator Control	R6	Program noise period
Mixer Control	R7	Enable tone and/or noise on selected channels
Amplitude Control	R10--R12	Select "fixed" or "envelope-variable" amplitudes
Envelope Generator Control	R13--R15	Program envelope period and select envelope pattern

Tone Generator Control
(Registers R0, R1, R2, R3, R4, R5)

The frequency of each square wave generated by the three Tone Generators (one each for Channels A, B, and C) is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 12-bit Tone Period value. Each 12-bit value is obtained in the PSG by combining the contents of the relative Coarse and Fine Tune registers, as illustrated in the following

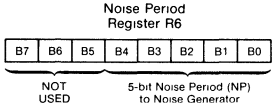
Coarse Tune Register	Channel	Fine Tune Register
R1	A	R0
R3	B	R2
R5	C	R4



12-bit Tone Period (TP) to Tone Generator

Noise Generator Control
(Register R6)

The frequency of the noise source is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 5-bit Noise Period value This 5-bit value consists of the lower 5 bits (B4--B0) of register R6, as illustrated in the following



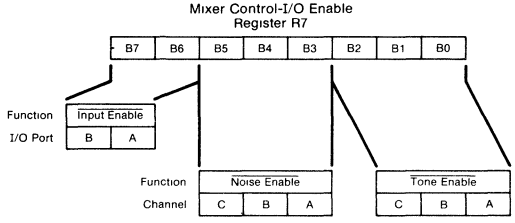
Mixer Control-I/O Enable
(Register R7)

Register R7 is a multi-function Enable register which controls the three Noise/Tone Mixers and the two general purpose I/O Ports

The Mixers as previously described, combine the noise and tone frequencies for each of the three channels The determination of combining neither/either/both noise and tone frequencies on each channel is made by the state of bits B5--B0 of R7

The direction (input or output) of the two general purpose I/O Ports (IOA and IOB) is determined by the state of bits B7 and B6 of R7

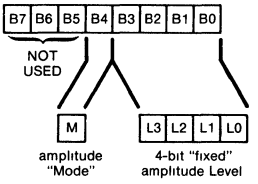
These functions are illustrated in the following



Amplitude Control
(Registers R10, R11, R12)

The amplitudes of the signals generated by each of the three D/A Converters (one each for Channels A, B, and C) is determined by the contents of the lower 5 bits (B4--B0) of registers R10, R11, and R12 as illustrated in the following

Amplitude Control Register	Channel
R10	A
R11	B
R12	C

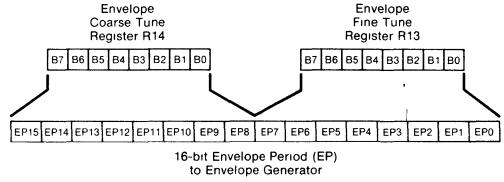


Envelope Generator Control
(Registers R13, R14, R15)

To accomplish the generation of fairly complex envelope patterns, two independent methods of control are provided in the PSG first, it is possible to vary the frequency of the envelope using registers R13 and R14; and second, the relative shape and cycle pattern of the envelope can be varied using register R15 The following paragraphs explain the details of the envelope control functions, describing first the envelope period control and then the envelope shape/cycle control

ENVELOPE PERIOD CONTROL (Registers R13, R14)

The frequency of the envelope is obtained in the PSG by first counting down the input clock by 256, then by further counting down the result by the programmed 16-bit Envelope Period value. This 16-bit value is obtained in the PSG by combining the contents of the Envelope Coarse and Fine Tune registers, as illustrated in the following

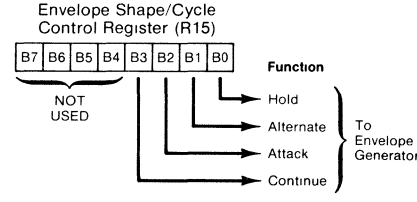


16-bit Envelope Period (EP) to Envelope Generator

ENVELOPE SHAPE/CYCLE CONTROL (Register R15)

The Envelope Generator further counts down the envelope frequency by 16, producing a 16-state per cycle envelope pattern as defined by its 4-bit counter output, E3 E2 E1 E0 The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern (count up/count down) of the 4-bit counter and by defining a single-cycle or repeat-cycle pattern

This envelope shape/cycle control is contained in the lower 4 bits (B3--B0) of register R15 Each of these 4 bits controls a function in the envelope generator, as illustrated in the following



AUDIO

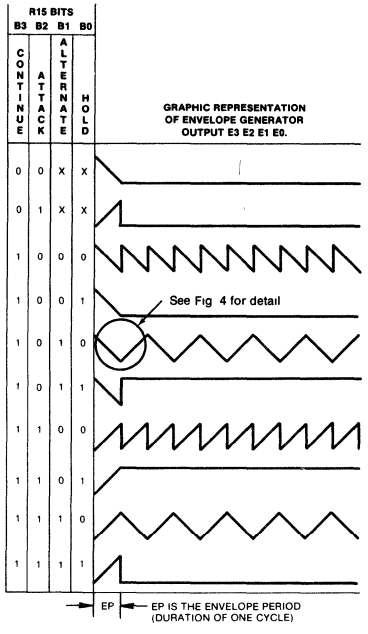


Fig. 1 ENVELOPE SHAPE/CYCLE OPERATION

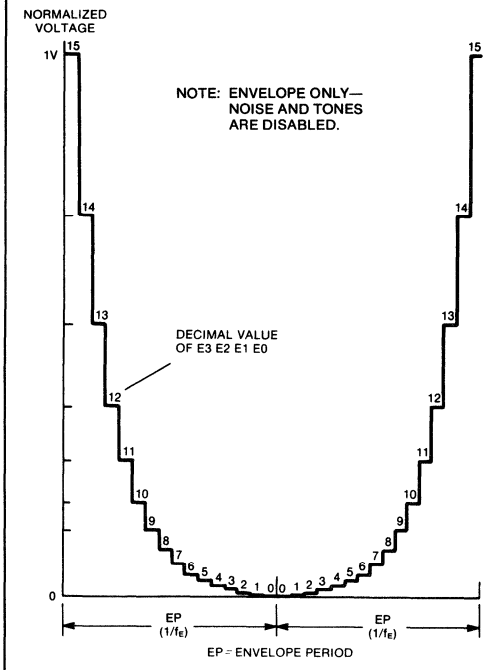


Fig. 3 D/A CONVERTER OUTPUT

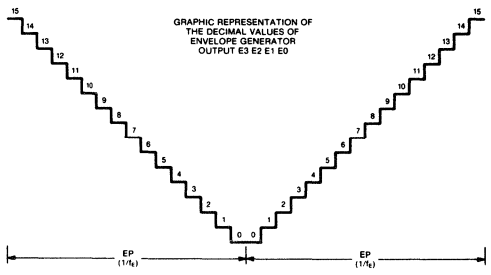


Fig. 2 DETAIL OF TWO CYCLES OF Fig. 1 (ref. waveform "1010" in Fig. 1)

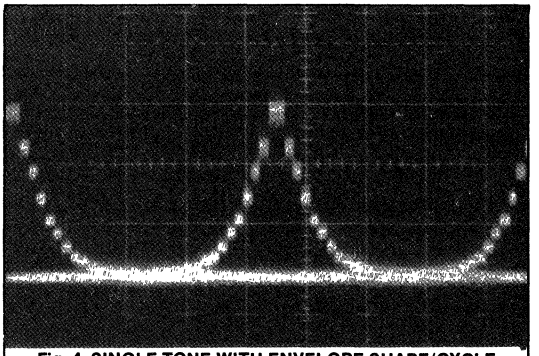


Fig. 4 SINGLE TONE WITH ENVELOPE SHAPE/CYCLE PATTERN 1010

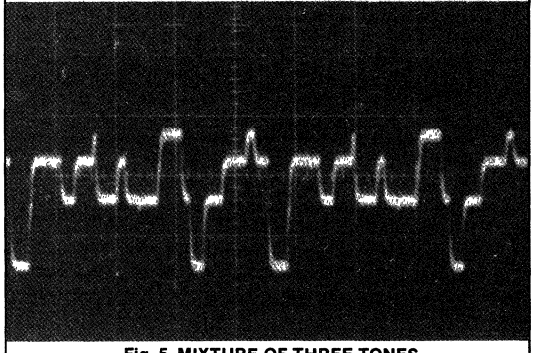


Fig. 5 MIXTURE OF THREE TONES WITH FIXED AMPLITUDES

AUDIO

I/O Port Data Store (Registers R16, R17)

Registers R16 and R17 function as intermediate data storage registers between the PSG/CPU data bus (DA0--DA7) and the two I/O ports (IOA7--IOA0 and IOB7--IOB0) Both ports are available in the AY-3-8910, only I/O Port A is available in the AY-3-8912 none are available on the AY-3-8913 Using registers R16 and R17 for the transfer of I/O data has no effect on sound generation

D/A Converter Operation

Since the primary use of the PSG is to produce sound for the highly imperfect amplitude detection mechanism of the human ear, the D/A conversion is performed in logarithmic steps with a normalized voltage range of from 0 to 1 Volt. The specific amplitude control of each of the three D/A Converters is accomplished by the three sets of 4-bit outputs of the Amplitude Control block, while the Mixer outputs provide the base signal frequency (Noise and/or Tone).

ELECTRICAL CHARACTERISTICS (AY-3-8910, AY-3-8912)

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +40°C
V_{CC} and all other Input/Output
Voltages with Respect to V_{SS} ..... −0.3V to +8.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{CC} = +5V ±5%
V_{SS} = GND
Operating Temperature = 0°C to +40°C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
All Inputs						
Low Level	V_{IL}	0	—	0.6	V	
High Level	V_{IH}	2.4	—	V_{CC}	V	
All Outputs (except Analog Channel Outputs)						
Low Level	V_{OL}	0	—	0.5	V	I_{OL} = 1.6mA, 20pf
High Level	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 100μA, 20pf
Analog Channel Outputs	V_O	0	—	60	dB	Test Circuit: Fig. 6
Power Supply Current	I_{CC}	—	45	85	mA	
AC CHARACTERISTICS						
Clock Input						
Frequency	f_C	1	—	2	MHz	Fig. 7
Rise Time	t_r	—	—	50	ns	
Fall Time	t_f	—	—	50	ns	
Duty Cycle	—	25	50	85	%	
Bus Signals (BDIR, BC2, BC1)						
Associative Delay Time	t_{BD}	—	—	50	ns	
Reset						
Reset Pulse Width	t_{RW}	500	—	—	ns	Fig. 8
Reset to Bus Control Delay Time	t_{RB}	100	—	—	ns	
A9, A8, DA7--DA0 (Address Mode)						
Address Setup Time	t_{AS}	400	—	—	ns	Fig. 9
Address Hold Time	t_{AH}	100	—	—	ns	
DA7--DA0 (Write Mode)						
Write Data Pulse Width	t_{DW}	500	—	10,000	ns	Fig. 10
Write Data Setup Time	t_{DS}	50	—	—	ns	
Write Data Hold Time	t_{DH}	100	—	—	ns	
DA7--DA0 (Read Mode)						
Read Data Access Time	t_{DA}	—	250	500	ns	Fig. 11
DA7--DA0 (Inactive Mode)						
Tristate Delay Time	t_{TS}	—	100	200	ns	

**Typical values are at +25°C and nominal voltages.

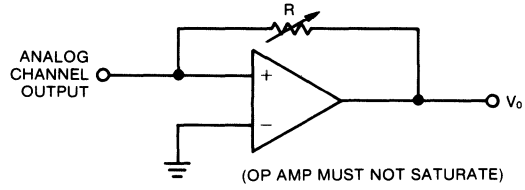


Fig. 6 ANALOG CHANNEL OUTPUT TEST CIRCUIT

AUDIO

ELECTRICAL CHARACTERISTICS (AY-3-8913)

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +70°C
V_{CC} and all other Input/Output Voltages with Respect to V_{SS} ..... −0.3V to +8.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{CC} = +5V ±5%
V_{SS} = GND
Operating Temperature = 0°C to +70°C

Characteristics	Sym	Min	Max	Units	Conditions
DC CHARACTERISTICS					
Input Voltage Levels					
Low Level	V_{IL}	0	0.7	V	
High Level	V_{IH}	2.2	V_{CC}	V	
Output Voltage Levels (except Analog Channel Outputs)					
Low Level	V_{OL}	0	0.4	V	1 TTL Load
High Level	V_{OH}	2.4	V_{CC}	V	+100pf
Analog Channel Outputs	V_O	0	2000	μA	Test Circuit: Fig. 6
Power Supply Current	I_{CC}	—	85	mA	
AC CHARACTERISTICS					
Clock Input					
Frequency	f_c	1	2.5	MHz	Fig. 7
Rise Time	t_r	—	50	ns	
Fall Time	t_f	—	50	ns	
Duty Cycle	—	40	60	%	
Bus Signals (BDIR, BC2, BC1)					
Associative Delay Time	t_{BD}	—	50	ns	
Reset					
Reset Pulse Width	t_{RW}	5	—	μs	Fig. 8
Reset to Bus Control Delay Time	t_{RB}	100	—	ns	
A9, A8, DA7--DA0 (Address Mode)					
Address Setup Time	t_{AS}	300	—	ns	Fig. 9
Address Hold Time	t_{AH}	50	—	ns	
DA7--DA0 (Write Mode)					
Write Data Pulse Width	t_{DW}	1800	—	ns	Fig. 10
Write Data Setup Time	t_{DS}	50	—	ns	
Write Data Hold Time	t_{DH}	100	—	ns	
DA7--DA0 (Read Mode)					
Read Data Access Time	t_{DA}	—	350	ns	Fig. 11
DA7--DA0 (Inactive Mode)					
Tristate Delay Time	t_{TS}	—	400	ns	

TIMING DIAGRAMS

Fig. 7 CLOCK AND BUS SIGNAL TIMING

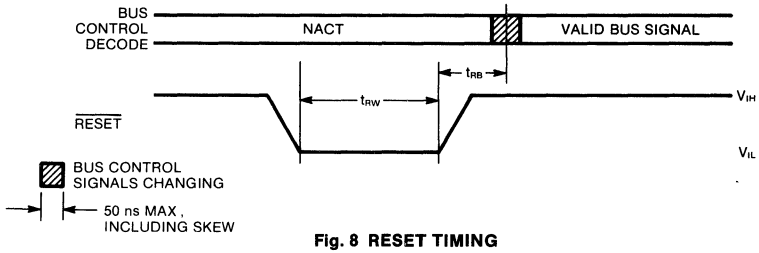
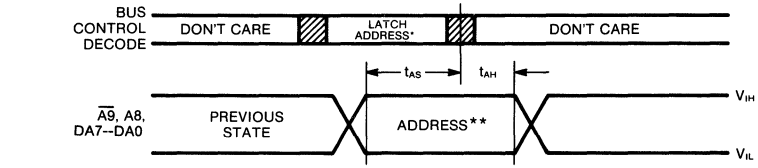


Fig. 8 RESET TIMING

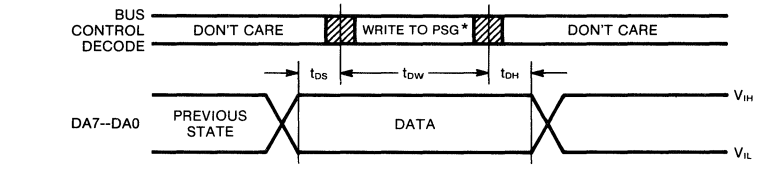


**REFER TO PARAGRAPH 2 1 1 FOR A DESCRIPTION OF "VALID" PSG ADDRESSING

*ANY COMBINATION OF BDIR, BC2, BC1 WHICH DECODE "LATCH ADDRESS"

	BDIR	BC2	BC1
	0	0	1
or	1	0	0
or	1	1	1

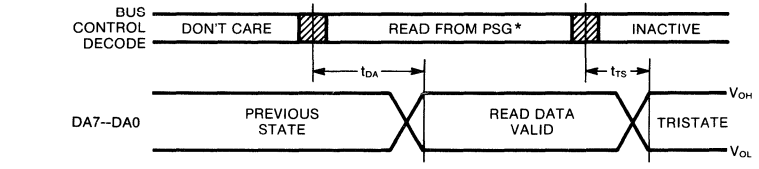
Fig. 9 LATCH ADDRESS TIMING



*"WRITE TO PSG"

BDIR	BC2	BC1
1	1	0

Fig. 10 WRITE DATA TIMING



*"READ FROM PSG"

BDIR	BC2	BC1
0	1	1

Fig. 11 READ DATA TIMING

AUDIO

GENERAL INSTRUMENT

AY-3-1350

Tunes Synthesizer

FEATURES

- 25 Different Tunes Plus 3 Chimes
- Mask Programmable with Customer Specified Tunes for Toys, Musical Boxes, etc.
- Minimal External Components
- Automatic Switch-Off Signal at End of Tune for Power Savings
- Envelope Control to Give Organ or Piano Quality
- Sequential Tune Mode
- 4 Door Capability When Used as Doorchime
- Operation with Tunes in External PROM if Required
- Single Supply (+5V) Operation

DESCRIPTION

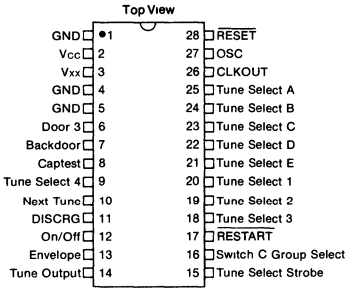
The AY-3-1350 is an N-Channel MOS microcomputer based synthesizer of pre-programmed tunes for applications in toys, musical boxes, and doorchimes. The standard device has a set of 25 different popular and classical tunes chosen for their international acceptance. In addition there are 3 chimes making a total of 28 tunes.

The chip is mask-programmable during manufacture enabling the quantity user to select his own music. Up to 28 tunes of varying length can be chosen.

The device has multi-mode operation making it suitable for a wide variety of applications.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



TUNES

The standard AY-3-1350 contains the following tunes:

A0 Toreador
B0 William Tell
C0 Hallelujah Chorus
D0 Star Spangled Banner
E0 Yankee Doodle

A1 John Brown's Body
B1 Clementine
C1 God Save the Queen
D1 Colonel Bogey
E1 Marseillaise

A2 America, America
B2 Deutschland Leid
C2 Wedding March
D2 Beethoven's 5th
E2 Augustine

A3 O Sole Mio
B3 Santa Lucia
C3 The End
D3 Blue Danube
E3 Brahms' Lullaby

A4 Hell's Bells
B4 Jingle Bells
C4 La Vie en Rose
D4 Star Wars
E4 Beethoven's 9th

Chime X Westminster Chime
Chime Y Simple Chime
Chime Z Descending Octave Chime

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Voltage on any pin with respect to ground (V_{SS}) ..... −0.3V to +10.0V

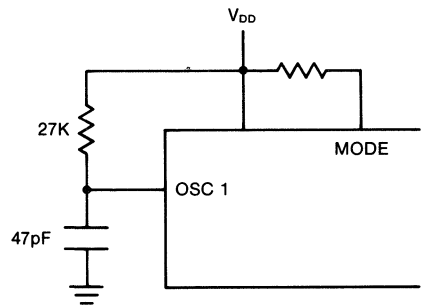
Standard Conditions (unless otherwise noted)
Operating Temperature (T_A) = 0°C to +70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics	Sym	Min	Max	Units	Conditions
DC CHARACTERISTICS					
Primary Supply Voltage	V_{DD}	4.5	7	V	
Output Buffer Supply Voltage	V_{XX}	4.5	9	V	
Primary Supply Current	I_{DD}	—	55	mA	No load
Output Buffer Supply Current	I_{XX}	—	5	mA	No load
Logic Input Low Voltage	V_{IL}	−0.2	0.8	V	
Logic Input High Voltage (Note 2) (Except $\overline{RESET}$ and OSC when driven externally)	V_{IH_1}	2.4	V_{DD}	V	
Logic Input High Voltage ($\overline{RESET}$ and OSC)	V_{IH_2}	4	V_{DD}	V	
Logic Output High Voltage (Note 2)	V_{OH}	2.4		V	I_{OH} = 100 μA
Logic Output Low Voltage	V_{OL}	—	0.45	V	I_{OL} = 1.6μA, V_{XX} = 4.5V
	—	—	0.90	V	I_{OL} = 5mA, V_{XX} = 9V
	—	—	0.50	V	I_{OL} = 5mA, V_{XX} = 9V
	—	—	0.90	V	I_{OL} = 10mA, V_{XX} = 9V (Note 1)
AC CHARACTERISTICS					
Oscillator frequency variation for a fixed RC network	Δf	−20%	+20%		@ CLK OUT 167KHz (Note 3)
CLK OUT Output					
Period	t_{CY}	4	20	μs	
High Pulse Width	t_{CLKH}	¼ t_{CY}			
Low Pulse Width	t_{CLKC}	¾ t_{CY}			

NOTES: 1. Total I_{OL} for all registers must be less than 150mA under any conditions
2. Except following pins which have open drain outputs/inputs: 6, 7, 8, 12 and 13.
3. Test circuit:



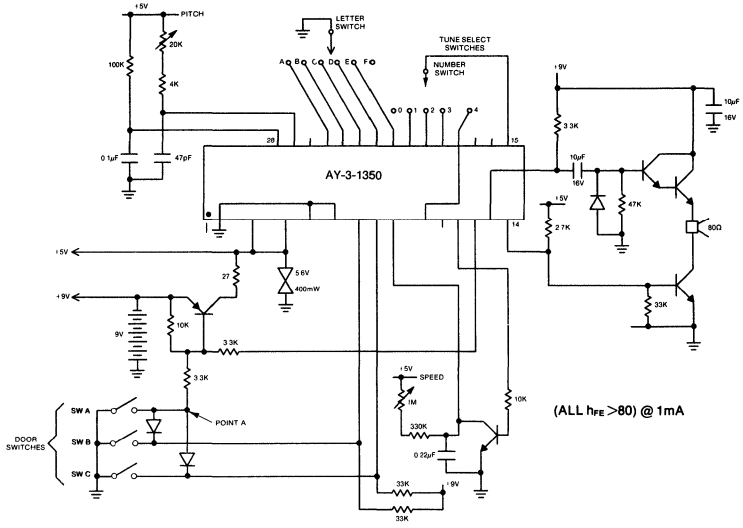


Fig. 1 SYSTEM DIAGRAM

OPERATION SUMMARY

Use of the AY-3-1350 can be split into three groups which are described in detail in separate sections:

ONE CHIP AY-3-1350 system generating 25 tunes plus 3 chimes which have been pre-programmed into the standard device

ONE CHIP AY-3-1350 system generating any number of tunes desired. This involves mask programming during manufacture and is usually not suitable for small quantity production.

TWO CHIP AY-3-1350 plus PROM system generating any tunes desired as above, but using the standard device so that applications, including small quantities, become feasible. (CMOS gate also required.)

ONE CHIP STANDARD AY-3-1350 SYSTEM

Typical Implementation

There are many ways to connect the standard device depending on the exact application. Figure 1 shows just one implementation of the device in a doorchime. This circuit gives access to all 25 tunes from switch A and one of 5 tunes from switch C as well as the descending active chime from switch B. The tune selected for switch B follows the tunes list according to the setting of the two tune select switches (A—E and 0—4). The tune selected from switch C in Figure 1 is one of the five tunes A0 through E0 depending on the setting of the letter switch. For example, with the letter switch set at E and the number switch set at 4, the tunes available will be:

Switch A: Beethoven's 9th (E4)
Switch C: Yankee Doodle (E0)
Switch B: Descending Octave Chime (Chime Z)

When the letter switch is in position F there will be chimes on all doors independent of the number switch setting as follows:

Switch A: Westminster Chime
Switch C: Simple Chime
Switch B: Descending Octave Chime

There is virtually no power consumption in the standby condition (external transistor leakages only). When any door switch is activated the circuit powers up, plays a tune, and then automatically powers down again to conserve the battery, even if the operator keeps his finger on the switch to the end of the tune. He must release it and re-press to play again with the circuit in Figure 1. Activating any of the door switches will pull point A to ground turning on the PNP transistor in the power supply line. This causes +5V to be applied to the AY-3-1350 and the first operation of the chip is to put ON/OFF (pin 12) to logic 0. This maintains the power through the PNP, even after the switch is released. The device can turn off its own power at the end of a tune by raising ON/OFF to logic 1.

Figure 1 shows only a typical one-chip implementation. Further options come from use of different switching and/or from use of the next tune facilities built into the chip. These will now be considered in turn.

Switching Options

In Figure 1 the Switch C Group Select pin (16) is not connected, and one of the five tunes (A0 through E0) will play if switch C is activated. Other number groups can be chosen by connecting the Switch C Group Select pin as follows:

TABLE 2

Switch C Group Select pin (16) is connected to:	Switch C Tunes
no other pin	A0—E0
Tune Select 1 (pin 20)	A1—E1
Tune Select 2 (pin 19)	A2—E2
Tune Select 3 (pin 18)	A3—E3
Tune Select 4 (pin 9)	A4—E4

Which of the five possible switch C tunes will be played depends on the current setting of the LETTER SWITCH A—E.

Switch C selection can be made by hard-wire connection for a permanent selection or a third switch can be added for an additional group selection feature.

LED Direct Drive

Vxx drives the gate of the output buffer, allowing adjustment of drive capability:

Vxx	Vout	Isink (typ.)
5V	0.4V	2.5mA
5V	0.7V	4 2mA
10V	0 4V	5.8mA
10V	0.7V	10.0mA
10V	1.0V	14.1mA

AUDIO

Using the power-up circuit of Figure 1, the AY-3-1350 will have +5V applied and be latched within a few microseconds (dependant upon external components) from any bell-push closing. The device starts to operate when the RESET pin reaches logic 1 (about 10ms with components shown) but in fact the tune select switches are not interrogated until approximately 6ms later. The total is sufficient for most bell-pushes to complete any bounce period and for a firm selection of tunes to be made.

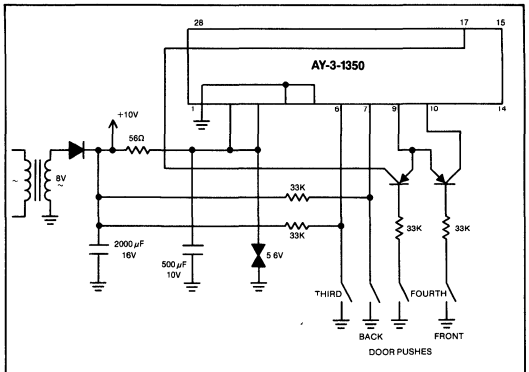
Next Tune Facilities

At the end of tune play the circuit of Figure 1 powers down because ON/OFF (pin 12) is raised to a logic 1. This simplified flow diagram in Figure 3 shows that before the power down there is a test for connection between NEXT TUNE (pin 10) then RESTART (pin 17) with TUNESELECT 4 (pin 9). At this time NEXT TUNE (pin 10) then RESTART (pin 17), which are normally at logic 1, output a logic 0. This is looked for at input TUNESELECT 4 (pin 9). If neither is found the power down system is reached as in Figure 1.

A NEXT TUNE (pin 10)—TUNE SELECT 4 (pin 9) connection at the moment of test causes the next tune in the list to be played after a short pause (equal to a musical breve—the actual time depends on the setting of the tune speed control). The order of the tunes is A0 to E4 as given in the listing of standard AY-3-1350 tunes. If the last tune (E4) was played then the circuit will go on to play the first tune A0 (and then successive ones). The chimes are not included in the cycling sequence.

A RESTART (pin 17)—TUNESELECT 4 (pin 9) connection at the moment of test at the end of a tune causes the same selected tune to be played again. Figure 3 shows that in this case the tune sensing mechanism is passed through once more so the tune would be different the second time if the switches were altered while the first tune was playing.

The connections referred to cannot be permanent because otherwise the circuit would never stop playing tunes. Figure 2 shows how transistors are used to make the connection in a practical application.



PIN	FUNCTION
6	DOOR 3
7	BACKDOOR
9	TUNESELECT 4
10	NEXT TUNE
17	RESTART

Fig. 2

ONE CHIP CUSTOM TUNES SYSTEM

Customizing the Tunes

The AY-3-1350 has pre-programmed tunes, but the device is mask programmable during manufacture with any music required. A minimum of 1 tune to a maximum of 28 tunes can be incorporated. Examples as follows:

Tunes	Total No. of notes, all tunes together	Average notes per tune
1	252	252
2	251	126
5	248	50
10	243	24
20	233	12
25	228	9

(The general formula is Total No. of notes = 253—No. of tunes.)

As an indication, about 90 seconds of music can be incorporated

All musical rests are counted as one note. Semiquavers, quavers, dotted quavers, crotchets, dotted crotchets, minims, dotted minims and semibreves can all be accommodated. The range is about 2½ octaves. The position of these octaves can be chosen by the user up to a maximum pitch of A = 1760Hz. The tunes for incorporation in the device should be presented to General Instrument as normal music manuscript.

Applications for Customized Tunes

If the number of tunes is less than the number of switch positions then the circuit will automatically proceed directly to power down if this mode is being used, or will find the next available tune if in the sequential mode.

All the different facilities described are still available when user tunes are masked into the device.

For toys, sequential tune playing adds variety and reduces the number of switches required, keeping costs to a minimum.

For musical boxes, playing the same tune repeatedly preserves the traditional features.

TWO CHIP STANDARD AY-3-1350 PLUS PROM SYSTEM

Introduction

With the addition of an external ROM or PROM the standard AY-3-1350 will play almost any tune or tunes desired. 28 tunes averaging 8 notes each or one tune of up to 252 notes is available. General Instrument can later integrate the external tunes into the main synthesizer to give a one chip system.

Overall Coding Scheme

The external PROM should be 256 x 8 bits and of any static TTL compatible type.

It can have more words, but the tunes synthesizer will only use 256 x 8 bits at a time, e.g. if PROM type 2708 is used (1K x 8 bits), the two higher order address lines should be connected to ground or switches put on them to give 4 times the amount of music (see logic diagram Figure 4). The rest of this article will assume a 256 x 8 bit PROM, and the addresses will be referred to as 000 to 377 Octal notation is used throughout.

The PROM address 000 must contain data 377 and address 377 must contain data 125 which is a key to open up the external PROM features All other addresses can contain tune data.

Each tune consists of a series of notes with one byte of PROM for each. Every tune must have a tune end marker byte 377 after the last note, and the final tune must have a byte 376 after the 377 end marker The memory allocation is shown diagrammatically in Figure 5. Tunes can be of any length and there can be any number of them subject only to the memory limit (28 max.).

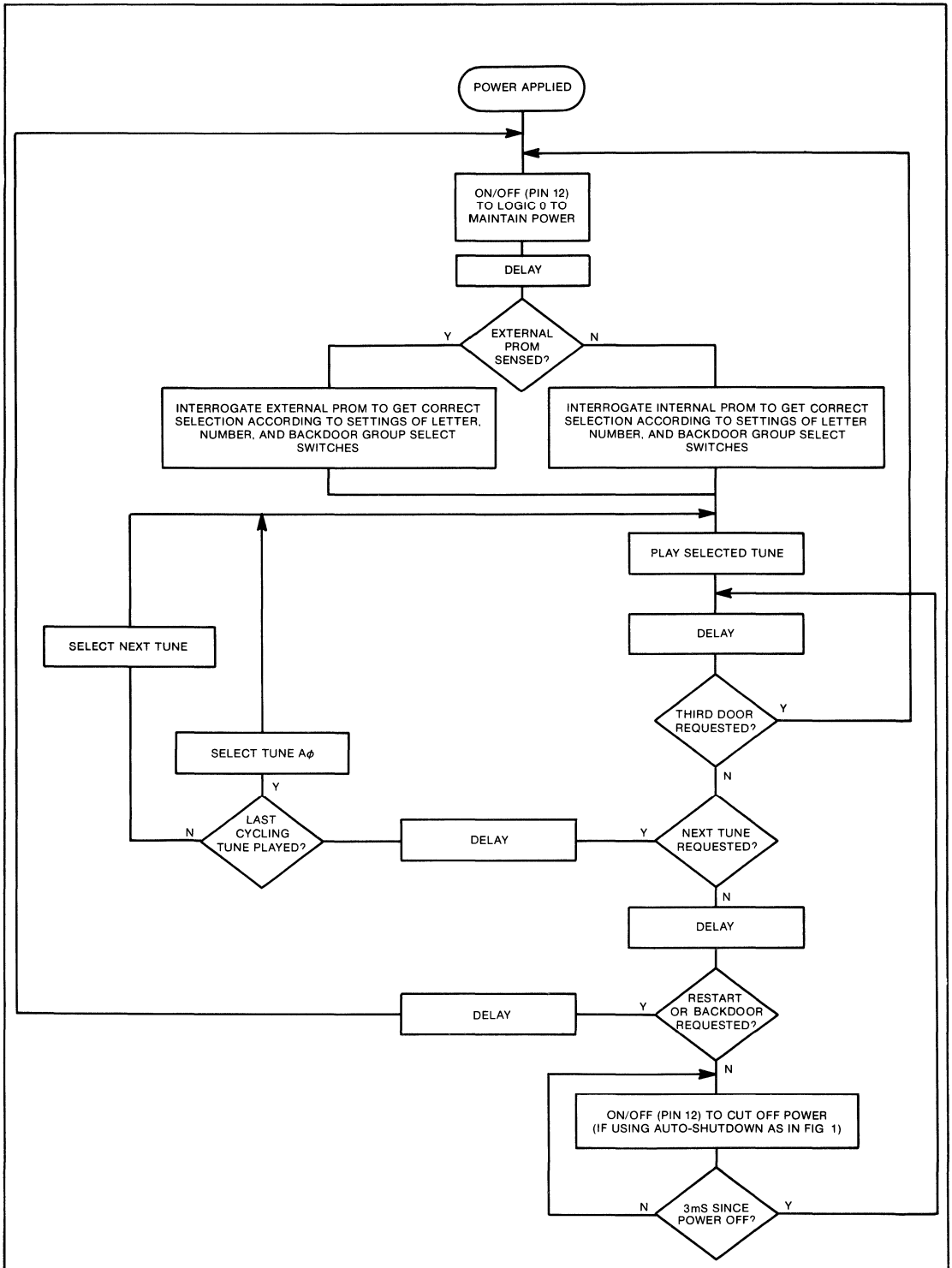


Fig. 3 SIMPLIFIED FLOW DIAGRAM

AUDIO

PROM Memory Allocation

Address	DATA	
0	377	(tunes select timeslot)
		Tune 1
	377	(end of tune marker)
		Tune 2
	377	(end of tune marker)
		More tunes
		Last Tune
	377	(end of tune marker)
	376	(end of listing)
	000	Not used
	000	
	000	
	000	
377	125	(external ROM enable key)

Fig. 4

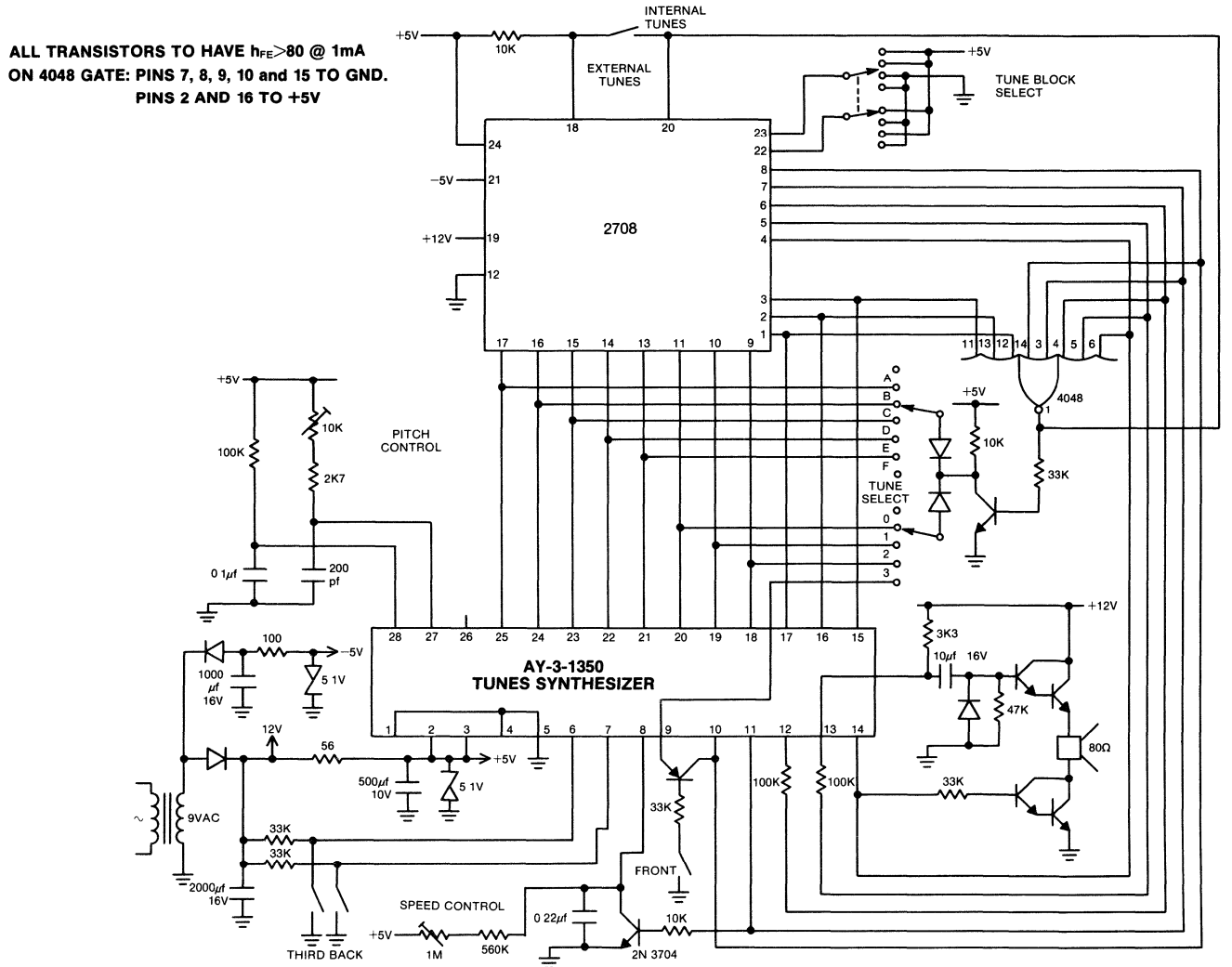


Fig. 5 PLAYING YOUR OWN TUNES WITH EXTERNAL PROM (OR INTERNAL TUNES)

Telephony 6

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			Dialers
PUSHBUTTON TELEPHONE DIALERS	Converts pushbutton input to rotary dial pulses.	AY-5-9151A/B	6-4
		AY-5-9152/B	6-4
		AY-5-9153A/B	6-4
		AY-5-9154A	6-4
LOOP DISCONNECT DIALER	Pushbutton-rotary dial converter with re-dial.	AY-5-9158	6-11
MULTI-FREQUENCY DIALER	Dialer with dual tone.	AY-5-9559	6-14
			Multi-Frequency Generators
DUAL TONE MULTI-FREQUENCY GENERATORS	Generates DTMF/tone telephone frequencies.	AY-3-9400	6-18
		AY-3-9410	6-18
			Code Conversion
CODEC	Duplex Delta-Sigma/PCM converter.	AY-3-9900	6-22
			Programmable Dialers
PROGRAMMABLE MICRO-COMPUTER TELEPHONE DIALERS	Single chip microcomputer pre-programmed for in-telephone applications.	TZ-2001	6-30
		TZ-2002	6-30
		TZ-2003	6-30

GENERAL INSTRUMENT

Dialers

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
PUSHBUTTON TELEPHONE DIALERS	Converts pushbutton input to rotary dial pulses.	AY-5-9151A/B	6-4
		AY-5-9152/B	6-4
		AY-5-9153A/B	6-4
		AY-5-9154A	6-4
LOOP DISCONNECT DIALER	Pushbutton-rotary dial converter with re-dial.	AY-5-9158	6-11
MULTI-FREQUENCY DIALER	Dialer with dual tone	AY-5-9559	6-14

Push Button Telephone Dialers

FEATURES: AY-5-9151A

- 2.5V to 5V and 200μA operation, plus standby mode
- Frequency of on-chip clock set by external RC network
- Selectable break: make ratio and interdigital pause
- Uses 3 x 4 matrix keyboard with no keyboard ground or common contact
- Keyboard inputs have antibounce protection
- Input pull-up or pull-down resistors on-chip
- Redial and access pause controlled from keyboard
- 22 digit capacity including access pauses
- Dialer reset for line power breaks>200ms.

FEATURES: AY-5-9151B. Same as AY-5-9151A except:

- 18 Pin package

FEATURES: AY-5-9152. Same as AY-5-9151A except:

- Break: Make fixed at 60:40 plus:
- Two antiphase mask outputs for driving bistable relay

FEATURES: AY-5-9152/B. Same as AY-5-9152 except:

- 18 Pin package

FEATURES: AY-5-9153A. Same as AY-5-9151A when in 3 x 4 matrix keyboard mode plus:

- Pin selectable options of 1 of 12 keyboard, 2 of 7 keyboard wired to produce 4-bit code with common
- 8 bit output for displaying number in digit store
- Simple call-barring facility using display outputs

FEATURES: AY-5-9153B. Same as AY-5-9153A except:

- Keyboard is binary input with common

FEATURES: AY-5-9154A. Same as AY-5-9153A except:

- Break: Make fixed at 60:40 plus:
- Two antiphase mask outputs for driving bistable relay

DESCRIPTION

This range of CMOS Pushbutton Dialers consists of seven devices AY-5-9151A to AY-5-9154A, all of which perform the function of converting input data (e.g. from a keyboard) into a series of pulses suitable for loop disconnect dialing. The series is based on two devices: a simple, basic dialer circuit and a more complex and versatile device which accepts a variety of data entry codes and has a display facility.

The use of CMOS technology results in low voltage and current requirements, enabling easy interfacing with a variety of telephones. The versatility of the devices and the low external component count enables the building of sophisticated, reliable telephones at low cost.

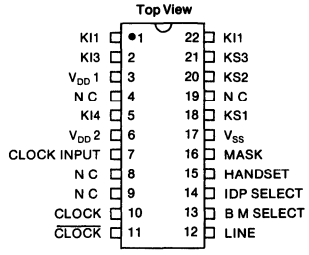
Part Number	Min Supply Voltage	# of Pins	IDP Pin Select	B:M Pin Select	# of Positive Voltage Supply Pins	Keyboard	Two Antiphase Mask Outputs	Display Capability
*AY-5-9151A	2.5V	22	700, 800 500ms	yes	2	4 x 3	no	no
*AY-5-9151B	2.5V	18	700, 800 500ms	yes	2	4 x 3	no	no
*AY-5-9152	2.5V	22	700, 800 500ms	fixed (60:40)	2	4 x 3	yes	no
*AY-5-9152/B	2.5V	18	700, 800 500ms	fixed (60:40)	2	4 x 3	yes	no
*AY-5-9153A	2.5V	28	700, 800 500ms	yes	2	4 x 3 1 of 12 4 bit & common	no	yes
*AY-5-9153B	2.5V	28	700, 800 500ms	yes	2	binary input	no	yes
*AY-5-9154A	2.5V	28	700, 800 500ms	fixed (60:40)	2	4 x 3 1 of 12 4 bit & common	yes	yes
*AY-5-9158	2.5V	18	800, 500ms	fixed (66.7:33.3)	1	4 x 3	no	no

*Redial capability: 22 digits
Dial Rate: 10pps

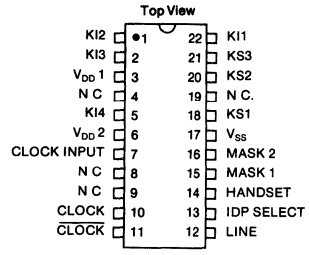
PIN CONFIGURATIONS

22 LEAD DUAL IN LINE

AY-5-9151A



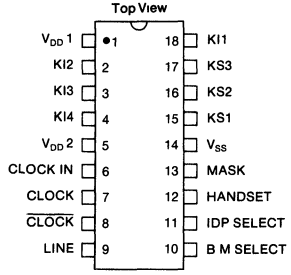
AY-5-9152



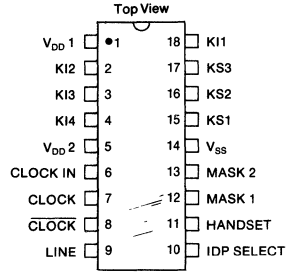
PIN CONFIGURATIONS

18 LEAD DUAL IN LINE

AY-5-9151B



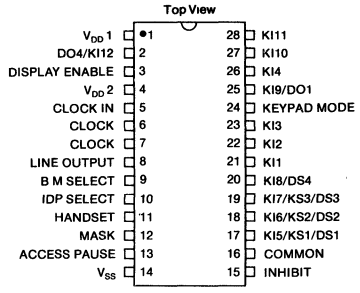
AY-5-9152B



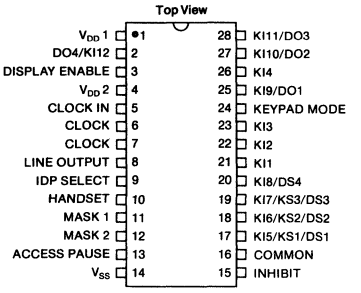
PIN CONFIGURATIONS

28 LEAD DUAL IN LINE

AY-5-9153A/9153B



AY-5-9154A



PIN FUNCTIONS

V_{SS} - The negative supply to the device. All voltages are referenced to this pin.

V_{DD1} - The positive supply to the digit store and write counter. Power must be maintained on this pin if the redial function is used.

V_{DD2} - The positive supply to the clock generator and control logic. V_{DD2} should rise to 2.5V within 20ms of switch-on.

Clock In, $\overline{\text{Clock}}$, Clock - These pins are connected to an external RC network which controls the frequency of the clock generator and hence the timing of the line and mask outputs.

Handset Input - The state of the handset is used to control this input, a logic 1 on the input indicating that the handset is on-hook and a logic 0 indicating that the handset is off-hook. This input is used to reset the control logic depending on the past history of the input.

If the input is taken from logic 1 to logic 0, and the clock is not oscillating, a reset pulse is produced when clock pulses are detected. The device is then ready for operation.

If the input is taken to logic 1 for less than 200ms and the clock generator is operating throughout this period, a reset pulse is not produced when the input is taken back to logic 0. Thus short breaks in line power will not affect the operation of the circuit.

If the input is taken to logic 1 for more than 200ms, and clock pulses are present throughout this period, a reset pulse will be generated at the end of the 200ms period.

Line Output - The loop disconnect dial pulses appear at this output. It is an open drain output with the source of the output transistor being connected to V_{SS}. A break period corresponds to this transistor being switched on and a make period or IDP corresponds to the transistor being switched off. The first digit of any outdialing sequence is preceded by a pre-digit pause equal in length to an interdigital pause.

Mask Output/Mask 1 Output - This is a push-pull output and is used to mute the telephone speech circuit. A logic 1 indicates that the speech circuit is to be muted, this occurring immediately on recognition of an input from the keypad.

Mask2 Output — The AY-5-9152/B and AY-5-9154A are fixed at 60:40 Break Make ratio and a Mask 2 output is substituted for the Break Make input. The mask 2 output is identical to the mask 1 but is driven in antiphase to enable a bistable mask relay to be used

On initial application of power, a pulse is produced on Mask 1 and Mask 2 outputs to reset a bistable relay which may be connected to these outputs.

IDP Input - This pin is used to select the duration of the interdigital pause. With a clock frequency of 18kHz, interdigital pauses of 700, 800 or 500ms may be selected.

Break: Make Ratio — A choice of four break make ratio is available as a pin programmable option, 70:30, 66 6.33 3, 60.40 and 50 50

Display Enable - When display data is being output from the dialer, this output goes to a logic 1.

Common Input - When a 4 bit code is used for data input a logic 1 on this input strobes the data into the device. Antibounce protection is provided for this input. A steady logic 1 of less than 5ms duration will not be recognized and a steady logic 1 of greater than 10ms duration will be recognized. This input has a pull down resistor to V_{SS}.

Inhibit Input - This is used to inhibit outdialing. If a logic 1 is placed on this input while a digit is being dialed, outdialing will cease when the digit has been completed. If the logic 1 appears during an IDP, outdialing will cease immediately. When outdialing has ceased, the Mask 1 output goes to logic 0 and Mask 2 goes to logic 1. When the input is taken to logic 0, the Mask signal reappears and dialing continues, starting with an IDP.

Access Pause Output - When an access pause is reached in the dialing sequence, this output goes to logic 1. By connecting this to the inhibit input, further outdialing will be prevented.

Keyboard Mode - The data on this pin determines whether the device will accept data from:

a) 1 of 12 keyboard with keyboard ground
b) 2 of 7 keyboard with keyboard ground and common switch
c) 4 bit binary code with common signal
d) 4 x 3 matrix keyboard without keyboard ground and common switch

When modes b, c or d are in use with the AY-5-9153A/B or AY-5-9154A data in the form of two, four-bit words is available for display purposes, except when a key is pressed

Keyboard Inputs/Keyboard Scans/Display Outputs 1 of 12 Mode - All twelve pins are used as keyboard inputs, on-chip pull-up resistors to logic 1 being incorporated A logical AND of the twelve inputs produces an on-chip Any Key Down signal when any input is taken to logic 0. Detection of this signal initiates an anti-bounce period and at the end of this period, the data on the twelve inputs is read into the digit store, provided the Any Key Down signal is present throughout this period. Any further data is then inhibited until an antibounce period has been completed with all keys up If, during the antibounce period, the Any Key Down signal disappears, the antibounce timer will be reset

2 of 7 Mode - Keyboard inputs 1-4 are used for the 4-bit data, the common input strobing the data into the digit store On-chip pull down resistors to logic 0 are incorporated on the four data inputs and the common input When the common input is taken to logic 1, an antibounce timer is started and if the common input is at logic 1 throughout, the data is read at the end of the period. Further data is then inhibited until the common input has been at logic 0 for an antibounce period.

Binary Mode - The 4-bit word is entered into the digit store via inputs 1-4 by use of the common input, in a similar manner to the 2 of 7 mode. On-chip pull down resistors to logic 0 are incorporated. When data is not being read into the device (i e when the common input is at logic 0) these four inputs are used as output pins for a 4-bit word for digit display purposes as described later

4 x 3 Matrix Mode — This function will be described for the AY-5-9151 Series, and AY-5-9152/B. The mode of operation is slightly different for the AY-5-9153A/B and AY-5-9154A, as explained later.

A pulse to logic 0 is sequentially switched around the three keyboard scan outputs, taking 5ms for a complete scan cycle When a key is pressed the pulse appears on one of the four keyboard inputs 1-4 (provided with pull-up resistors to logic 1), and if it occurs on the same input on the next scan cycle, the data is entered into the digit store Before a second key depression may be recognized, the first key must be released and a full scan cycle completed without a pulse on any input.

If two keys are pressed during the same scan cycle, the data will be rejected and again a full scan cycle must be completed without a pulse appearing on any of the inputs before another key depression may be recognized

If a key is pressed during an inhibit period, or two keys are pressed simultaneously, all three scan outputs will go to logic 0 until the key or keys is/are released.

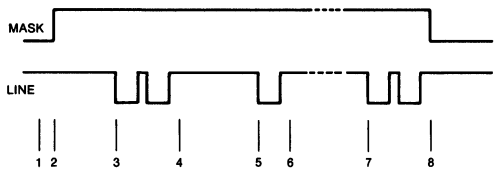
Display Scans/Display Outputs - Data for the first 16 digits and access pauses in the store is available for display.

The position of a digit within a telephone number is indicated by a 4 bit binary word from the Display Scan outputs. Display Scan 1 is the least significant bit and Display Scan 4 is the most significant bit. Binary word 0000 corresponds to the left-hand digit of the display (the first number entered) and 1111 corresponds to the right-hand (16th) digit of the display.

The digit being output is available as a 4 bit word on the display outputs (Display Out 1 = least significant bit) Binary word 0001 represents digit 1 and so on to 0000 = digit 10 Access pauses are represented by 1011.

When in the 2 of 7 mode or the Binary mode, the display data is inhibited by the appearance of the common signal When in the 4×3 matrix mode, depression of a key causes display scan data to appear on the keyboard inputs. The dialer then reverts to the normal keyboard scanning mode of operation.

LINE AND MASK OUTPUT TIMING



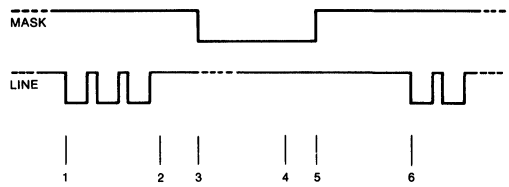
The above sequence of events is that which occurs when the digit store is initially empty. The time intervals quoted in the following explanation are valid only for a clock frequency of 18kHz. The time intervals are inversely proportional to the clock frequency.

	Event	Time Interval
1	The first key is depressed and the anti-bounce timer is started	T_{1-2} = 5-10ms after end of bounce
2	The data from the keyboard is accepted. The mask output appears and the pre-digital pause commences. This is the same duration as the inter-digital pause and is pin selectable.	T_{2-3} = 700, 800, or 500ms
3	Dialing of the first digit starts. The example shown is a digit 2.	$T_{3-4} = n \times 100$ms where n = digit dialed
4	End of 1st digit and start of inter-digital pause.	T_{4-5} = 700, 800, or 500ms
5	Dialing of 2nd digit starts. The example shown is a digit 1.	$T_{5-6} = n \times 100$ms where n = digit dialed
6	End of 2nd digit and start of inter-digital pause.	T_{6-7} = 700, 800, or 500ms

Dialing of further digits continues in a similar manner until the last digit.

7	Dialing of last digit commences, in this case a digit 2.	$T_{7-8} = n \times 100$ms where n = digit dialed
8	End of last digit and end of mask signal.	

EFFECT OF ACCESS PAUSE ON LINE AND MASK OUTPUT TIMINGS



The following time intervals are valid only for a clock frequency of 18kHz.

	Event	Time Interval
1	Dialing of the last digit before the access pause commences. A digit 3 is shown in this example.	$T_{1-2} = n \times 100$ms where n = digit dialed.
2	The end of the last digit before the access pause.	T_{2-3} = 700, 800, or 500ms
3	The mask signal is removed so that the telephone user can listen for the appearance of the second dial tone.	
4	The telephone user presses the # key to release the access pause. The antibounce timer is started.	T_{4-5} = 5-10ms
5	The data from the # key is accepted or the inhibit input is taken to logic 0 and the mask signal reappears. A pre-digital pause equal in length to an inter-digital pause starts.	T_{5-6} = 700, 800, or 500ms
6	The digit after the access pause is dialed out. Dialing then continues as normal.	

Access Pause and Redial Operation

These facilities are available on all devices, control being via the keypad or data input codes The 1 of 12 keypad and 4 × 3 keypad use the '*' button to insert an access pause and the '#' button to release the access pause.

The '#' button may also be used to redial the number in the digit store. If the redial mode is used, power must be maintained on V_{DD1} at all times.

PIN SELECTABLE OPTIONS

a) Break:Make Ratio

Ratio	Voltage On Pin
70:30	Clock
66.6.33.3	V_{DD}
60:40	V_{SS}
50.50	Clock

b) IDP (with 18kHz clock frequency)

IDP	Voltage on Pin
700ms	V_{DD} 2
800ms	V_{SS}
500ms	Clock

c) Keyboard Mode

Mode	Voltage On Pin
2 of 7	V_{DD}
3 × 4	V_{SS}
1 of 12	Clock
Binary	Clock

DATA INPUT CODES

KI = Keyboard Input

Binary

KI 4	KI 3	KI 2	KI 1	Digit
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	Access Pause
1	1	0	0	Redial

2 of 7

KI 1	KI 2	KI 3	KI 4	Digit
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
1	0	0	0	7
1	0	0	1	8
1	0	1	0	9
0	0	1	1	10
1	1	0	0	Access Pause
1	1	0	1	Redial

4-bit codes other than those shown above are ignored.

DATA OUTPUT CODES

Display Scan (DS)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DS4	DS3	DS2	DS1	Position
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

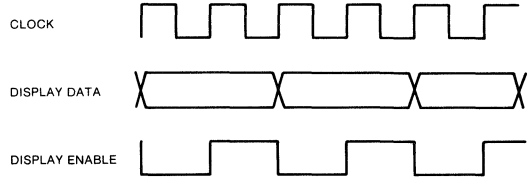
Display Outputs (DO)

DO4	DO3	DO2	DO1	Digit
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
0	0	0	0	0
1	0	1	1	Access Pause

The Display Scan outputs are continuously incremented, and the Display outputs changed accordingly, to enable the display of all the digits in the digit store by the use of multiplexing.

The Display Scan code is incremented at half the clock frequency.

The relationship between Clock, Display Data out and Display enable is as follows.



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} ..... +7.0V to −0.3V
Storage Temperature Range ..... −65° C to +150° C

Standard Conditions (unless otherwise noted):

$V_{SS} = 0V$
$V_{DD1} = V_{DD2} = 2.5V$ to $5.0V$ ($V_{DD1} \geq V_{DD2}$)
$T_A = -25°C$ to $+85°C$

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Clock frequency = 18kHz The device will function correctly from 8kHz to 50kHz but all timings (break period, IDP etc.,) will be directly dependent on the clock period.

Characteristic	Min.	Typ.	Max.	Units	Conditions
Inputs					
IDP, B:M, Key Pad Mode					
Logic '0' Level	−0.3	—	0.2	V	
Logic '1' Level	V_{DD2} −0.2	—	V_{DD2}+0.3	V	
All Other Inputs					
Logic '0' Level	−0.3	0	0.5	V	Note 1
Logic '1' Level	V_{DD2} −0.5	V_{DD}	V_{DD2} +0.3	V	
Capacitance	—	—	10	pF	$V_{IN} = V_{SS}$, f = 1MHz
CURRENT SOURCE TO V_{DD2}					
Keyboard Inputs	2	—	60	μA	
CURRENT SINK TO V_{SS}					
Keyboard Inputs Common IDP, B:M	3	—	90	μA	
	0.6	—	15	μA	
Clock In Leakage Current	—	—	20	nA	$T_A = +25°C$
					$V_{IN} = V_{SS}$ or V_{DD1}
Key Depression Period	10	—	—	ms	
OUTPUTS					
LINE:					
Logic '0' Output Current	2	—	—	mA	$V_O = 1.0V$
Logic '1' Leakage Current	—	—	1	μA	$V_O = 5.0V$
MASK:					
Logic '0' Output Current	2	—	—	mA	$V_O = 1.0V$
Logic '1' Output Current	2	—	—	mA	$V_O = V_{DD2} - 1.0V$
ALL OTHER OUTPUTS:					
Logic '0' Output Current	0.1	—	—	mA	$V_O = 1.0V$
Logic '1' Output Current	0.1	—	—	mA	$V_O = V_{DD} - 1.0V$
CLOCK FREQUENCY	17.2	—	18.6	kHz	$V_{DD1} = V_{DD2} = 3.75V$
	14.3	—	—	kHz	$V_{DD1} = V_{DD2} = 2.5V$
	—	—	19.5	kHz	$V_{DD1} = V_{DD2} = 5.0V$
Temperature Stability	—	—	±2	%	Relative to value at +25° C $V_{DD2} = 5.0V$
	—	—	±5	%	Relative to value at +25° C $V_{DD2} = 2.5V$
SUPPLY CURRENT					
I_{DD1}	—	—	7	μA	$V_{DD1} = 5.0V$, $V_{DD2} = 0V$
I_{DD2}	—	—	200	μA	$V_{DD2} = 5.0V$, Note 2

NOTES:

1. The device will function correctly with a maximum logic '0' of 1.0V and a minimum logic '1' of V_{DD} −1.0V. However, use under these conditions may result in an increased supply current.
2. Measured with Break: Make, IDP, Inhibit and Keyboard Mode inputs at V_{SS}, and with no keys depressed.

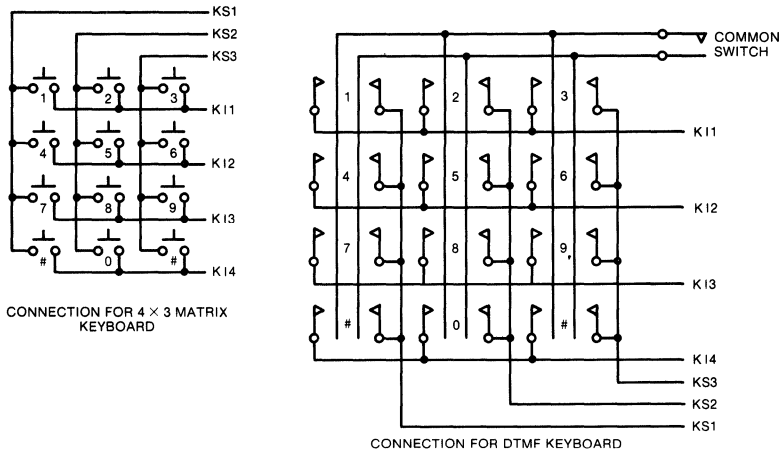


Fig. 1 KEYBOARD CONNECTIONS FOR AY-5-9151A & AY-5-9152

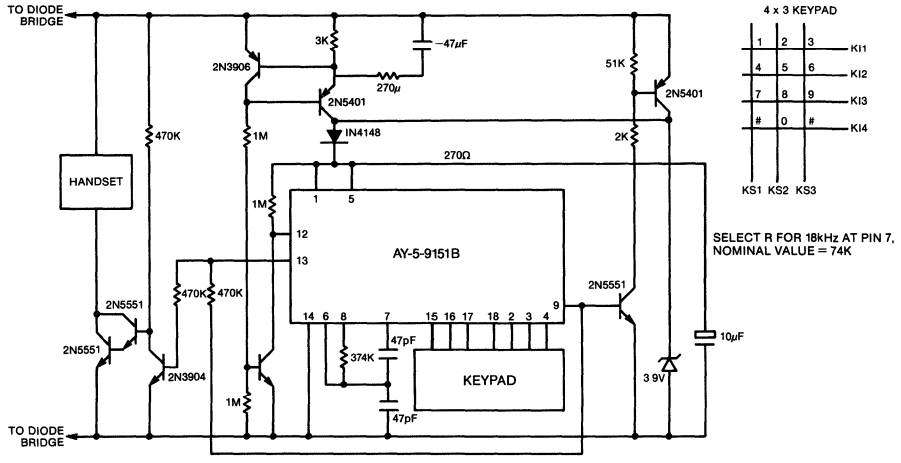


Fig. 2 PROVISIONAL PUSH-BUTTON DIALER CIRCUIT USING AY-5-9151A

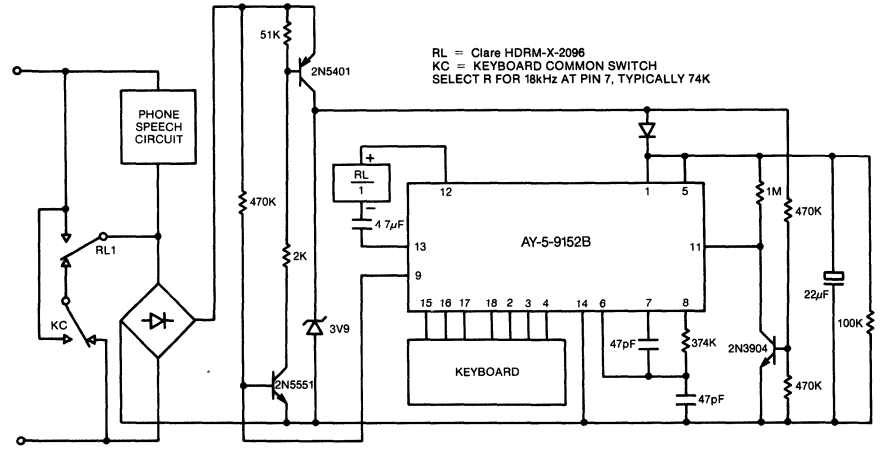


Fig. 3 PUSHBUTTON DIALER USING MASK RELAY

Loop Disconnect Dialer

FEATURES

- 2.5 to 5.0V supply voltage
- Low power standby mode for redial
- On-chip clock generator
- 4 × 3 matrix single contact keypad
- Pin selectable IDP
- On-chip input pull up/down devices
- Redial and access pause controlled from keypad
- 22 digit capacity including access pauses
- Plastic or Ceramic package

DESCRIPTION

The AY-5-9158 is a CMOS loop disconnect dialer with full access pause and redial capabilities, featuring pin-programmable Interdigital Pause. The use of a low voltage CMOS process realizes well known advantages of low power and high noise immunity, particularly desirable features in a loop disconnect telephone dialer.

PIN FUNCTIONS

V_{SS}

This should be connected to the negative terminal of the power supply to the dialer. Voltages on all other pins of the dialer are normally referenced to this pin

V_{DD}

This should be connected to the positive supply of the dialer. If the redial facility is required, power must be maintained on this pin when the handset is on-hook

Clock Input, Clock and $\overline{\text{Clock}}$

The clock pulse generator consists of two inverters, the frequency of oscillation being controlled by external components connected to these three pins. The circuit is sufficiently versatile to allow the use of a variety of external component configurations. Figure 1 shows the configuration used throughout this data sheet Details of the performance of this circuit are given in the section describing electrical characteristics

IDP Select

The signal applied to this pin controls the duration of the interdigital pause as follows

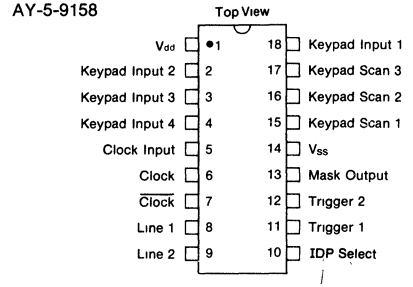
Voltage on Pin	IDP
V_{SS}	800ms
Clock	500ms

The pin may also be connected to $\overline{\text{CLOCK}}$ This increases the keypad scan frequency and outdialing frequency by a factor of 15 to facilitate high speed testing of the device. The data on this pin is read during a reset controlled by the Trigger 1 input. This pin has an on-chip pull down device to V_{SS}

Line 1 and Line 2 Outputs

The loop disconnect dial pulses appear at these outputs. The ouput stage is a push-pull type with separate pins for the drains of

PACKAGE INFORMATION
PIN CONFIGURATION
18 LEAD DUAL IN LINE
AY-5-9158



the output transistors as shown in Figure 2. During a dial pulse break period, the N channel device is off and the P channel device is on, creating a logic 1 at the Line 2 output During a make period and an IDP the N channel device is on and the P channel device is off, creating a logic 0 at the Line 1 output. The timing of the Line 1 output relative to the Mask output is shown in Figure 3. The Break:Make ratio is fixed at 66 7 33.3.

Mask Output

This is a push-pull output and is used to control the muting of the telephone speech circuit during dialing. A logic 1 indicates that the telephone is to be muted, the transition to logic 1 occurring immediately on recognition of a key depression

Keypad Scans 1-3

These are push-pull outputs used to scan the keypad columns at a rate of 200Hz Figure 4 shows how these outputs are connected to the keypad

Keypad Inputs 1-4

The keypad contacts are used to connect one keypad scan output to one keypad input to enable recognition of a key depression Each of these inputs has an on-chip pull up device to V_{DD} For a description of how the keypad inputs recognize data, see Section 2.

Trigger 1 and Trigger 2

These are connected to the input and output respectively of two inverters in series as shown in Figure 5 Connection of resistors R1 and R2 allows a Schmitt trigger circuit to be realized, the switching thresholds being determined by the values of these resistors. The characteristic of the Schmitt trigger is shown in Figure 6 If the input voltage V_T is lower than the lower threshold V_{TL}, the clock generator is stopped and the scan outputs become high impedance. In this state the dialer consumes only a small leakage current and data in the RAM is maintained. If V_T is increased and exceeds V_{TH} the clock generator is started, the read and write counters are reset and a pulse appears at the Mask output as shown in Figure 7. The duration of the pulse is 16-19ms for a clock frequency of 18kHz.

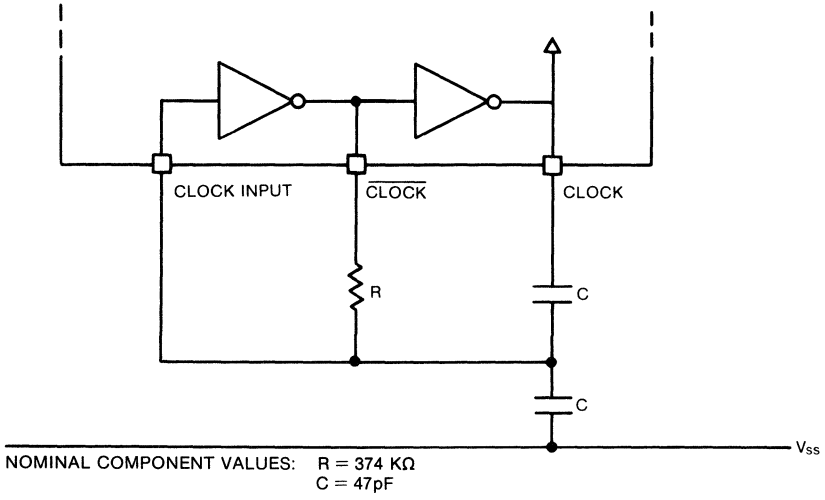


Fig. 1

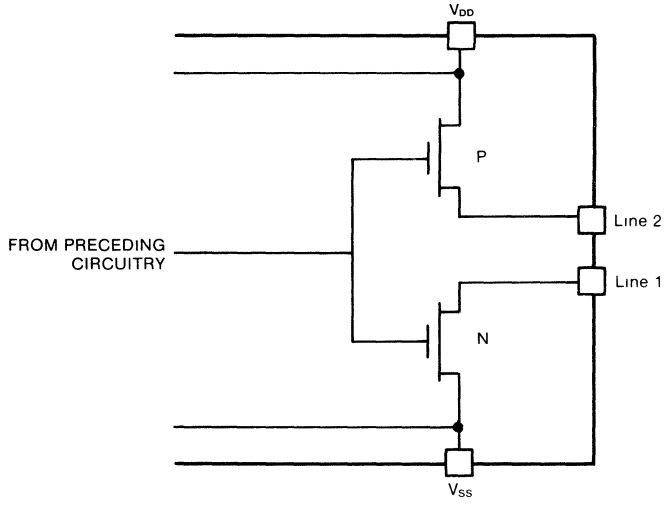
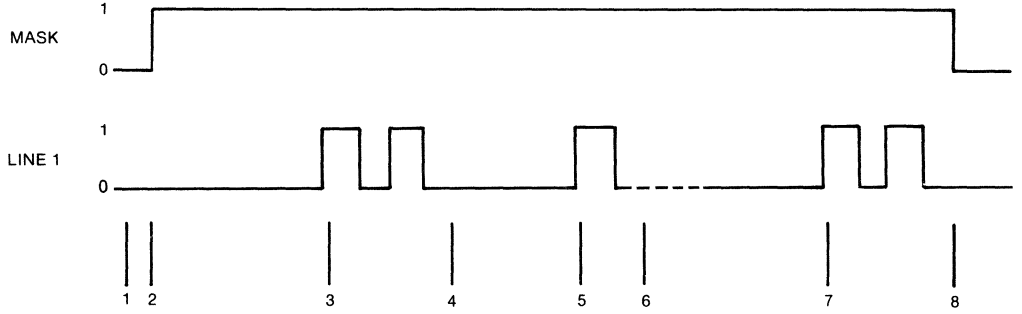


Fig. 2



The above sequence of events is that which occurs when the digit store is initially empty. The time intervals quoted in the following explanation are valid only for a clock frequency of 180kHz. The time intervals are inversely proportional to the clock frequency.

Fig. 3

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} ..... +7.0 to −0.3
Storage Temperature Range ..... −65° C to +150° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

V_{SS} = 0.0V
V_{DD} = 2.5V to 5.0V
Ambient Temperature = −25° C to +80° C
Clock frequency = 18kHz nominal (set by components shown in Fig. 1)

Characteristics	Min	Typ	Max	Units	Conditions
Supply Current					
I_{DD}	—	—	7	μA	V_{dd} = 5 0, V_{TL} = 0.0
	—	90	240	μA	V_{dd} = V_{TL} = 5 0V
					Note 1.
Inputs					
KEYPAD SCANS·					
Logic '0'	−0 3	—	0 5	V	
Logic '1'	V_{DD}	—	V_{DD}	V	
	−0.5	—	+0.3	V	
IDP.					
Logic '0'	−0 3	—	0 2	V	
Logic '1'	V_{dd}	—	V_{dd}	V	
	−0 2	—	+0.3	V	
V_{TH}	1.76	—	2.63	V	V_{DD} 3 6V, with specified Values of R1 and R2.
V_{TL}	.96	—	1.84	V	Note 2.
CURRENT SOURCE TO V_{DD}.					
Keypad Inputs	2	—	60	μA	V_{IN} = V_{SS}
CURRENT SINK TO V_{SS}.					
IDP	0 6	—	15	μA	V_{IN} = V_{DD}
LEAKAGE CURRENT:					
Trigger 1, Clock 1	—	—	20	nA	T_A = +25 °C, V_{IN} = V_{DD} or V_{SS}
Outputs					
MASK:					
Logic '0' Output Current	2	—	—	mA	V_O = 1.0V
Logic '1' Output Current	2	—	—	mA	V_O = V_{dd} −1.0V
LINE 1.					
Logic '0' Output Current	2	—	—	mA	V_O = 1 0V
Logic '1' Leakage Current	—	—	1	μA	V_O = V_{DD}
LINE 2:					
Logic '0' Leakage Current	—	—	1	μA	V_O = V_{SS}
Logic '1' Output Current	2	—	—	mA	V_O = V_{DD} −1 0V
KEYPAD SCANS, Trigger 2.					
Logic '0' Current	100	—	—	μA	V_O = 1 0
Logic '1' Current	100	—	—	μA	V_O = V_{DD} −1 0V
Clock Frequency	17.2	—	18 6	kHz	V_{DD} = 7 75V
	14 3	—	—	kHz	V_{DD} = 2.5 T_A = +25 °C
	—	—	19 5	kHz	V_{DD} = 5 0
Clock Frequency Temperature Stability	—	—	±2	%	Relative to value at V_{DD} = 5.0V
	—	—	±5	%	Relative to value at V_{DD} = 2 5

NOTES
1. Measured with IDP at V_{SS}, Keypad Inputs at V_{DD} and all outputs open circuit.
2. R1 = 330K ohms, R2 = 1.5M ohms.

Dual Tone Multi-Frequency Dialer

FEATURES

- Pin for pin compatible with AMI S2559
- 2.5V to 10V supply voltage
- Uses 3.58MHz crystal to provide high accuracy tones
- 4 x 3 matrix single contact or 2 of 8 "telephone-type" keyboard
- Mute drivers on chip
- On chip reference voltage
- Dual and single tone capability
- Manufactured in General Instrument's proprietary OXI-CMOS* technology

DESCRIPTION

The AY-5-9559 is a digital tone generator designed primarily for use as a DTMF telephone dialer. It is pin for pin and fuctionally equivalent to the AMI S2559 and pin for pin compatible with the Mostek MK5087.

Eight keyboard inputs provide an interface to either an X-Y format or 2 of 8 format (telephone type) keyboard. No common input is necessary. The inputs are arranged as four column and four row inputs, the column inputs being pulled high and the row inputs low by on-chip active current sources/sinks in the absence of a key depression When one key is depressed, a high level is detected on the appropriate row input. This causes the oscillator to start up and a keyboard scan routine to be initiated in order to detect which key has been depressed.

The eight inputs provide the ability for the chip to generate all 16 possible combinations of four low group and four high group frequencies according to Table 1, although in normal telephone dialing applications the highest high group frequency (initiated by column 4) is not used

The oscillator is crystal controlled, using a standard U.S. TV crystal at a frequency of 3.579545MHz. Apart from the crystal, no external oscillator components are required. The fundamental accuracy of the generated tones is better than 0.75%, as shown in Table 1, assuming the accuracy of the crystal (normally better than 0.01%) does not impact on this figure.

When a valid key depression is detected, divide ratios are programmed into two counters, one for the high group tone and one for the low group tone. Each counter drives a 32 step weighted resistor ladder D-A converter to synthesize a sine wave of the correct frequency, at an amplitude governed by a voltage regulator. The two signals are linearly summed by an op amp which then drives the base of an open-emitter NPN transistor whose collector is connected to V_{dd}. This transistor provides sufficient current gain to drive a low impedance load in the emitter follower configuration.

Depression of a single key will activate one row and one column, thereby generating the appropriate two-tone combination. Depression of two keys in the same row or two keys in the same column will cause a single low group (row) tone or high group (column) tone to be generated, providing the Single Tone Inhibit input is either unconnected or held high If this input is connected low, no output will be generated if more than one key is depressed.

In the absence of a key depression the chip remains in its power down mode, the oscillator is disabled and the XMIT switch acts as a current source in order to power external circuitry. The MUTE output is held low as an indication of the state of the device. When a key is depressed, the chip switches to its operating mode, indicated by the MUTE output going high. The oscillator is enabled and the XMIT output goes open circuit, ceasing to source current to the external circuitry.

PIN CONFIGURATION

16 LEAD DUAL IN LINE

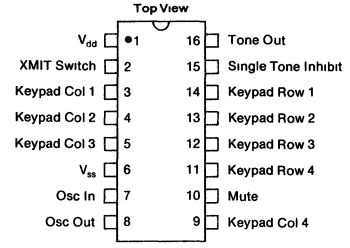


Table 1: FREQUENCIES GENERATED BY AY-5-9559

Keyboard Input	Tone Output Frequency (Hz) Standard	Actual	% Error
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0 57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

OXI-CMOS Technology
The high performance OXide Isolated silicon gate CMOS process is a state-of-the-art VLSI CMOS process capable of high speed and low power operation over a wide range of operating conditions. It is being used to manufacture a range of advanced performance telecommunications products characterized by their high reliability and ease of application.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltages on any Pin with Respect to V_{SS} ..... −0.3V to +15V
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... −25°C to +70°C

Standard Conditions (unless otherwise stated):

Operating Temperature ..... −25°C to +70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS All voltages below referred to V_{ss} = OV

Characteristic	Min	Typ	Max	Units	Conditions
Positive Supply voltage	2.5	—	10.0	V	Active
	1.5	—	10.0	V	Standby
Supply Current — active	—	—	2.0	mA	V_{dd} = 3V
— standby	—	—	30.0	µA	V_{dd} = 3V
(see Note 1) — active	—	—	16.0	mA	V_{dd} = 10V
— standby	—	—	100	µA	V_{dd} = 10V
Ambient temp. range	−25	—	+80	°C	
Tone Output voltage	110	315	495	mV RMS	V_{dd} = 3.5V, R_L = 390Ω
— single tone (Row)	325	525	660	mV RMS	V_{dd} = 5V, R_L = 390Ω
	400	575	755	mV RMS	V_{dd} = 10V; R_L = 240Ω
Column/Row tone pre-emphasis	1 0	2.0	3 0	dB	
Output signal distortion (Note 2)	—	—	7	%	
	—	—	−23	dB	
Tone output rise time	—	—	5	ms	
XMIT output voltage (high) (Standby)	1.5	—	—	V	V_{dd} = 3V; I_{ohx} = 15mA
	8.5	—	—	V	V_{dd} = 10V, I_{ohx} = 50mA
XMIT output leakage current (low) (Active)	—	—	10	µA	V_{dd} = 10V; V_{olx} = OV
MUTE output voltage (high) — no load	2.5	—	—	V	V_{dd} = 2.5V; I_{ohm} = 0.5mA
	9.5	—	—	V	V_{dd} = 10V; I_{ohm} = 0.6mA
MUTE output voltage (low) — no load	—	—	0.5	V	V_{dd} = 2.5V; I_{olm} = 0.5mA
	—	—	0.5	V	V_{dd} = 10V; I_{olm} = 2mA
Oscillator output sink current	0.2	—	—	mA	V_{dd} = 3V, V_{ol} = 0.5V
	0 8	—	—	mA	V_{dd} = 10V, V_{ol} = 0.5V
Oscillator output source current	0 1	—	—	mA	V_{dd} = 3V; V_{oh} = 2.5V
	0 4	—	—	mA	V_{dd} = 10V; V_{oh} = 9.5V
Oscillator input sink current (Standby)	25	—	—	µA	V_{il} = 0.5V
Oscillator start-up time	—	—	5	ms	V_{dd} = 10V
	—	—	4	ms	V_{dd} = 3V
Oscillator input/output capacitance	—	—	16	pF	V_{dd} = 3V
	—	—	14	pF	V_{dd} = 10V
Column input pull-up current	100	—	—	µA	V_{dd} = 3V; V_{ih} = 2.5V
	300	—	—	µA	V_{dd} = 10V; V_{ih} = 9.5V
Row input pull-down current	1 0	—	—	µA	V_{dd} = 3V, V_{il} = 1V
	1 0	—	—	µA	V_{dd} = 10V; V_{il} = 2.5V
Single tone inhibit pull-up current	1.5	—	—	µA	V_{dd} = 3V
	20	—	—	µA	V_{dd} = 10V

NOTES:
1. Active — one key selected; TONE, XMIT and MUTE outputs unloaded. Standby — no key selected; TONE, XMIT and MUTE outputs unloaded.
2. Distortion defined as the ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal, to the total power of the frequency pair.

PIN FUNCTIONS

Signal	Function
V_{dd}	Positive supply voltage
V_{ss}	Negative supply voltage
Osc In Osc Out	Input and output of a high gain amplifier designed to oscillate at 3.58MHz with the addition of an external crystal. All other necessary oscillator components are provided on chip.
Keypad Col 1 Keypad Col 2 Keypad Col 3 Keypad Col 4	Column inputs for a 4x4 matrix keyboard, single or double contact With no key depressed, active pull-up devices pull these inputs high.
Keypad Row 1 Keypad Row 2 Keypad Row 3 Keypad Row 4	Row inputs for a 4x4 matrix keyboard, single or double contact. With no key depressed, active pull-down devices pull these inputs low.
XMIT Switch	Emitter connection of an open-emitter NPN switching transistor with collector connected to V_{dd}. Functions as a current source when chip is in standby mode (no key depressed).
Mute	Output of a CMOS buffer. — Switches high when a key depression is detected, otherwise stays low.

GENERAL INSTRUMENT

Multi-Frequency Generators

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
DUAL TONE MULTI-FREQUENCY GENERATORS	Generates DTMF/tone telephone frequencies.	AY-3-9400	6-18
		AY-3-9410	6-18

Dual Tone Multi-Frequency Generators

FEATURES

- No tuning required, inherent accuracy ± 0.25%
- Uses low cost ceramic resonator
- 12 tone pairs (16 tone pairs with AY-3-9410 and choice of high group pre-emphasis with AY-3-9410)
- Total harmonic distortion less than 8% (but dependent on external filter)
- Instant generation of tone outputs
- Low voltage drop
- Low power consumption (less than 35mW)
- Good thermal and voltage stability
- Keyboard lock out inhibits output if more than one key depressed
- N-channel ion implant construction
- High group pre-emphasis fixed at 3.52dB (AY-3-9400), 3/6dB (AY-3-9410)
- Pre-emphasis can be varied by simple component adjustment.

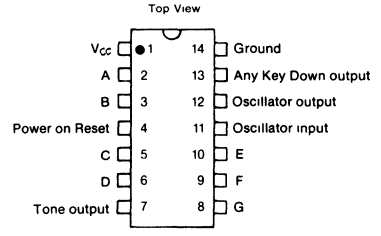
DESCRIPTION

The AY-3-9400/9410 DTMF circuits generate all the tone pairs required for multifrequency tone dialing. The tones are generated from a single ceramic controlled master oscillator, ensuring high accuracy and stability of the output frequencies and eliminating the need for any adjustments. The digitally synthesized tones give precisely controlled characteristics.

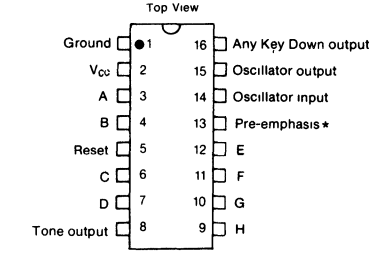
The AY-3-9400/9410 is fabricated using the ion implant N-channel low voltage process, and employs novel logic techniques to minimize power consumption and voltage drops. The circuit is suitable for operation direct from telephone line power, or it can be used with main power or battery supplies.

PIN CONFIGURATION

14 LEAD DUAL IN LINE
AY-3-9400

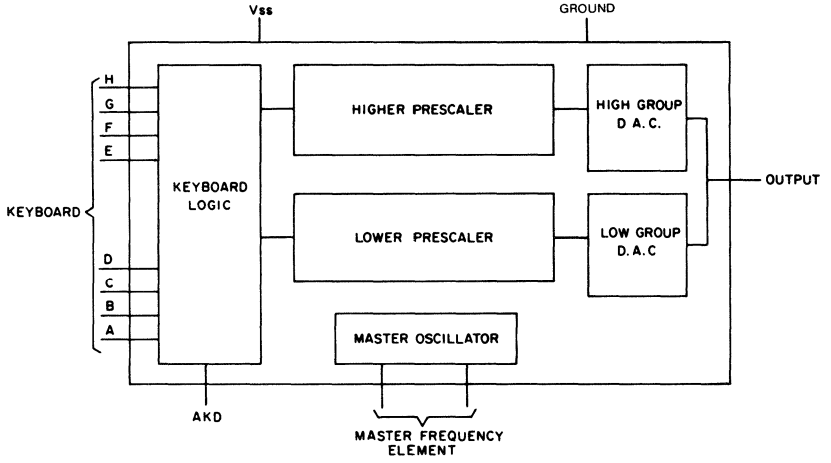


16 LEAD DUAL IN LINE
AY-3-9410



*3/6dB on AY-3-9410

BLOCK DIAGRAM



AY-3-9410

OPERATION

When a key is pressed the chip will immediately start operating, the output tones both starting from zero on the first negative half cycle. The first cycle will be of full amplitude assuming the power supply is at the correct level. If power is applied at the same time as a key is pressed, the power on reset circuit will operate, preventing spurious outputs.

When two or more keys are pressed together, one or both tones will be switched off. The tones will start from zero as soon as the extra keys have been released. When all keys are released, the tone outputs will immediately cease.

If only one key contact is made, a single tone corresponding to the closed contact will be output. The "Any Key Down" output, which requires a pull-up resistor (typ. 47K), goes to logic '0' as soon as a key depression is recognized.

The tones are output on a single pin, as a mixture of pulse width modulated, constant amplitude square waves. This output signal is constructed into resultant sine waves in the external low pass filter. The approximation chosen yields a total harmonic distortion of less than 8%.

The amplitude of the output signal is directly proportional to the V_{CC} supply voltage.

A low pass filter buffer amplifier is used to remove switching noise and interface the tones to the line. There is an option of either a low impedance or a high impedance output for interfacing to telephone lines. The low impedance circuit is shown in Fig. 1; the high impedance circuit is shown in Fig. 2.

Pre-emphasis selection for the AY-3-9410 is accomplished by connecting pin 13 to V_{CC} for 3dB high group pre-emphasis, or to ground for 6dB pre-emphasis. The circuits are otherwise identical in operation to the AY-3-9400.

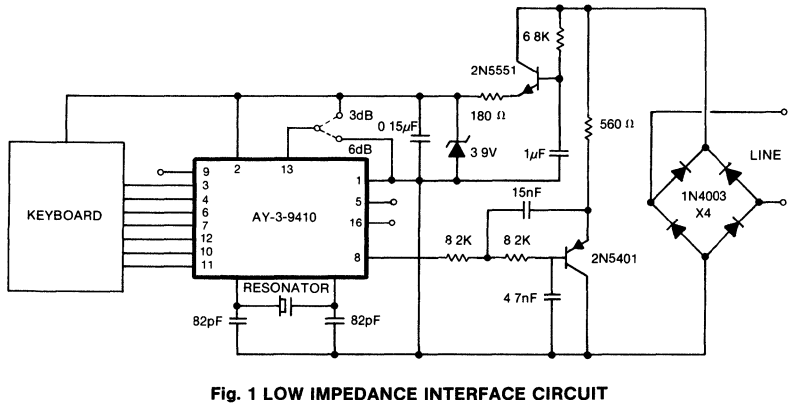


Fig. 1 LOW IMPEDANCE INTERFACE CIRCUIT

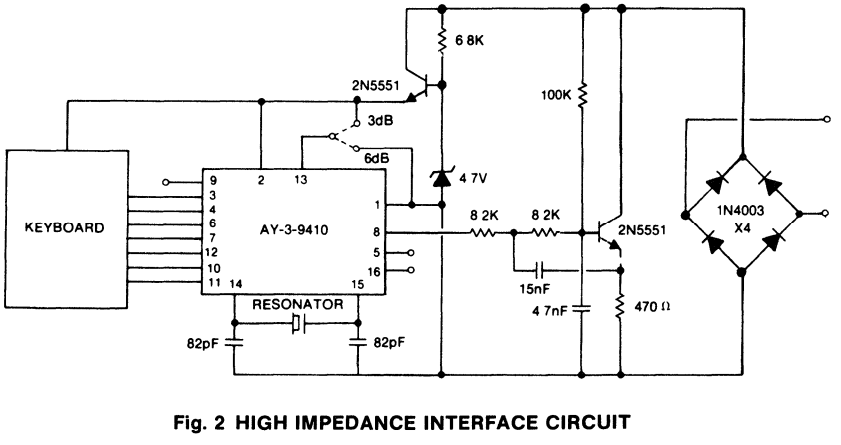


Fig. 2 HIGH IMPEDANCE INTERFACE CIRCUIT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to Ground Pin ..... +10V to −0.3V
Storage Temperature Range ..... −65°C to +150°C
Ambient Operating Temperature Range ..... −25°C to +70°C

Standard Conditions (unless otherwise noted):

V_{CC} = +3.5 to +8V
F Clock=559.7kHz
Operating Temperature (T_A) -25°C to +70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristic	Min	Typ**	Max	Units	Conditions
Input Logic '1'	+3.3	—	+8	Volts	Logic '1' activates tone
Input Logic '0'	−0.3	—	+0.4	Volts	
Input pull down resistance	20	—	100	kΩ	Resistor to ground
Input capacitance	—	—	10	pF	
Tone output Low Group	—	0.312	—	V_{peak}	V_{CC} = 4V, Note 1,
Tone output High Group	—	0.486	—	V_{peak}	V_{CC} = 4V, Note 1,
High group pre-emphasis	—	3.52	—	dB	
Output impedance	—	—	500	Ω	Note 2, Note 3
Any Key Down output					
On resistance	—	—	1	kΩ	Vout = +1V
Off Leakage	—	—	10	μA	Vout = +8V
Total Distortion	—	—	−23	dB	Note 4
Harmonic component	—	—	−30	dB	Note 4
Supply current	—	—	8	mA	V_{CC} = +3.5V
	—	—	10	mA	V_{CC} = +8V

**Typical values are at +25°C and nominal voltages.

NOTE:
1 The amplitudes of the output signals are directly related to the V_{CC} supply voltage.
2. The chip output is intended to drive a low pass filter having an input impedance of greater than 8K.
3 The output would be buffered to drive the line, the buffer can be arranged to have either a high impedance current output or a low impedance voltage output (See Fig. 1).

FREQUENCY OUTPUTS

All output frequencies are derived from a 559.7kHz master oscillator.
The output frequencies are as follows:

	Nominal Frequency Hz	Actual Frequency Hz	Error %	Key	Input Tone Pair Low Group (Hz)	Input Tone Pair High Group (Hz)	Normal Digit Representation C1
	697	695.28	−0 25	A	697	1209	1
	770	768.82	−0.15	B	697	1336	2
Low Group	852	850.61	−0.16	C	697	1477	3
	941	940.68	−0.03	D	697	1633	(A)
					770	1209	4
	1209	1211.48	+0.21	E	770	1336	5
	1336	1332.62	−0.25	F	770	1477	6
High Group	1477	1480 69	+0 25	G	770	1633	(B)
	1633	1631 78	−0 07	H	852	1209	7
					852	1336	8
					852	1477	9
					852	1633	(C)
					941	1209	*
					941	1336	0
					941	1477	#
					941	1633	(D)

GENERAL INSTRUMENT

Code Conversion

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
CODEC	Duplex Delta-Sigma/PCM converter	AY-3-9900	6-22

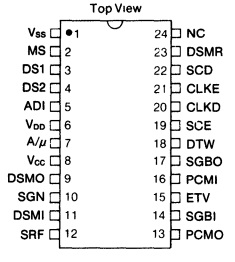
PCM Code Converter (CODEC)

FEATURES

- Converts a delta-sigma modulated pulse stream at 2048 kbit/sec into 8 ksample/sec companded PCM
- Converts 8 ksample/sec companded pcm into a delta-sigma modulated pulse stream at 2048 kbit/sec
- Enables the realization of a single channel PCM Codec using a minimum of external components
- Serial PCM input/output interface can operate in a single channel mode at 64 kbit/sec, or at up to 2048 kbit/sec for a multi-channel burst format
- All digital technique uses no on-chip precision components
- Pin-selectable A-law/μ-law companding characteristic
- Optional alternate digit inversion provided
- Direct interface with standard TTL or CMOS
- Encoder and Decoder can be clocked asynchronously (useful for PCM multiplex applications)

PIN CONFIGURATION

24 LEAD DUAL IN LINE



DESCRIPTION

The AY-3-9900 is a PCM Code Converter containing all the logic necessary to realize a high performance low cost single channel PCM Codec according to the system block schematic, Fig. 1. It contains no analog components and is fabricated with General Instruments N-Channel Ion-Implant GIANT II process, ensuring high performance with proven reliability and production history.

Together with the chip, an external delta-sigma modulator and demodulator using a small number of easily obtainable components, is required to construct the Codec, which uses delta-sigma modulation as an intermediate stage in the conversion of an analog signal into PCM and vice-versa. A pin-selectable companding characteristic which meets the CCITT recommendations G711/G712 for both. A-law and μ-law with good safety margins is included, together with a very flexible serial PCM input/output interface to allow the Codec to be readily used in a wide number of applications.

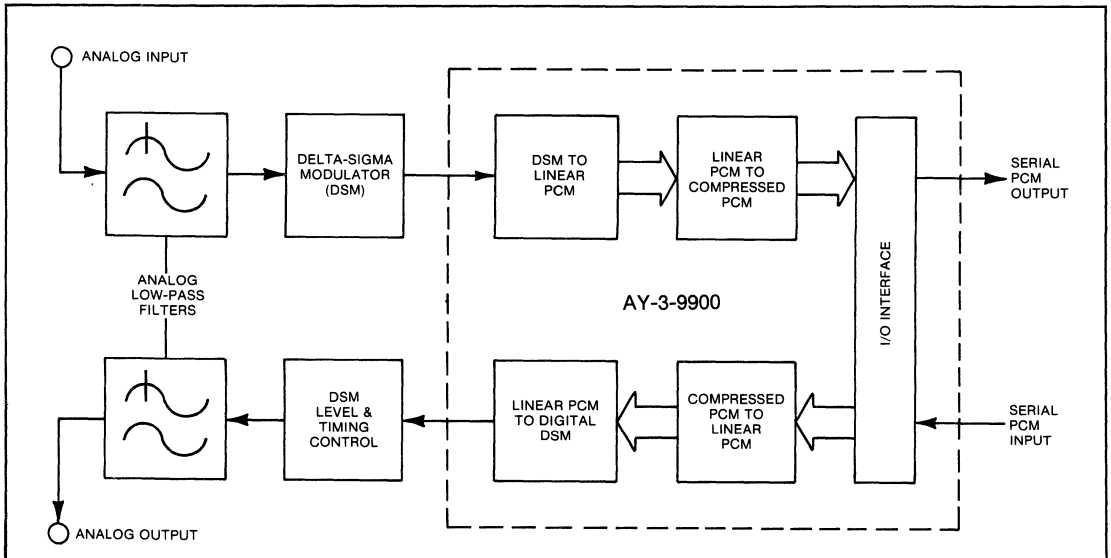


Fig.1 BLOCK DIAGRAM OF A COMPLETE CODEC

CIRCUIT DESCRIPTION

The AY-3-9900 consists of two autonomous logic systems, designated in this specification as encoder and decoder. The encoder provides the necessary logic for the digital conversion of a delta-sigma encoded pulse density signal at 2048 kbit/sec into standard 8 ksample/sec 8 bit compressed PCM codewords. The decoder provides the necessary logic for the digital conversion of standard 8 bit compressed PCM characters at 8ksample/sec into a delta-sigma encoded pulse density signal at 2048 kbit/sec. Serial PCM input/output interfaces are also provided with facilities for a data rate of 64 to 2048 kbit/sec to enable its use in either a single channel system or a standard 30 channel TDM environment. For the necessary timing information to clarify this section reference should be made to the waveform diagrams, Figs. 5a, 5b, and 5e.

The encoder logic, operating continuously on the delta-sigma input pulse train, will generate a corresponding compressed PCM codeword every 125μs; with alternate digit inversion being provided if required by appropriate use of the ADI control input. A timing vector pulse (ETV) of nominal width equal to one encoder clock period, will define the required frame start time and should be repeated every 125μs to ensure correct synchronization.

If the mode select (MS) input is connected high then the 8 bit PCM codeword will be transmitted serially at a rate of 64 kbit/sec at which speed each codeword will occupy the full 125μs frame period for transmission, with the leading edge of the first bit occurring at a time defined by the ETV pulse.

Alternatively, if the MS input is left open circuit or connected low, the serial PCM transmission will be under the control of an externally generated shift clock (SCE) which can vary in frequency from 64kHz to 2048kHz. The timing of this input function allows the insertion of a number of signalling bits into the PCM stream via the SGBI input.

With the MS input connected high, an input PCM bit stream at 64 kbit/sec will be accepted by the decoder logic under the control of internal clocks generated from the CLKD signal. Because of delays through the transmission network, normally under the control of transmission switches, the input pulse stream may be delayed in time by number of digit periods from the original pulse stream as transmitted. To allow for this, a discrete delay of 0 to 3 digit periods can be selected by the control inputs DS1 and DS2 which results in a controlled shift of decoder timing in order to re-align bit 1 in its correct position in the input register. Alternatively, if the MS input is left open circuit or connected low, the decoder input interface will be under the control of externally generated waveforms in which case it requires an input shift clock (SCD) and timing waveform (DTW) to define the time when bit 1 of the input codeword occupies its correct position in the input register. In this mode, the device will accept an input PCM stream at up to 2048 kbit/sec, with any signalling bits present in this signal being extracted via the SGBO output.

Upon receipt of a compressed PCM codeword, the decoder logic will first remove alternate digit inversions if necessary (under the control of the ADI input) after which the codeword will be linearized. A digital delta-sigma modulator will then generate a delta-sigma bit stream at 2048 kbit/sec for external decoding to produce the required analog signal.

All inputs and outputs of the AY-3-9900 are directly compatible with standard TTL (driving capacitive loads) or CMOS.

INPUT/OUTPUT FUNCTIONS

Supplies:

V_{SS}	GND
V_{CC}	+5V
V_{DD}	+9V

DC Control Signals:

MS — Mode Select — Selects between internal and external PCM I/O interface timing
Logic 0 = external
Logic 1 = internal
A resistor is connected internally between this input and V_{SS}.

ADI — Alternate-digit-inversion control – Selects ADI or no ADI
Logic 0 = no ADI
Logic 1 = ADI
A resistor is connected internally between this input and V_{SS}.

DS1, DS2 — Decoder delay select — A two bit binary word to select the required digit delay between encoder and decoder.

DS1	DS2	Digit Delay
0	0	0
0	1	1
1	0	2
1	1	3

A resistor is connected internally between each input and V_{SS}.

A/μ — Companding characteristic select-selects either A-law or μ-law
Logic 0 = A-law
Logic 1 = μ-law
A resistor is connected internally between this unput and V_{SS}.

CLOCKS & AC CONTROL SIGNALS

CLKE — Encoder main clock — 2.048MHz clock signal

CLKD — Decoder main clock — 2.048MHz clock signal

SCE — Encoder shift clock — Used to control the output of serial PCM data from the encoder (when MS=0)

SCD — Decoder shift clock — Used to control the input of serial PCM data to the decoder (when MS=0)

ETV — Encoder timing vector — A pulse defining the beginning of each frame, used to maintain encoder timing.

DTW — Decoder timing waveform — A pulse used to indicate to the decoder when the input PCM stream is in the input register (only required when external shift clocks are used).

DSMR — Delta-sigma reset — a pulse used to reset the digital delta sigma modulator during testing only Should be tied to ground during normal operation.

ENCODER OPERATIONAL INPUTS & OUTPUTS

DSMI — Delta-Sigma modulated input signal — Input to the encoder from the delta-sigma modulator.

SRF — Spectral redistribution function — 8kHz Output signal used to operate on the delta-sigma modulator to reduce low frequency quantization noise.

SGN — Sign bit output — Sign bit from the encoder, used to operate on the delta-sigma modulator for DC alignment

SGBI — Signalling bit input — facility for adding signalling bit(s) to the output PCM stream. (MS = 0).

PCMO — PCM output — Serial PCM output under the control of the encoder shift clock (MS = 0) or the encoder main clock (MS=1).

DECODER OPERATIONAL INPUTS AND OUTPUTS

PCMI — PCM input — Serial PCM input under the control of the decoder shift clock (MS = 0) or the decoder main clock (MS=1)

SGBO — Signalling bit output — Serial output for extracting signalling bit(s) from the incoming PCM stream.

DSMO — Delta-sigma modulated output signal — Output pulse stream from the decoder.

A SINGLE CHANNEL PCM CODEC

The block schematic of a single channel Codec using the AY-3-9900 is shown in Fig. 1. It consists of a band limiting low pass filter followed by a delta-sigma modulator which, by sampling at a rate of 2048kHz provides a highly over-sampled, waveform-tracking A/D conversion. The bit stream produced by this modulator at 2048 kbits, is then converted into 8 bit compressed PCM code words at the standard rate of 8 ksample/sec; which, after conversion into serial format is transmitted serially at a bit rate of 64 kbit/sec. By the application of external timing signals, the PCM output transmission rate can be increased to allow for multiplexing in a burst format, with a maximum bit rate of 2048 kbit/sec.

The PCM input interface will accept either a 64 kbit/sec bit stream or, by the application of external timing signals, a bit rate of up to 2048 kbit/sec in a burst format. This input PCM stream will be converted into a delta-sigma modulated pulse stream at 2048 kbit/sec, from which the original analog signal can be recovered by the use of a low pass filter,cutting off just above the highest signal frequency to be recovered (3.4kHz).

The transition times and voltage levels of the delta-sigma modulated pulse streams are critical to the performance of the system. The delta-sigma modulator should therefore be constructed using TTL D-Types; with the delta-sigma modulated output pulse stream from the AY-3-9900 being clocked through a similar D-type before the analog signal is recovered.

Fig. 2 shows a more detailed diagram of the necessary external components (including component tolerances) required to realize a complete PCM Codec using the AY-3-9900. The response of such a Codec is shown graphically in Figs. 3 and 4.

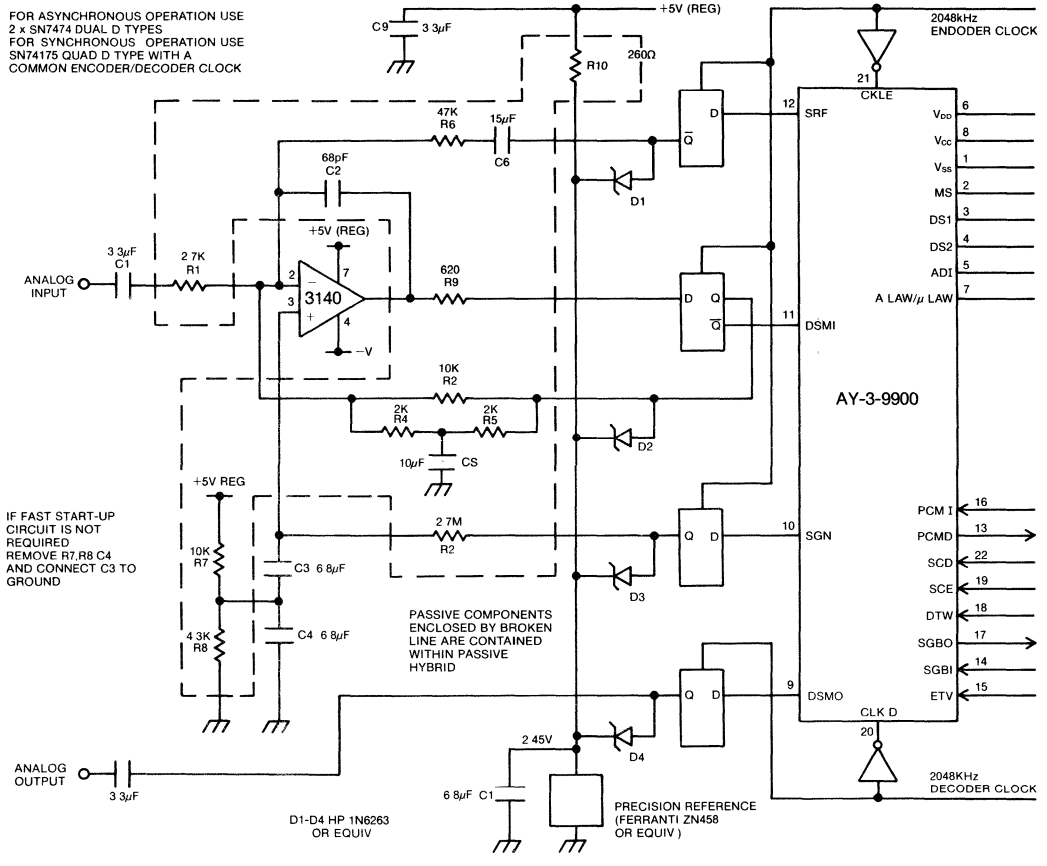
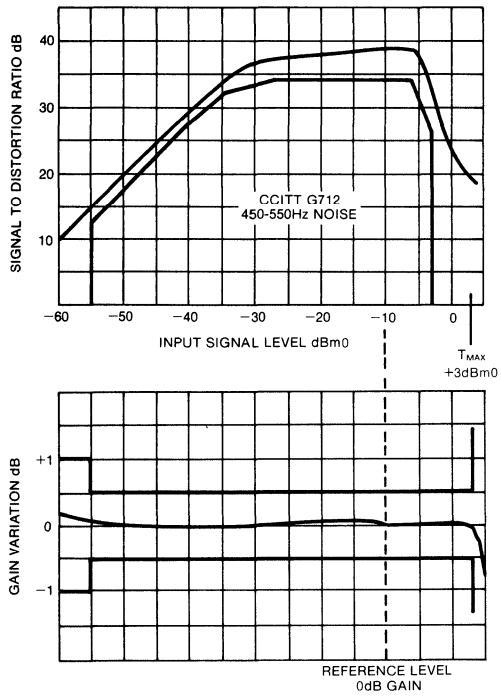


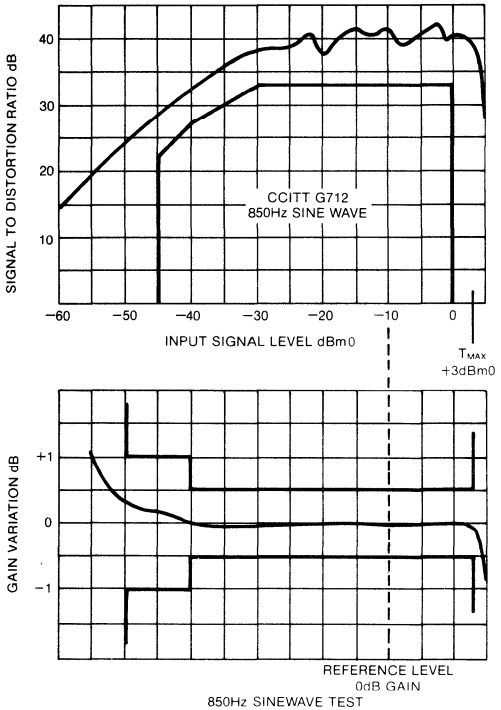
Fig.2 DETAILS OF DELTA-SIGMA MODULATOR, WITH DEMODULATOR LEVEL GENERATOR

TYPICAL PERFORMANCE MEASUREMENTS: A-LAW



450-550Hz NOISE TEST FOR LEVEL < −10dBm0
850Hz SINEWAVE TEST FOR LEVEL > −10dbm0

TYPICAL PERFORMANCE MEASUREMENTS: μ-LAW



850Hz SINEWAVE TEST

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} . . . . . +10V to −0.3V
Storage Temperature Range . . . . . −55°C to +150°C

Standard Conditions (unless otherwise noted):

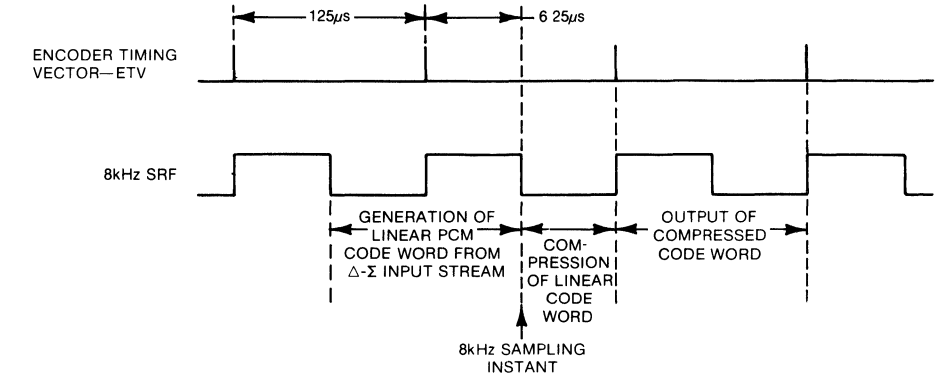
V_{SS} = 0V (substrate voltage)
V_{CC} = +5V ± 5%
V_{DD} = +8.5V to +12.5V
Operating temperature (T_A) = −25°C to +75°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

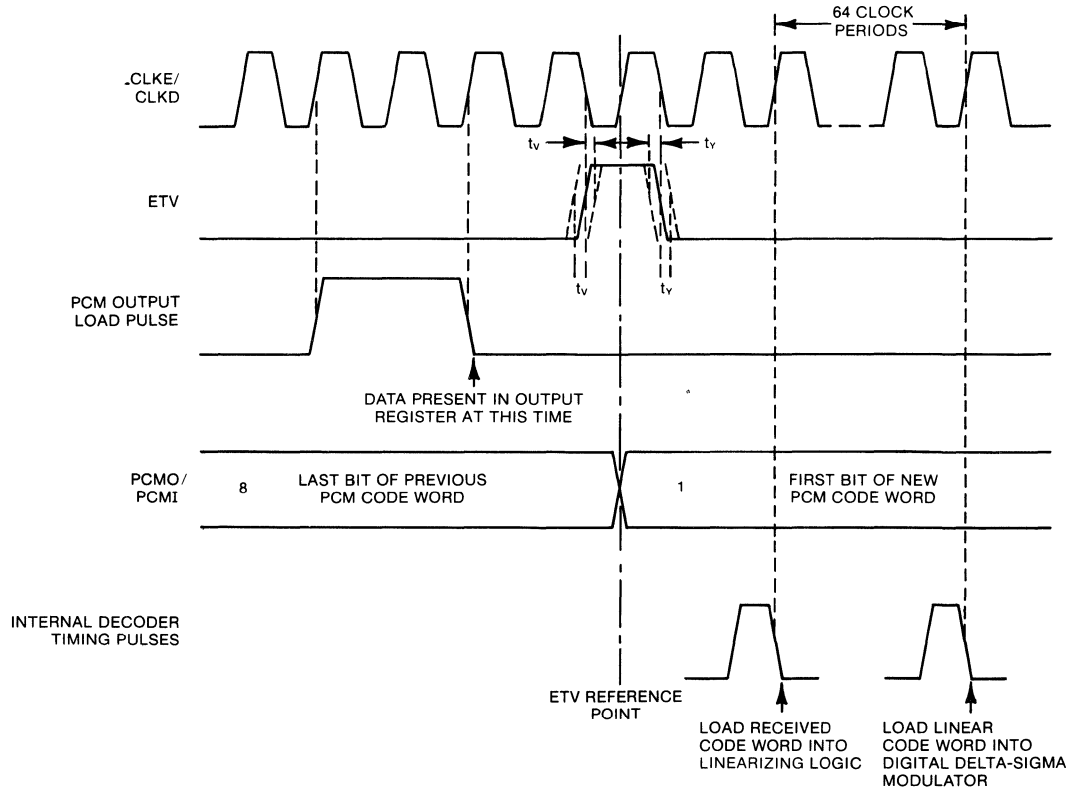
Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristic	Min.	Typ.**	Max.	Units	Conditions
DC Control Inputs					
Logic 1	4.75	5	10	V	Connect to V_{CC} or V_{DD}
Logic 0	0	–	0.4	V	Connect to V_{SS}
Pull down resistor	200	–	1000	kΩ	Resistor to V_{SS}
CLOCKS (CLKD & CLKE)					
Logic 1	3	–	10	V	
Logic 0	−0.2	0	0.4	V	
Rise & Fall Times	5	–	40	ns	0.4V-3V transition
Frequency	–	2.048	–	MHz	
Pulse Width	200	–	–	ns	Between 1.5V levels (Fig. 4c)
Input Capacitance	–	–	10	pF	
Other A.C. Control Signals					
Logic 1	3	–	10	V	
Logic 0	−0.2	0	0.4	V	
Rise & Fall times	5	–	40	ns	0.4-3V transition
SCE/SCD pulse width	200	–	–	ns	between 1.5V levels
ETV width (tvw)	–	488	–	ns	See Fig. 4c.
edge variation (tvv)	–	–	100	ns	See Fig. 4c.
DTW width	10	–	–	μs	One digit period (see Fig. 4c)
Input Capacitance	–	–	10	pF	
Operational Inputs					
Logic 1	3	–	10	V	
Logic 0	−0.2	0	0.4	V	
Rise & Fall Times	5	–	40	ns	0.4-3V transition
Pulse Width	200	–	–	ns	between 1.5V levels
Input capacitance	–	–	10	pF	
Operational Outputs					
Logic 1	4	5	5.25	V	
Logic 0	0	–	0.4		
Logic 1 source current	100	–	–	μA	at V_O = 3V
Logic 0 sink current	1.6	–	–	mA	at V_O = 0.4V
Rise & Fall times	–	–	40	ns	0.4-3V transition (driving 15pF)
PCMO delay (from SCE edge)	40	100	140	ns	between 1.5V levels
Power Consumption	–	–	450	mW	at V_{CC}=5V, V_{DD}=9V

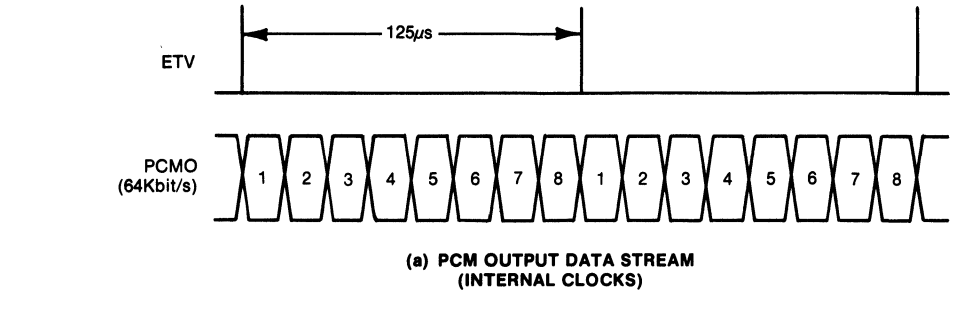
**Typical values are at +25°C and nominal voltages.



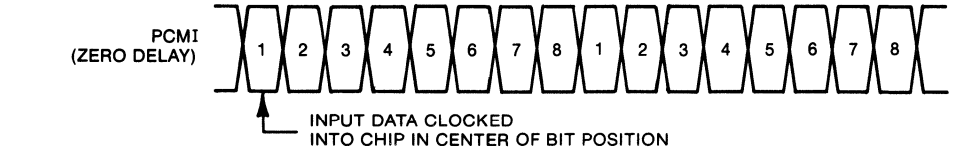
(a) TIMING OF ENCODER OPERATION

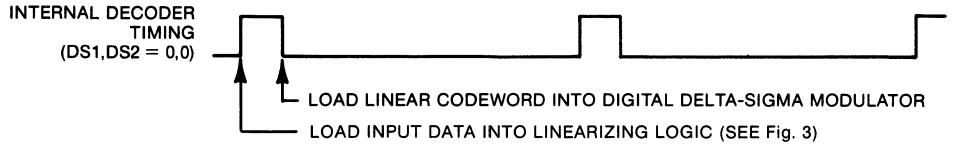


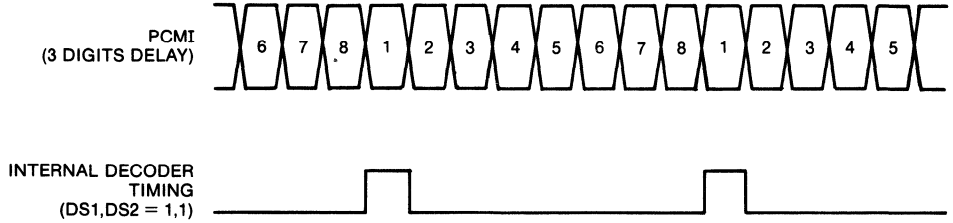
(b) DETAIL OF ETV TIMING AND INTERNAL CLOCK MODE INPUT/OUTPUT TIMING



(a) PCM OUTPUT DATA STREAM (INTERNAL CLOCKS)







(b) PCM INPUT DATA STREAM (INTERNAL CLOCKS)

GENERAL INSTRUMENT

Programmable Dialers

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
PROGRAMMABLE MICRO-COMPUTER TELEPHONE DIALERS	Single chip microcomputer pre-programmed for in-telephone applications.	TZ-2001	6-30
		TZ-2002	6-30
		TZ-2003	6-30

Programmable Microcomputer Telephone Dialers

FEATURES

- Microcomputer based dialer
- On board keyboard debounce circuitry
- Single button redial of last number dialed
- Program can be customized by single mask change

STANDARD PROGRAMMED DEVICE FEATURES

TZ-2001 — Pulse Dialer

- Outputs for 12 digit time multiplexed display
- 16 numbers by 12 digit repertory storage via 1 button recall
- Real time clock (hrs., min., sec.)
- Elapsed time timer/stopwatch
- Optional calculator interface with C-59X series

TZ-2002 — Dual Tone Dialer

- Outputs for 12 digit time MUX display
- 16 numbers by 12 digit repertory storage via 1 button recall
- Real time clock (hrs., min., sec.)
- Prompting display for simple operation

TZ-2003 — Pulse or Dual Tone Dialer

- 32 numbers by 16 digit repertory storage
- Selectable pulse dialing rates
- Selectable tone duration lengths
- Indicators for auto redial, hold and store modes

DESCRIPTION

The TZ-2000 series telephone dialers are from the General Instrument PIC series microcomputers. They are programmed to function as dialer circuits to produce either dual tone or pulse dialing functions. As with the PIC microcomputers, the TZ-2000 series are fabricated in N-channel Ion Implant technology and contain RAM, I/O parts, C.P.U. and pre-programmed ROM.

The TZ-2001 is a pulse dialer that simulates the outputs of a rotary telephone dial. It also displays and stores up to 16 12-digit telephone numbers, keeps real time displaying hours, minutes, and seconds, and can act as a stopwatch to enable the telephone user to time a call.

The TZ-2002 is a dual-tone dialer that produces the tone codes for the General Instrument AY-3-9400 Dual Tone Multifrequency Generator to generate the tonal outputs in a telephone set. It also displays and stores up to 16 12-digit telephone numbers and keeps real time displaying hours, minutes, and seconds.

The TZ-2003 is a pulse or dual tone dialer with the ability to store 32 16-digit telephone numbers. It also has selectable pulse duration rates and selectable tone duration rates plus LED function indicator drivers.

The logic timing is provided by an on-chip oscillator using an external R-C network. The use of an external 32.768kHz crystal is implemented for real time events.

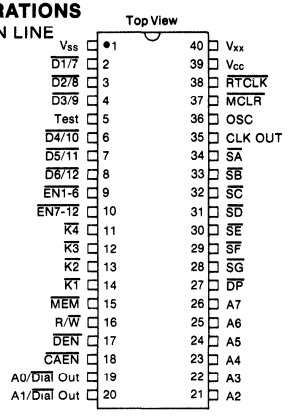
The repertory storage is achieved through the use of external RAM devices. The TZ-2001 and TZ-2002 use a 256 x 4 bit RAM device.

The Keyboards required for these devices consist of single key depression switches arranged in matrixes. The TZ-2001 and TZ-2002 devices require an 8 x 4 matrix and the TZ-2003 requires a 4 x 4 matrix.

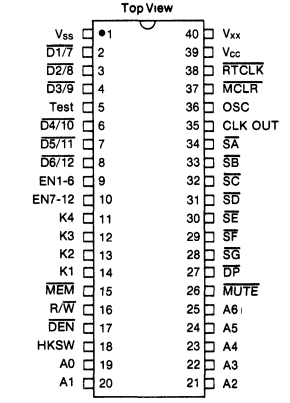
PIN CONFIGURATIONS

40 LEAD DUAL IN LINE

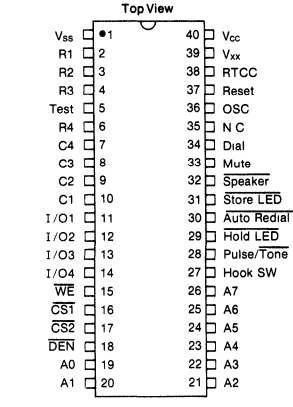
TZ-2001



TZ-2002



TZ-2003



TZ-2000 SERIES OPERATION

Dial Mode

The TZ-2001 simulates a rotary dial telephone in that the output produces a series of pulses. The TZ-2001 may be dialed by consecutive numerical entries from the keyboard after depressing the Dial Key.

The number depressed will appear in the right hand side of the display. As consecutive numbers are entered the numbers will shift left on the display. The minimum time interval between number entries is 80 msec.

The "PA" key allows a pause in access or break within the dialed sequence. The "RE" key allows a redial of the number entered. A double depression of the "DIAL" key erases the number displayed.

The TZ-2002 drives the AY-3-9400 to generate a dual tone frequency. Depression of the "DIAL" key prompts the user with the words "DIAL PLEASE" on the display.

Consecutive digit entries with a minimum of 80 nsec between entries will be displayed and dialed.

A double depression of the "DIAL" Key enables the complete number to be redialed. A display of "NONE" indicates no number in storage or an erasure of a number. The "P" Key enables the user to pause or break the dial out sequence for 2 seconds. To dial from the repertory storage, depress one of the 16 storage keys L1 to L16 after a "DIAL PLEASE" prompt display.

Store Mode

Depression of the "Store" key enables numbers to be entered into the storage memory. Both the TZ-2001 and TZ-2002 have prompting messages displayed after the store mode is entered.

The TZ-2001 prompts with a "ST" displayed and the TZ-2002 prompts with "STORE INTO" displayed after entering the "STORE" mode with the given prompting, the location must be selected by depressing one of the L1 to L16 keys. After the location is determined the TZ-2001 prompts with "STORE PLEASE" displayed. Then the telephone number can be entered as in the dial mode.

Time Mode

Depression of the "TIME" key puts the TZ-2001 and TZ-2002 circuits into the time display mode. They both indicate real time in a hours, minutes and seconds format. To set the time of day on the TZ-2001 depress the "TIME SET" key on the TZ-2002 depress the "P" key. Then enter the correct time starting with tens of hours, hours, tens of minutes then minutes. The real time starts with the fourth digit entry of the time.

The stop watch on the TZ-2001 starts with a double depression of the "TIME" key and can count up to 12 hours of elapsed time. Another depression of the "TIME" key stops the elapsed time and a final depression of the "TIME" reverts back to real time.

TZ-2003 OPERATION

The TZ-2003 has four modes of operation:

1. Dial
2. Automatic redial
3. Store
4. Hold mode

Dialing

Dialing can be operated in either the pulse or tone functions. Consecutive digit and pause entries cause the dialing to occur. Dialing may be made with either the hardset on hook or off hook. A redial of the same number can be made by depressing the redial key.

Automatic Redial

Automatic redialing of the same number consecutively at 40 sec intervals can be augmented by depressing the redial key twice.

Store

Depression of store key enters circuit into the store mode indicated by LED store indicator. Next two digits enters the storage location number from 01 to 32.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +70°C
V_{CC}, V_{XX}, all other I/O Voltages .... −0.3V to 12.0V (with Respect to V_{SS})

Standard Conditions (unless otherwise noted):

V_{CC} = +5.0V ±5%
V_{XX} = 4.75V to 10.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

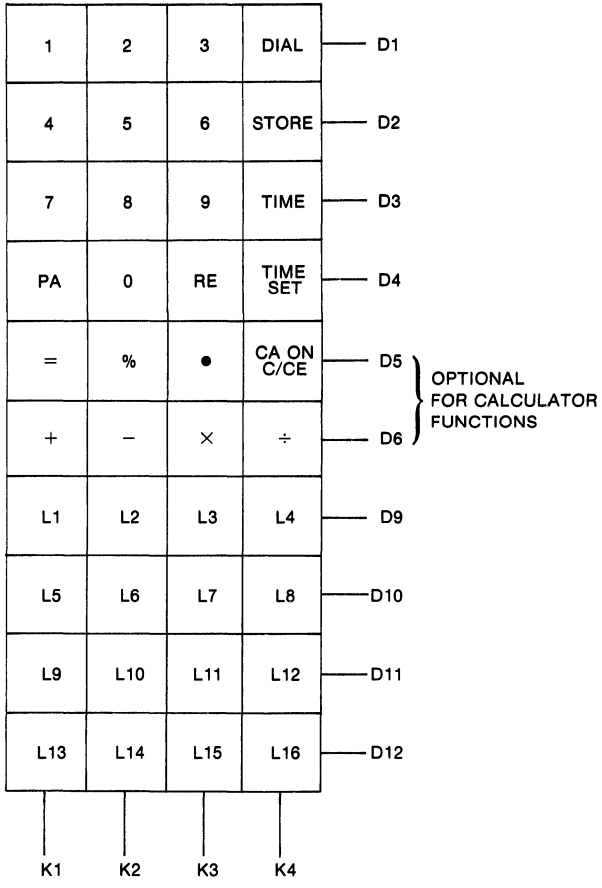
Characteristic	Sym	Min	Typ	Max	Units	Conditions
Power Supply Currents	I_{CC}	—	35	50	mA	
	I_{XX}	—	1	5	mA	
Logic Inputs						
Low	V_{IL}	0	—	0.65	V	
	V_{IH}	2.4	—	V_{CC}	V	
Logic Outputs						
Low	V_{OL}	—	—	0.45	V	V_{XX} = 5V @ I_{OL} = 1.6mA
High	V_{OH}	2 4	—	V_{CC}	V	I_{OH} = 100μA
Osc Frequency	f_{in}	0.8	—	1.0	MHz	
Rt Clk Frequency	f_{rt}	—	32.768	—	kHz	Crystal Generated
CLK OUT Frequency	—	0.25 f_{in}	—	—	—	
Key Debounce Time	t_{db}	15.6	—	23.4	ms	
Interdigit Pause	IDP	—	125	—	ms	
Tone Duration	—	—	125	—	ms	

TABLE 3: DUAL TONE FREQUENCY OUTPUTS

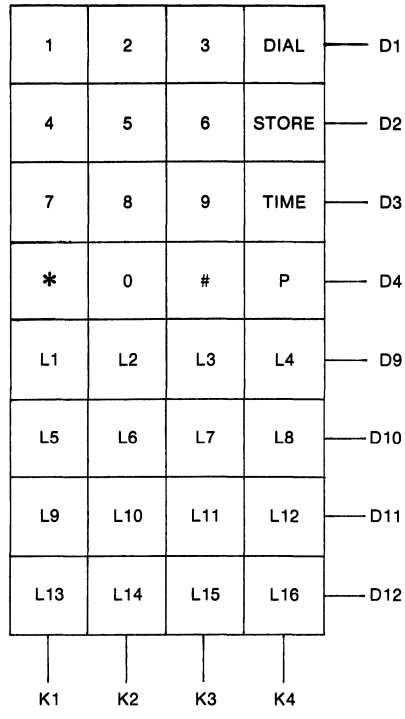
DIGIT	LOW FREQUENCY (Hz)	HIGH FREQUENCY
1	697	1209
2	697	1336
3	697	1477
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1477
0	941	1336
A (*)	941	1209
n (#)	941	1477

KEYBOARD LAYOUT

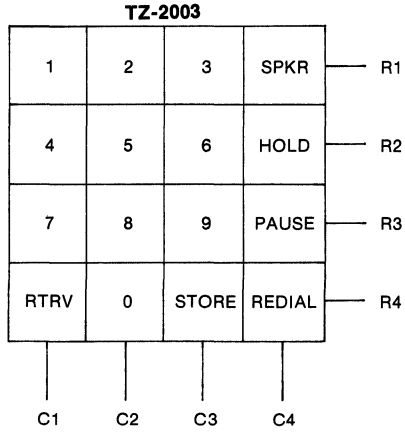
TZ-2001

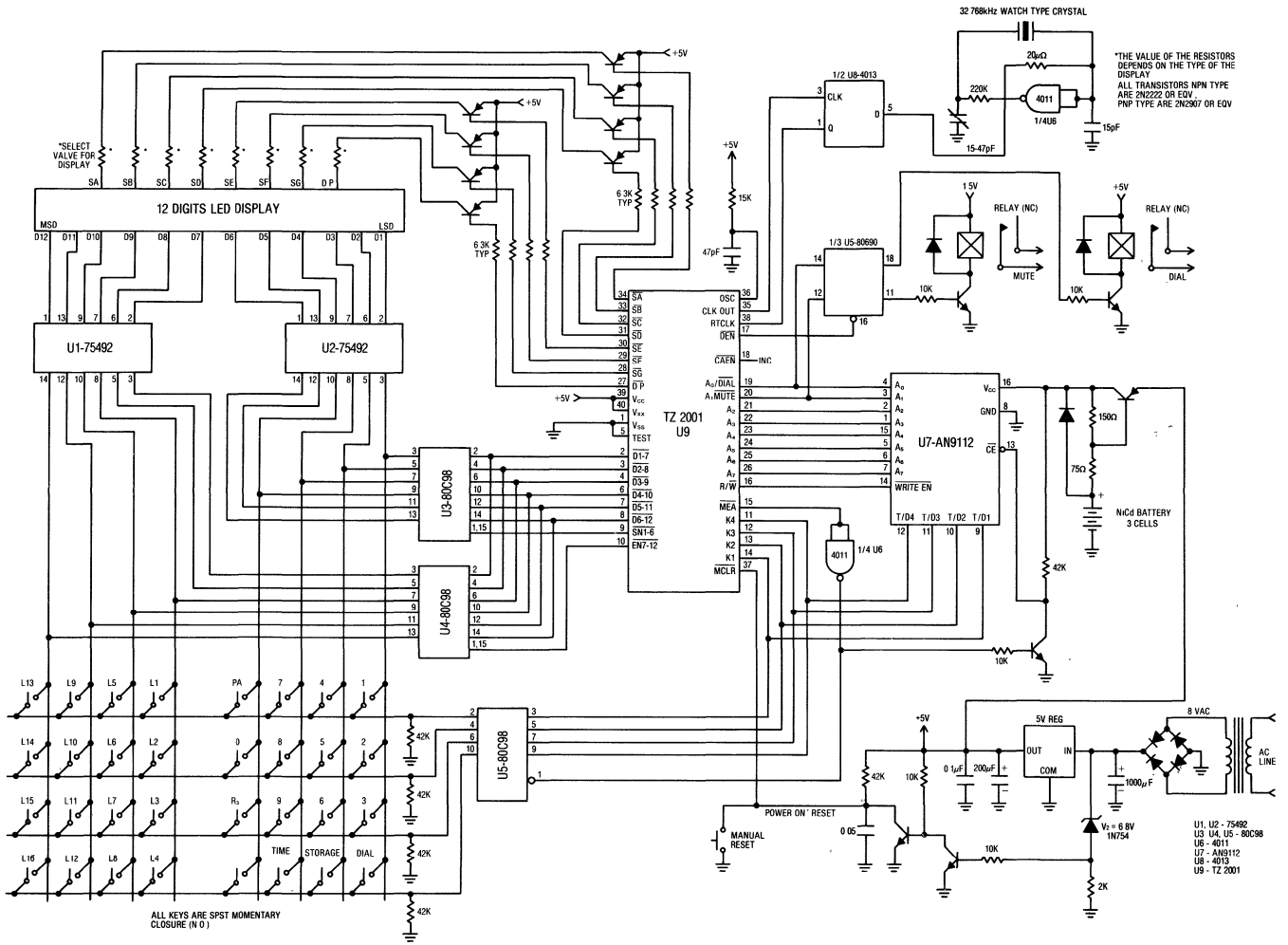


TZ-2002

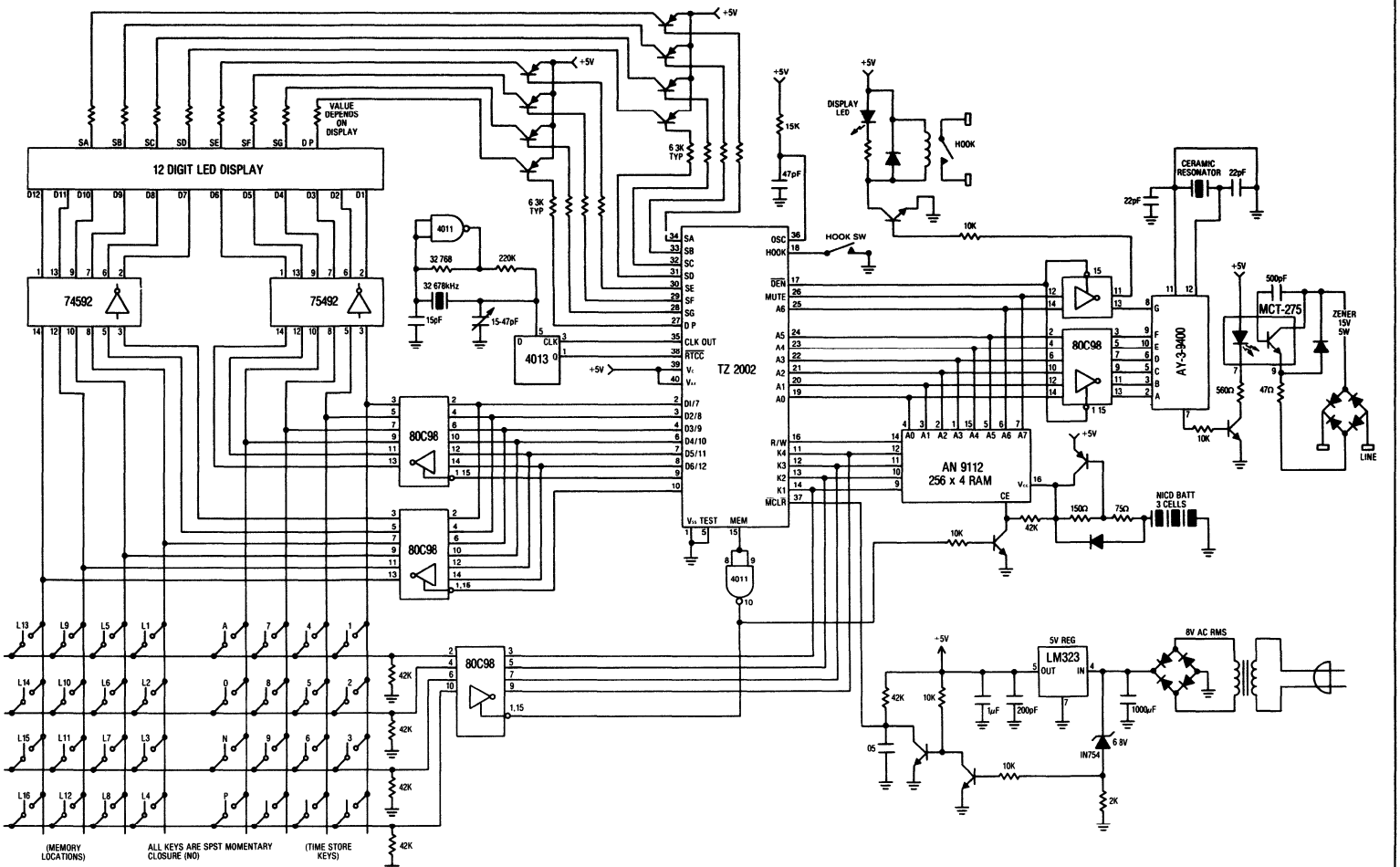


TZ-2003

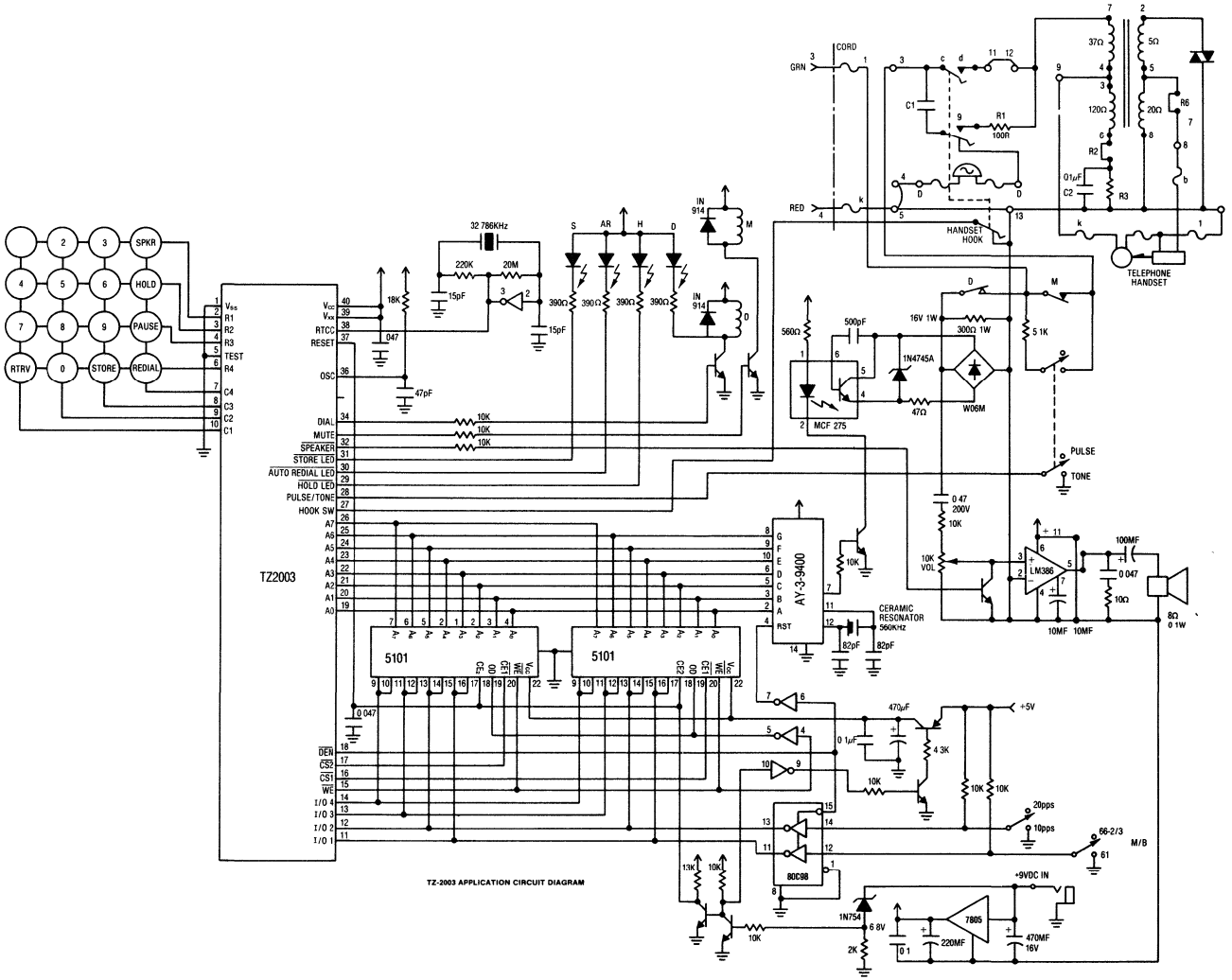




TZ-2001 APPLICATION CIRCUIT DIAGRAM (16 NUMBER REPERTORY STORAGE) WITH BATTERY BACK UP



TZ-2002 APPLICATION DIAGRAM



TZ-2003 APPLICATION CIRCUIT DIAGRAM

TZ-2003 APPLICATION CIRCUIT DIAGRAM

Data Communications 7

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			UAR/T Devices
UAR/T	Complete 5-8 bit receiver/transmitter interface.	AY-3-1015D	7-4
DUAL BAUD RATE GENERATORS	16 Frequency, UART/USRT compatible.	AY-5-8116	7-13
		AY-5-8116T	7-13
		AY-5-8136	7-13
		AY-5-8136T	7-13
			Clocks
4 DIGIT CLOCK RADIO	12/24 Hour clock, 24 hour alarm, sleep timer, battery standby.	CK3300	7-18
			Appliances
DIGITAL THERMOMETER	Digital thermometer and temperature controller.	AY-3-1270	7-32
			Remote Control
REMOTE CONTROL TRANSMITTER	256 Command PCM infrared transmitter.	AY-3-8470	7-42
REMOTE CONTROL RECEIVER	256 Command PCM infrared receiver.	AY-3-8475	7-48

UAR/T Devices

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
UAR/T	Complete 5-8 bit receiver/transmitter interface.	AY-3-1015D	7-4
DUAL BAUD RATE GENERATORS	16 Frequency, UART/USRT compatible.	AY-5-8116	7-13
		AY-5-8116T	7-13
		AY-5-8136	7-13
		AY-5-8136T	7-13

GENERAL INSTRUMENT

AY-3-1015D

UAR/T: Universal Asynchronous Receiver/Transmitter

FEATURES

- DTL and TTL compatible—no interfacing circuits required—drives one TTL load
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation
- Full Duplex Operation—can handle multiple bauds (receiving-transmitting) simultaneously
- Start Bit Verification—decreases error rate with center sampling
- Receiver center sampling of serial input; 46% distortion immunity
- High Speed Operation
- Three-State Outputs—bus structure capability
- Low Power—minimum power requirements
- Input Protected—eliminates handling problems

AY-3-1015D

- Single Supply Operation: +4.75V to +5.25V
- 1½ stop bit mode
- External reset of all registers except control bits register
- N-channel Ion Implant Process
- 0 to 25K baud
- Pull-up resistors to V_{CC} on all inputs

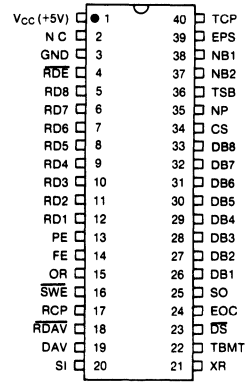
DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, 1, 1½, or 2 stop bit capability, and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

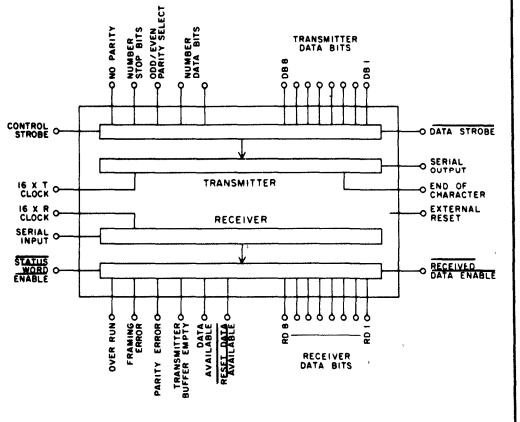
PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{CC} Power Supply (V_{CC})	+5V Supply
2	N.C.	(Not connected)
3	Ground	Ground
4	Received Data Enable ($\overline{RDE}$)	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits (RD8-RD1)	These are the 8 data output lines. Received characters are right justified. the LSB always appears on RD1 These lines have tri-state outputs; i.e., they have the normal TTL ouput characteristics when $\overline{RDE}$ is "0" and a high impedance state when $\overline{RDE}$ is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error (PE)	This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error (FE)	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run (OR)	This line goes to a logic "1" if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register Tri-state
16	Status Word Enable ($\overline{SWE}$)	A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	Reset Data Available ($\overline{RDAV}$)	A logic "0" will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data Available (DAV)	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig. 8.
20	Serial Input (SI)	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig. 7, 8.
21	External Reset (XR)	Resets all registers. Sets SO, EOC, and TBMT to a logic "1" Resets DAV, and error flags to "0". Clears input data buffer. Must be tied to logic "0" when not in use.
22	Transmitter Buffer Empty (TBMT)	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig. 14, 16.
23	Data Strobe ($\overline{DS}$)	A strobe on this line will enter the data bits into the data bits holding register Initial data transmission is initiated by the rising edge of $\overline{DS}$ Data must be stable during entire strobe.
24	End of Character (EOC)	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig. 13, 15.
25	Serial Output (SO)	This line will serially, by bit, provide the entire transmitted character It will remain at a logic "1" when no data is being transmitted.
26-33	Data Bit Inputs (DB1-DB8)	There are up to 8 data bit input lines available
34	Control Strobe (CS)	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register This line can be strobed or hard wired to a logic "1" level
35	No Parity (NP)	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication) The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0"
36	Number of Stop Bits (TSB)	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. The combined selection of 2 stop bits and 5 bits/character will produce 1½ stop bits.
37-38	Number of Bits/Character (NB2, NB1)	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits It also determines the parity that will be checked by the receiver A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} (with Respect to GND) ..... −0.3V to +16V
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... 0°C to +70°C
Lead Temperature (Soldering, 10 sec) ..... +330°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Condition (unless otherwise noted):

V_{CC} = +4.75V to +5.25V
Operating Temperature (T_A) = 0°C to +70°C

DC CHARACTERISTICS

Characteristic	Min	Typ**	Max	Units	Conditions
Input Logic Levels (AY-3-1015)					
Logic 0	0	—	0.8	Volts	
Logic 1	2.0	—	V_{CC}+0.3	Volts	Has internal pull-up resistors to V_{CC}.
Input Capacitance					
All inputs	—	—	20	pF	0 volts bias, f = 1MHz
Output Impedance					
Tri-State Outputs	1.0	—	—	MΩ	
Data Output Levels					
Logic 0	—	—	+0.4	Volts	I_{OL} = 1.6mA (sink)
Logic 1	2.4	—	—	Volts	I_{OH} = −40μA (source)—at V_{CC} = +5V
Output Capacitance	—	10	15	pF	
Short Ckt. Current	—	—	—	—	See Fig. 19
Power Supply Current					
I_{CC} at V_{CC} = +5V	—	10	15	mA	See Fig. 21

Standard Conditions (unless otherwise noted)

T_A = 25°C, Output load capacitance 50pF max.

AC CHARACTERISTICS

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Frequency	DC	—	400	kHz	at V_{CC} = +4.75V
Baud	0	—	25	kbaud	at V_{CC} = +4.75V
Pulse Width					
Clock Pulse	1.0	—	—	μs	See Fig. 5
Control Strobe	200	—	—	ns	See Fig. 11
Data Strobe	200	—	—	ns	See Fig. 10
External Reset	500	—	—	ns	See Fig. 9
Status Word Enable	500	—	—	ns	See Fig. 17
Reset Data Available	200	—	—	ns	See Fig. 18
Received Data Enable	500	—	—	ns	See Fig. 17
Set Up & Hold Time					
Input Data Bits	20	—	—	ns	See Fig. 10
Input Control Bits	20	—	—	ns	See Fig. 11
Output Propagation Delay					
TPD0	—	—	500	ns	See Fig. 17 & 20
TPD1	—	—	500	ns	See Fig. 17 & 20

**Typical values are at +70°C and nominal voltages.

TIMING DIAGRAMS

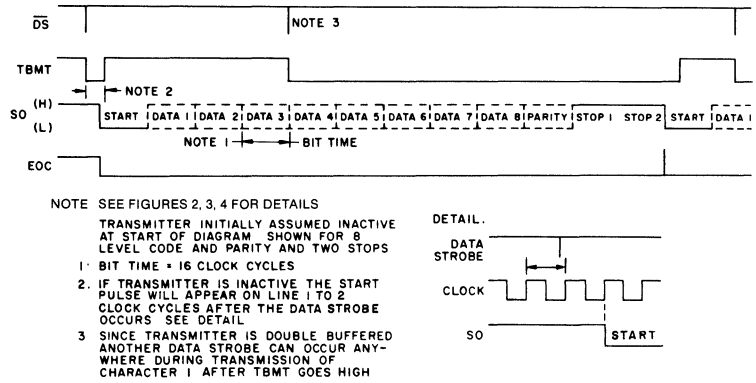


Fig. 1 UAR/T — TRANSMITTER TIMING

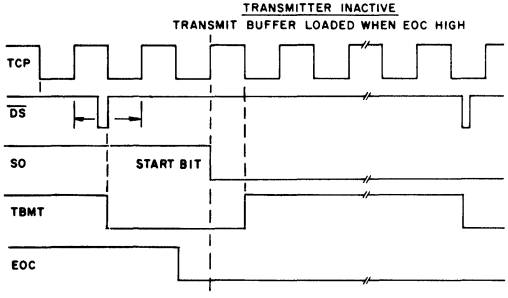


Fig. 2 TRANSMITTER AT START BIT NOT A TEST POINT

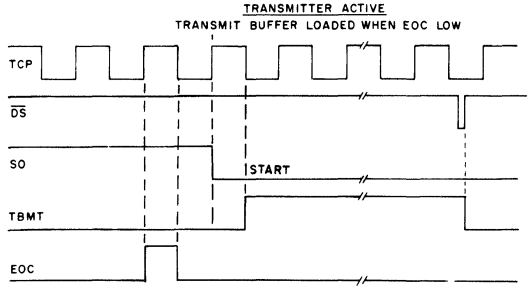


Fig. 3 TRANSMITTER AT START BIT

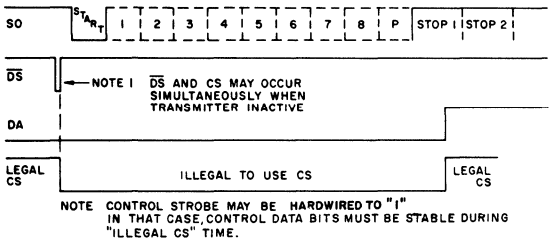


Fig. 4. ALLOWABLE POINTS TO USE CONTROL STROBE

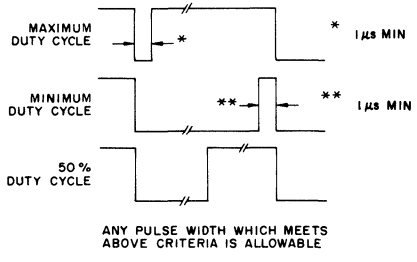
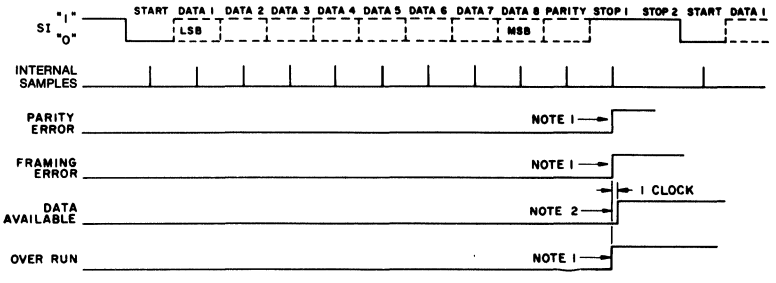


Fig. 5 ALLOWABLE TCP, RCP

TIMING DIAGRAMS



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS (SEE RECEIVER BLOCK DIAGRAM)
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED;* THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

Fig. 6 UAR/T — RECEIVER TIMING

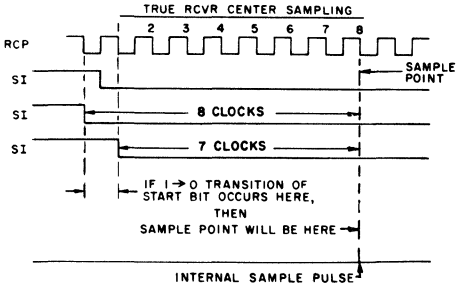


Fig. 7

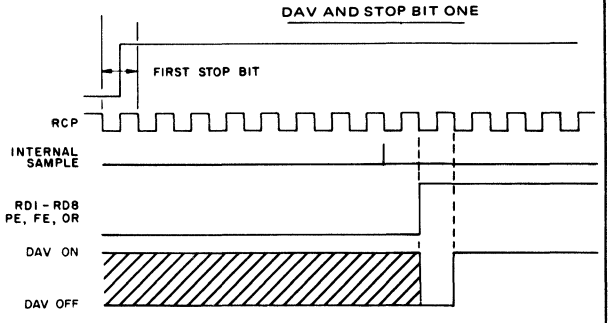
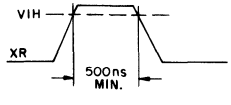


Fig. 8 RECEIVER DURING 1ST STOP BIT



WHEN NOT IN USE, XR MUST BE HELD AT GND

XR RESETS EVERY REGISTER EXCEPT THE CONTROL REGISTER. SO, TBMT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO OV

Fig. 9 XR PULSE

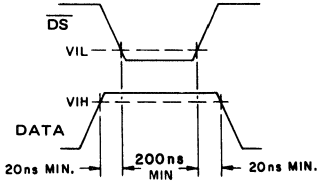
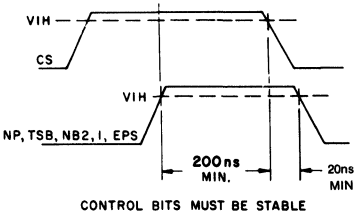
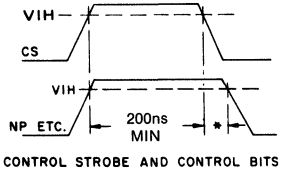


Fig. 10 $\overline{DS}$



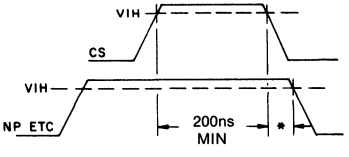
CONTROL BITS MUST BE STABLE FOR LAST 200ns OF CS.

Fig. 11a CS



CONTROL STROBE AND CONTROL BITS MUST BE 500ns MINIMUM

Fig. 11b



LEADING EDGE OF CONTROL DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

* 20ns MIN.

Fig. 12

TIMING DIAGRAMS

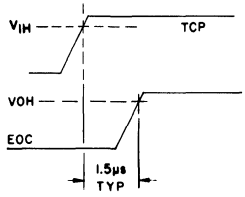


Fig. 13 EOC TURN-ON

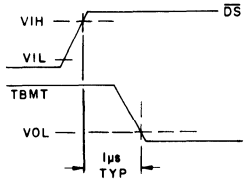


Fig. 14 TBMT TURN-OFF

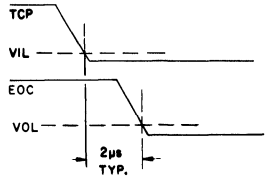


Fig. 15 EOC TURN-OFF

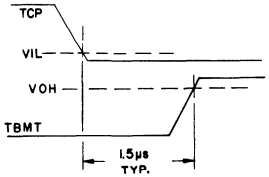


Fig. 16 TBMT TURN-ON

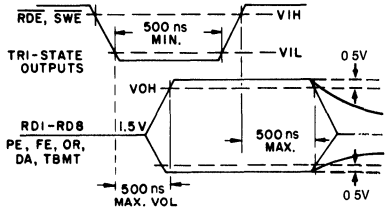


Fig. 17 RDE, SWE

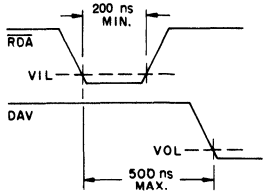


Fig. 18 RDAV

TYPICAL CHARACTERISTIC CURVES

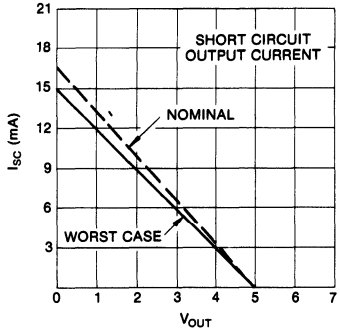


Fig. 19 SHORT CIRCUIT OUTPUT CURRENT
(only 1 output may be shorted at a time)

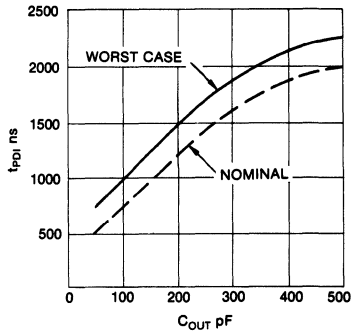


Fig. 20 RD1-RD8, PE, FE, OR, TBMT, DAV

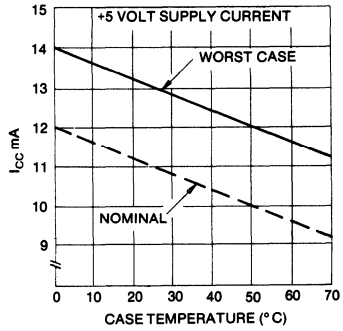


Fig. 21 +5 VOLT SUPPLY CURRENT

UAR/T: Universal Asynchronous Receiver/Transmitter

TRANSMITTER OPERATION

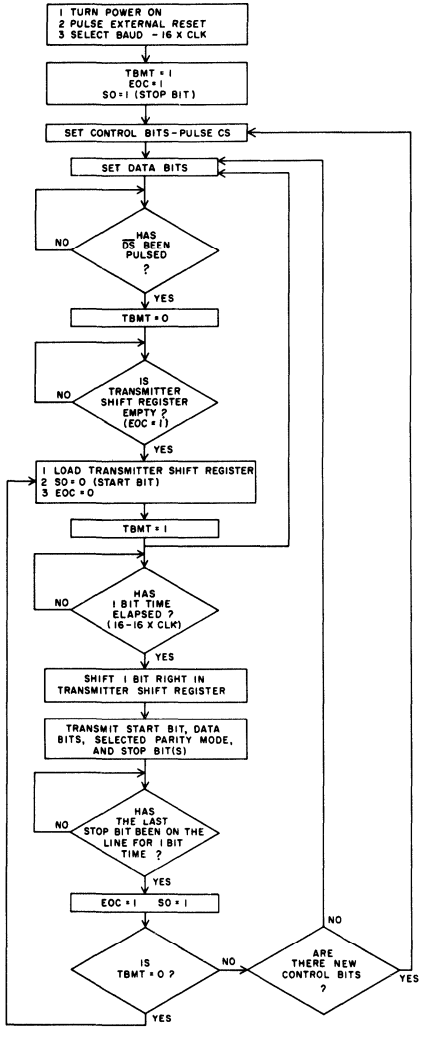


Fig. 23

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed.

RECEIVER OPERATION

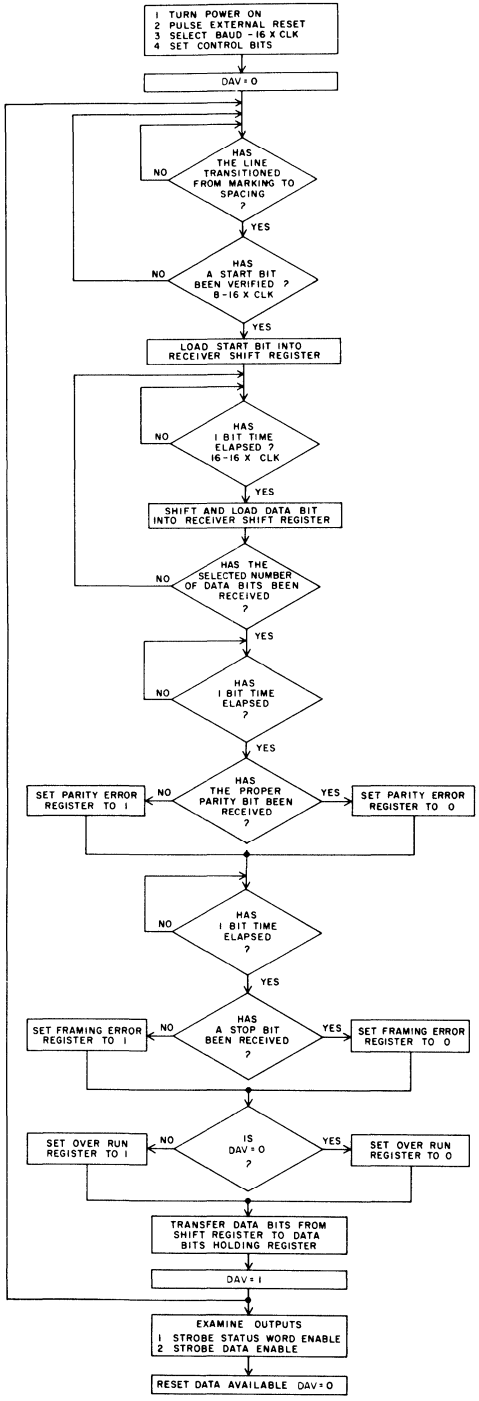


Fig. 24

Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud. The previous conditions will set data available (DAV) to a logic "1".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been the read out. If the DAV signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word hoiding register will be set to a logic "1". If the DAV signal is at a logic "0" the receiver will assume that data has been read out. After DAV goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

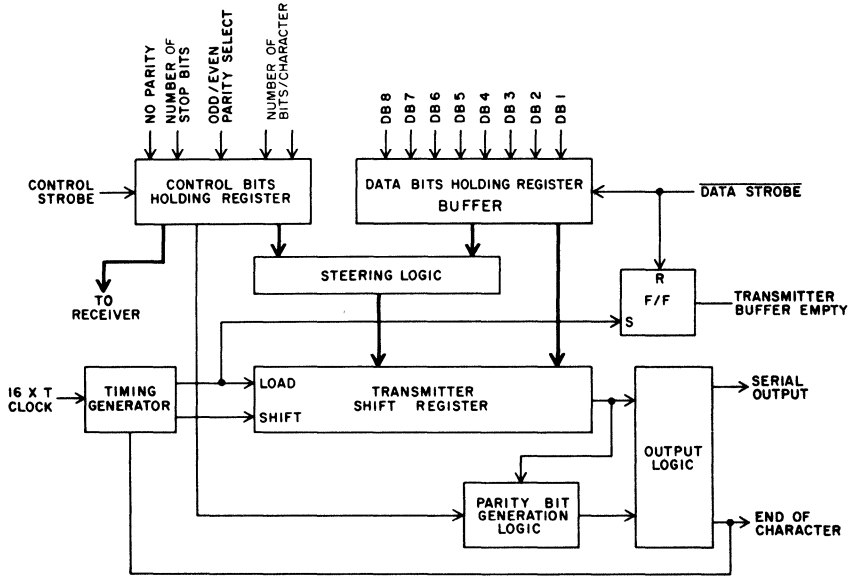


Fig. 25 TRANSMITTER BLOCK DIAGRAM

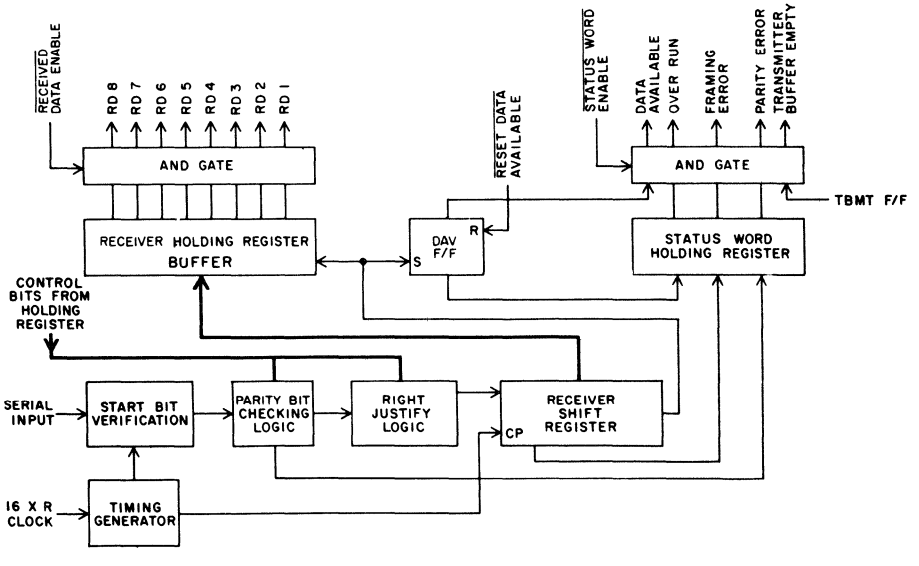


Fig. 26 RECEIVER BLOCK DIAGRAM

GENERAL INSTRUMENT

AY-5-8116/8116T
AY-5-8136/8136T

Dual Baud Rate Generator

FEATURES

- Single +5V power supply
- On-chip crystal oscillator 8116/8136 or external freq input 8116/8116T/8136/8136T
- Direct compatibility with UART/USRT
- Dual selectable 16x clock outputs
- High freq. reference output (Available only on 8136/8136T)
- Reprogrammable ROM allowing generation of non-standard frequencies
- TTL, MOS compatibility
- Pin for pin and functionally compatible with SMC's COM8116/8116T/8136/8136T
- General Instrument Advanced N-Channel Silicon Gate Process

DESCRIPTION

The General Instrument AY-5-8116/8136 Series is a very versatile family of Dual Buad Rate Generators. The AY-5-8116/8116T and AY-5-8136/8136T are pin for pin and functionally equivalent to SMC's COM8116/8116T/8136/8136T, respectively.

The AY-5-8116/8136 is designed to generate the full spectrum of 16 asynchronous/synchronous data communication frequencies for use with 16X UART/USRT devices.

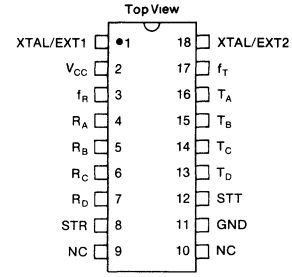
An on-chip crystal oscillator available on the 8116 and 8136 is capable of providing a master reference frequency. Alternatively, complimentary TTL level clock signals can be input to pins 1 and 18. The 8116T and 8136T are only suitable for this external TTL reference. When using TTL outputs to drive the XTAL/EXT inputs, they should not be used to drive other TTL inputs due to excessive loading which may result in a reduction of noise immunity

Dividers are used on the output of the oscillator/buffer which generate the output frequencies f_T and f_R. These dividers can divide any integer from 6 to $2^{19}+1$, inclusive When using an even divisor, the output will be square; an odd divisor will cause the output to be high longer than it is low by one clock period (f_X). The clock frequency (f_X) is used by the 8136/8136T to provide a high frequency output ($f_X/4$)

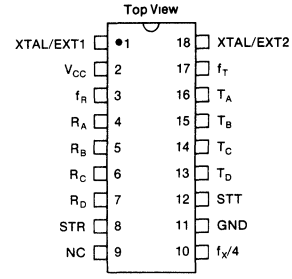
The 8116/8136 family allows generation of other frequencies with the use of its two divisor ROMs which contain 16 divisors, each 19 bits wide, allowing for up to 32 different divisors on custom parts

PIN CONFIGURATIONS

AY-5-8116/8116T



AY-5-8136/8136T



Externally strobed data latches are used to hold the divisor select bits, R_A-R_D and T_A-T_D. The strobe inputs, STR or STT, allow data to pass directly through the data latch when in the high state A new frequency is initiated within 3 5 usec of a change in any of the four divisor select bits read by the device Pull-up resistors are provided on the divisor select inputs while are not present on the strobe inputs

PIN FUNCTIONS

Pin No.	Signal	Function
1	XTAL/EXT1	Input is either one pin of the crystal package or one polarity of the external input
2	V_{cc}	Positive power supply — normally +5V.
3	f_R	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	These inputs, as shown in Table 1, select the receiver output frequency, f_R
8	STR	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register This input may be strobed or hard-wired to a high level.
9	NC	
10	NC or $f_X/4$	NC (8116/8116T), $f_X/4$ (8136/8136T)
11	GND	Ground
12	STT	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register This input may be strobed or hard-wired to a high level
13-16	T_D, T_C, T_B, T_A	These inputs, as shown in Table 1, select the transmitter output frequency, f_T.
17	f_T	This output runs at a frequency selected by the Transmitter divisor select data bits
18	XTAL/EXT2	This input is either the other pin of the crystal package or the other polarity of the external input.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Positive Voltage on any Pin, with respect to ground ..... +8 0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied. Operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed

Standard Conditions (unless otherwise noted):
$T_A = 0°C$ to 70°C, $V_{CC} = +5V \pm 5\%$

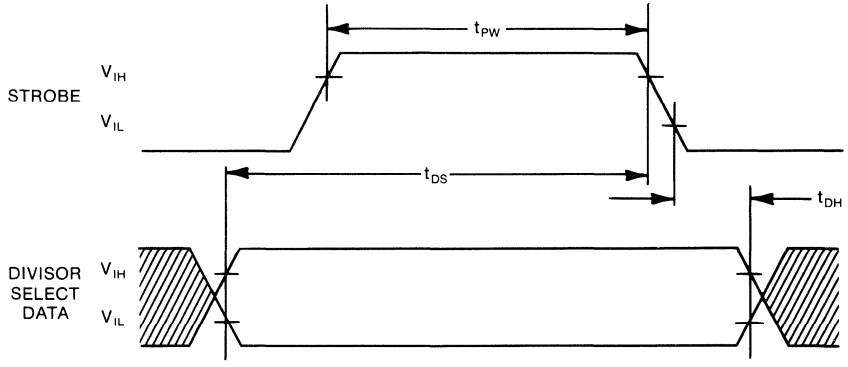
DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Unit	Conditions
INPUT VOLTAGE LEVELS						
Low Level	V_{IL}	—	—	0 8	V	
High Level	V_{IH}	2.0	—	—	V	excluding XTAL inputs
OUTPUT VOLTAGE LEVELS						
Low Level	V_{OL}	—	—	0.4	V	$I_{OL} = 1$ 6mA, for $f_x/4$,
		—	—	0.4	V	$I_{OL} = 3.2$mA, for f_R, f_T
High Level	V_{OH}	3 5	—	—	V	$I_{OH} = -100\mu A$
INPUT CURRENT						
Low-level	I_{IL}	—	—	−0 1	mA	V_{IN} = GND, R_A-R_D & T_A-T_D only
Input Capacitance All inputs		—	5	10	pF	V_{IN} = GND, excluding XTAL inputs
Power Supply Current	I_{CC}	—	—	50	mA	

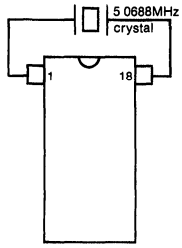
AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Unit	Conditions
Clock Frequency	f_x	0 01	—	5 1	MHz	XTAL/EXT, 50% Duty Cycle ±5%
Strobe Pulse Width	t_{PW}	150	—	DC	ns	
Input Set-up Time	t_{DS}	200	—	—	ns	
Input Hold Time	t_{DH}	50	—	—	ns	
Strobe to new Frequency Delay		—	—	3.5	μs	@f_x = 5.0 MHz

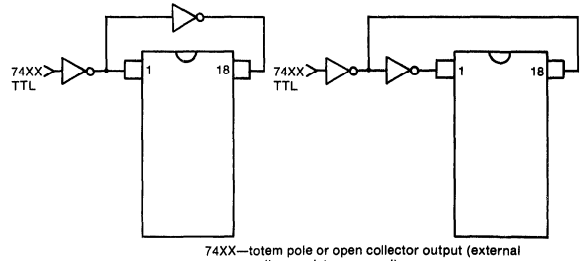
TIMING DIAGRAM



CRYSTAL OPERATION AY-5-8116/8136



EXTERNAL INPUT OPERATION AY-5-8116/8116T/8136/8136T



74XX—totem pole or open collector output (external pull-up resistor required)

BLOCK DIAGRAM: AY-5-8116/8116T/8136/8136T

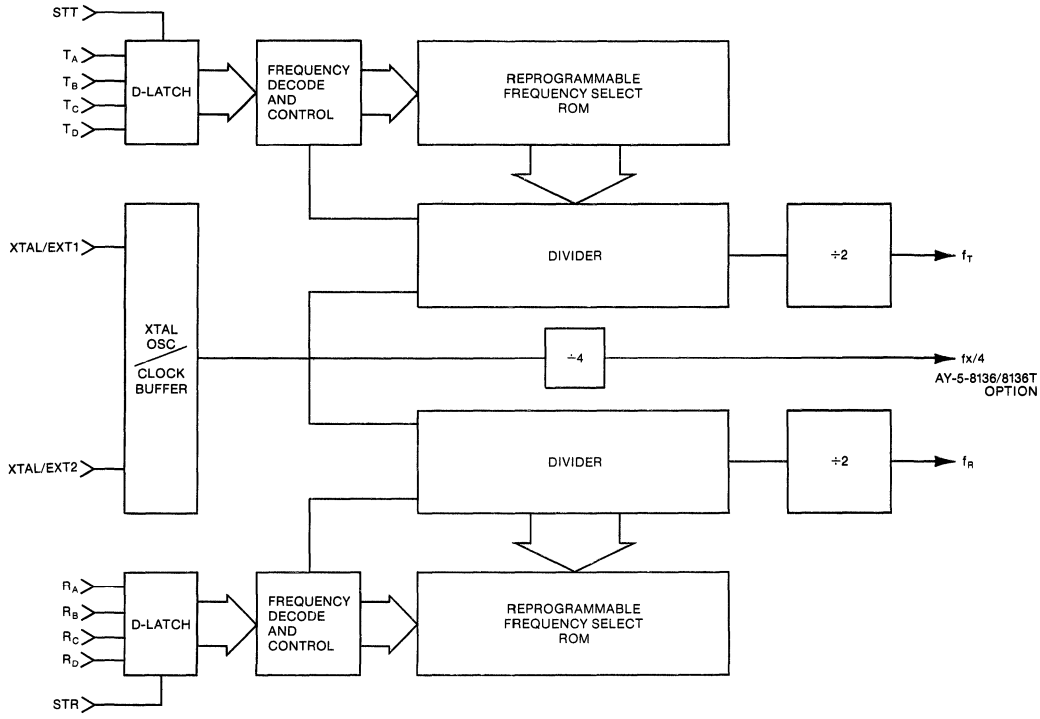


TABLE 1

Output Freq. AY-5-8116/8116T/8136/8136T

REFERENCE FREQUENCY = 5.068800MHz

Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.00	16X	0.80000	6336	50.00	0.800000	0.0000%
0001	75.00	16X	1.20000	4224	75.00	1.200000	0.0000%
0010	110.00	16X	1.76000	2880	110.00	1.760000	0.0000%
0011	134.50	16X	2.15200	2355	134.52	2.152357	0.0166%
0100	150.00	16X	2.40000	2112	150.00	2.400000	0.0000%
0101	300.00	16X	4.80000	1056	300.00	4.800000	0.0000%
0110	600.00	16X	9.60000	528	600.00	9.600000	0.0000%
0111	1200.00	16X	19.20000	264	1200.00	19.200000	0.0000%
1000	1800.00	16X	28.80000	176	1800.00	28.800000	0.0000%
1001	2000.00	16X	32.00000	158	2005.06	32.081013	0.2532%
1010	2400.00	16X	38.40000	132	2400.00	38.400000	0.0000%
1011	3600.00	16X	57.60000	88	3600.00	57.600000	0.0000%
1100	4800.00	16X	76.80000	66	4800.00	76.800000	0.0000%
1101	7200.00	16X	115.20000	44	7200.00	115.200000	0.0000%
1110	9600.00	16X	153.60000	33	9600.00	153.600000	0.0000%
1111	19200.00	16X	307.20000	16	19800.00	316.800000	3.1250%

Output Freq. AY-5-8116/8116T/8136/8136T-005

REFERENCE FREQUENCY = 4.915200MHz

Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.00	16X	0.80000	6144	50.00	0.800000	0.0000%
0001	75.00	16X	1.20000	4096	75.00	1.200000	0.0000%
0010	110.00	16X	1.76000	2793	109.93	1.758983	0.0100%
0011	134.50	16X	2.15200	2284	134.50	2.152000	0.0000%
0100	150.00	16X	2.40000	2048	150.00	2.400000	0.0000%
0101	300.00	16X	4.80000	1024	300.00	4.800000	0.0000%
0110	600.00	16X	9.60000	512	600.00	9 600000	0.0000%
0111	1200.00	16X	19.20000	256	1200.00	19.200000	0.0000%
1000	1800.00	16X	28.80000	171	1796.49	28.743859	0.1949%
1001	2000.00	16X	32.00000	154	1994.81	31.916883	0.2597%
1010	2400.00	16X	38.40000	128	2400.00	32.000000	0.0000%
1011	3600.00	16X	57.60000	85	3614.11	57.825882	0.3921%
1100	4800.00	16X	76.80000	64	4800.00	76.800000	0.0000%
1101	7200.00	16X	115.20000	43	7144.19	114.306976	0 7751%
1110	9600.00	16X	153.60000	32	9600.00	153.600000	0.0000%
1111	19200.00	16X	307.20000	16	19200.00	307.200000	0.0000%

Clocks

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
4 DIGIT CLOCK RADIO	12/24 Hour clock, 24 hour alarm, sleep timer, battery standby	CK3300	7-18

GENERAL INSTRUMENT

CK3300

4 Digit Clock Radio Circuit

FEATURES

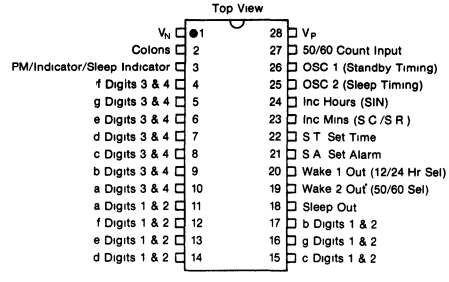
- 4 Digits plus colons
- LED direct duplex drive
- No display-IC interface components
- No radio frequency interference problems
- No external contact noise elimination circuits required
- No external line frequency noise rejection circuits required
- 12 or 24 hour display
- Leading zero suppression in 24 hour mode
- PM indication in 12 hour mode
- Alarm-snooze indicator
- 50Hz or 60Hz operation
- On-chip oscillator for standby operation with battery during line Failure
- Line power interrupt indication
- Sleep operation indicator
- Low power dissipation (under 30 mW)

CLOCK RADIO FEATURES

- Simple support electronics
- Analog sleep setting (user controlled 5 to 120 mins with 1 minute resolution). No necessity for daily adjustment
- Totally independent sleep and wake timing
- Independent volume of music during sleep and wake
- Radio sound muting during normal radio listening
- Wake to music or alarm tone
- Self-cancelling alarm after 80 minutes of wake
- 5 minute repeating snooze with radio and/or alarm
- Sleep override or sleep repeat
- Wake to alarm tone with quiet radio override (every 5 minutes) during snooze time (repeatable)
- Simple setting of time, alarm, and sleep
- Hold and synchronize capability for time setting
- Independent hours, minutes setting (carry propagation suppressed)
- 5 minute pre-alarm appliance switching
- Automatic tape recorder control (record your favorite program automatically 0-120 minutes—starting from the exact second)

PIN CONFIGURATION
28 LEAD DUAL IN LINE

Top View



DESCRIPTION

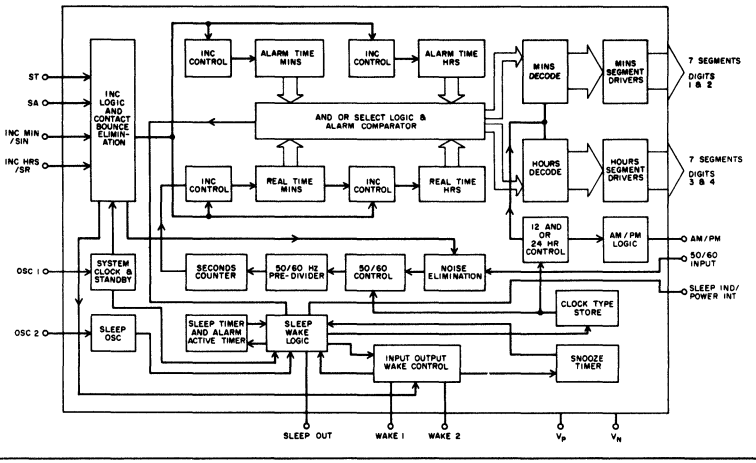
The CK3300 N-Channel MOS I.C. contains all the necessary logic, contact noise elimination circuits, control switching, segment drivers and timing circuits to implement simple-to-use, low cost, multi-featured clock radios.

Due to the extreme difficulties in eliminating R.F.I. in radios when used in conjunction with digital electronics a great deal of care has gone into the design of the L.S.I. to ensure that little or no R.F.I. problems are met by the clock radio designer. The largest R.F.I. problem in Display Driving has been solved using a novel technique—that of half-line cycle anode duplexing using the half-sine waves produced by two diodes, and ensuring that all segment data changes occur at the zero crossings of the line cycle. This technique allows brightness control to be achieved simply by resistively dividing down the line voltage with a potentiometer, or a simple two level scheme using a transformer tap.

Segment driving of the two groups is directly from the I.C. through 50 ohm switches which allow the high current peaks required of LEDs, up to one inch in size, while keeping the I.C. Power dissipation, for reliability, down to the 200 to 250 mW level.

The I.C. also contains many unique features which enable the equipment designer to put into the clock radio his company's own product image.

BLOCK DIAGRAM



PIN FUNCTIONS

V_N - (Pin 1)
Is the most negative power supply to the chip (0 volts).

Segment Drivers (Pins 2-17)
These outputs are 50Ω switches which drive the segments of common anode LED's directly. Their use and operation is as follows:

To use the CK3300 with LEDs, the LEDs must be of the COMMON ANODE TYPE, and connected in the following manner.

segment a digit 1 connected to segment a digit 2
segment b digit 1 connected to segment b digit 2
segment c digit 1 connected to segment c digit 2
segment d digit 1 connected to segment d digit 2
segment e digit 1 connected to segment e digit 2
segment f digit 1 connected to segment f digit 2
segment g digit 1 connected to segment g digit 2

segment a digit 3 connected to segment a digit 4
segment b digit 3 connected to segment b digit 4
segment c digit 3 connected to segment c digit 4
segment d digit 3 connected to segment d digit 4
segment e digit 3 connected to segment e digit 4
segment f digit 3 connected to segment f digit 4
segment g digit 3 connected to segment g digit 4

Colon 1 segment connected to colon 2 segment
PM indicator segment connected to sleep/power down indicator segment
Anode digit 1 to anode digit 3
Anode PM indicator to anode digit 4
Anode sleep indicator to anode digit 1
Anode colon upper to anode digit 3
Anode digit 2 to anode digit 4
Anode colon lower to anode digit 2

The anodes can then be selected by the application of alternate half-cycle sine waves derived from a transformer from the line. The phase of the incoming 50/60Hz count to IC will then automatically deliver the correct segment data to the display.

Anode phasing: 50/60 high = digit (1 & 3) selected
low = digit (2 & 4) selected

Sleep Output (Pin 18)
This output turns on while the sleep counter is running and is indicated as active by an indicator in the display (Pin 3). This output turns on immediately following a sleep initiate and is cancelled either by sleep time being complete, a sleep cancel, an alarm comparison taking place, or an end of snooze period. This pin is also used as an input during circuit test to speed up testing.

Wake 2 Output/50-60Hz Mode Select (Pin 19)
This output turns on at alarm compare time and stays on unless either an alarm cancel or a snooze repeat is activated.

If snooze repeat is activated this pin will go off until the next 5 minute period elapses when it will again turn on.

The snooze can be repeated indefinitely.

If the alarm is not cancelled this output will turn off 80 mins after the last snooze repeat re-triggering alarm for the next 24 hour period.

This pin is also the 50/60Hz Select input during the time at which Set Time and Set Alarm are at a logic '1' (last data on this input when either Set Time or Set Alarm changes state is stored in an internal latch).

Wake 1 Output/12 or 24 Hour Select (Pin 20)
This output turns on at alarm compare time and stays on uninterrupted until either:

a. An alarm cancel
b. 80 continuous minutes from alarm time
c. 80 continuous minutes from last snooze repeat

During the time that Set Time and Set Alarm are at a logic '1' together, this pin is the 12/24 hour select input.

The last data on this pin before a data change on Set Time or Set Alarm is stored internally in a latch, and defines 12 or 24 hour operation.

Set Alarm (Pin 21)
This pin, held at zero while Set Time is at a logic '1', enables the Increment Minutes and Increment Hours inputs to the alarm counter, such that each change of state (1→0) of the increment inputs will advance the appropriate counter by one unit.

Set Time (Pin 22)
Is identical in operation to the Set Alarm pin, but in this instance allows the counts to be entered into the time counter.

Taking both Set Time and Set Alarm to a logic '0' allows the Wake outputs to become active when the time reaches the alarm time. Returning either Set Time or Set Alarm to a logic '1' will cancel the alarm.

Increment Mins/Sleep Cancel/Snooze Repeat (Pin 23)
If Set Time or Set Alarm is at zero, this input provides one unit of increment for each logic transition from one to zero. (This input is de-bounced against switch noise). If both Set Time and Set Alarm are at a logic '1' or logic '0' and the sleep timer is running, a logic zero on this input will cancel sleep.

If both Set Time and Set Alarm are at a zero and the Wake outputs are active (i.e., post alarm time), then Wake 2 will be cancelled for a period of up to 5 mins when Pin 23 is taken to logic '0'. If this input is at zero when the alarm comparison takes place, then Wake 2 will stay off until 5 minutes have passed.

Increment Hours/Sleep Initiate (Pin 24)
If either Set Time or Set Alarm is at logic '0', this input provides one unit of increment to the required counter for each logic transition from 1 to 0. (This input is de-bounced against switch noise). If both Set Alarm and Set Time are at logic '1' or logic '0', this input will cause Sleep output to become active for the time resulting from current sleep oscillator frequency.

OSC 2 (Pin 25)
This pin produces a triangular wave oscillation depending on the value of resistance and capacitance. This oscillator is used to produce the sleep period by being gated internally with 160th of Osc 1 frequency (i.e. 50/60Hz).

Additionally connected to this pin is a low level detect circuit used with oscillator 1 for re-setting all internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used to detect that standby operation is required.

OSC 1 (Pin 26)
This pin produces a triangular wave oscillation depending on the external value of resistance and capacitance. The signal is used during normal operation to provide internally to the I C —
a. the internal timing for a series of one-shot gates
b. After division, the frequency to de-bounce other external pins via D-type latches. This frequency is further divided down to 50/60Hz and is used as the source frequency during standby operation.
Connected internally to this pin is a low level voltage detector which is used in conjunction with a low level voltage detector on Osc. 2 (pin 25) to reset all the internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used for test purposes.

50/60Hz In (Pin 27)
This input is the normal source of timing. This input drives both the internal count and the alternate half line selection of the segment outputs.
For equal brightness in the display this input must have a 1:1 mark space ratio (±20%).
There is no necessity for eliminating line noise externally when providing this input signal as an internal arrangement eliminates undesired counts.

V_P (Pin 28)
Is the most positive power supply to the chip (typically 10 volts)

FUNCTIONAL OPERATION

Pins 19, 20, 23 and 24 are dual function pins which operate as inputs or outputs dependent on the state of the Set Time and Set Alarm inputs:

S.T.	S.A.	INC MIN	INC HR	SC/ SR	SIN	Wake 1	Wake 2	50/ 60	12/ 24
1	1	-	-	*	*	-	-	*	*
1	0	*	*	-	-	-	-	-	-
0	1	*	*	-	-	-	-	-	-
0	0	-	-	*	*	*	*	-	-

*Operable - Not Operable

Set time (S.T.)	Pin 22
Set alarm (S.A.)	Pin 21
Increment minutes (inc min)	Pin 23
Increment hours (inc hrs)	Pin 24
Sleep cancel (S.C.)	Pin 23
Snooze repeat (S.R.)	Pin 23
Sleep initiate (SIN)	Pin 24
Wake 1	Pin 20
Wake 2	Pin 19
50/60Hz Select	Pin 19
12/24Hr. Select	Pin 20

Using Wake 1 Or 2—Input/Output Functions

When the Set Time (S.T.) and Set Alarm (S.A.) inputs are at logic one, the IC outputs Wake 1 and Wake 2 become inputs to two bistable gates which store the logic conditions on those pins: 50/60Hz Select on the Wake 2 pin and 12/24Hr. Select on the Wake 1 pin.

50/60Hz Select

Set Time or Set Alarm must be at zero before data on Wake 2 changes, or clock can change its 50/60 pre-divide mode. To avoid this, the following circuit is recommended:

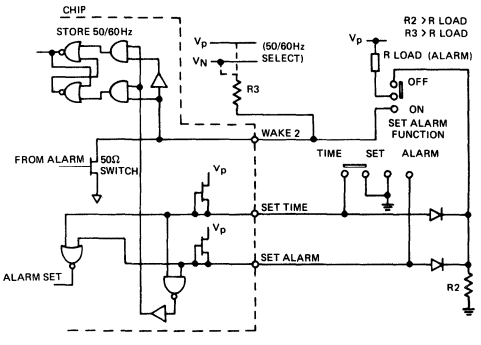


Fig. 1 SUGGESTED USE OF WAKE OUTPUTS TO ENSURE PROPER OPERATION OF INPUT/OUTPUT FUNCTION

With the Set switch in the center position the set inputs are pulled up to a logic '1' by the IC, provided the Alarm switch is in the off position. The load (R load) will pull the junction of the two diodes and R2 to a logic '1'.

The output pin Wake 2 will either be pulled up or down depending on the connection of R3.

Changing of Set switch will pull down the appropriate input and not affect other external circuit conditions.

Change of position of alarm ON-OFF switch will allow R2 to pull down both Set inputs to zero before Wake 2 output is connected to load. This ensures that the internal IC latch is disconnected from wake line before data on wake line can influence stored data in latch.

12/24 Hr. Select

For the "Wake 1 output 12-24 hour select", changing the logic polarity will immediately change the displayed time from 12 hour mode to 24 hour mode or vice versa.

e.g. 21 : 56 becomes •9 : 56
or •9 : 56 becomes 21 : 56

No leading zero is shown in 24 hour mode:

12 : 32 in 12 hour time becomes 0 : 32 in 24 hour time

(Note: 12 to 24 hour displayed time change can only be achieved when the alarm is not requested and not in set mode)

For economy of LEDs a single dot is employed which is illuminated during the PM period in 12 hour time.

Time Setting

Four input pins (S.T., S.A., Inc Hr., Inc Mins.) are provided to enable the following four functions to be provided:

a. Setting the time
b. Setting the alarm
c. Stopping the clock
d. Starting the clock

For synchronizing purposes

S.T. = 0

Allows each depression of Inc Hrs to advance hrs by one count. Clock will stop on the first inc mins and will remain stopped until ST = 1, thus allowing synchronization. The device assumes that the hours may need to be changed without affecting mins, but assumes clock is incorrect if minutes are changed, thus stopping clock and re-setting internal seconds counter to zero.

S.A. = 0

Selects alarm time and, for each depression of Inc Hours, hours are advanced one and, for each depression of Inc Mins, minutes are advanced one.

NOTE:
No carries from minutes to hours occur during setting of time or alarm

Radio Control Inputs

The inputs S.T., S.A., Inc Min, Inc Hr, serve as radio control inputs under the following conditions.

S.T. And S.A.

At zero together—alarm is requested S T and S A at logic one together—alarm not requested, but if taken to logic one during post alarm, alarm is cancelled.

S.T. and S.A. different will also cancel alarm if alarm is active

S.T.	S A.	Pre-Alarm	Post-alarm
1	1	Not required	Cancel
1	0	Not required	Cancel
0	1	Not required	Cancel
0	0	Requested	Alarm maintained for 80 mins

S.T., S.A. = 1

If S.T. and S.A. are at a logic 1 together during pre-alarm time, the following functions can be obtained using Inc Min—Inc Hrs inputs Inc Hrs input going to logic zero for at least 20 msecs will result in sleep output going to zero for the period of time set by sleep potentiometer.

At any time Inc Mins input (SC/SR) going to zero for at least 20 msecs will cancel sleep timer if sleep output is active

To reduce the number of knobs, switches, wiring etc., in the clock radio the following alternative feature is provided. If (S.C /S.R.) is wired to (SIN) a dual action is achieved, 1st depression of switch activates sleep, 2nd cancel sleep, 3rd re-activates etc. This allows features (a) if user decides he wishes radio off after he has been in bed for a few minutes, he pushes button, or (b) radio goes off automatically because sleep period has finished, but user is not asleep and would like radio to continue, so he presses button again.

S.T., S.A. = 0

In pre-alarm period the function performed when S.T., S.A. = 1 is identical. (When the alarm sounds at the requested alarm time the input (S.C./S.R.) (Inc Mins) becomes the 5 min snooze repeat input.)

At alarm, the effect of (S.C./S.R.) becoming zero for at least 20 msecs is to turn Wake 2 output off until next 5 min interval, if again depressed, Wake 2 will turn off for a further 5 mins—this sequence will go indefinitely until S.T., or S.A. or both are returned to logic '1', cancelling alarm. If inputs to the device are left unchanged for 80 mins then alarm will re-set for 24 hours.

Again to improve the radio features and simplify radio operation the tied function of (S.C./S.R.) and (SIN) on one button performs the following three functions:

Initiate sleep (SIN)
Cancel sleep (S.C.)
Snooze repeat (S.R.)

Delaying Alarm by 5 Minutes

If, when Wake 1 ouput is capacitively coupled to (S.C./S.R.) input then at alarm time Wake 1 will turn on and stay on but Wake 2 will immediately become cancelled, hence no alarm will be heard from radio until 5 minutes later; this allows an electrical appliance to be turned on 5 minutes prior to alarm sounding.

Use of Sleep Timer for Tape Recorder Control

If sleep input (SIN) in directly coupled to Wake 1 output, then a tape recorder or any electrical equipment can be turned on at alarm time using sleep output for a period of time set on sleep potentiometer.

Radio Control Outputs

There are three radio control outputs:

a. Wake 1
b. Wake 2
c. Sleep output

Function

1. Wake 1—goes at zero; i.e. is on at alarm time for a period of 80 mins or until an alarm cancel.

2. Wake 2 goes to zero at alarm time, and stays at zero until a snooze repeat is activated then it will stay off until next 5 minute point then return to zero, for a period of 80 mins unless snooze repeat is re-activated. Snooze repeat can be used indefinitely, until either a continuous 80 mins occurs or alarm is cancelled.

Note: The 5 minute period is any 5 min interval from alarm time and not 5 min from each snooze repeat.

3. Sleep output goes low after a sleep initiate for the period of time set by sleep potentiometer. (Will be overridden by Wake if sooner.)

Colon Utilization

	COLON CONDITIONS	
FUNCTION	BOTTOM	TOP
Set time	on	off
Set alarm	off	on
Stopped (Sync)	off	off
Run (alarm not requested)	1Hz	off
Run (alarm requested)	1Hz	1Hz
Snooze period	1Hz	1Hz

Sleep dot is on for sleep timer running, flashing for post line interrupt (removed from flashing by movement of S.T. or S.A. to '0')

Stand-By Operation

If a circuit is employed to change the IC power source to battery during line failure, e.g. two diodes, then if the external timing components of oscillator 1 are set to give 8kHz (nominally R = 120KΩ = 2200pF), then the IC will maintain operation to an accuracy of one part in 120, i.e., 30 secs/hr, during the failure. On return to main power the sleep indicator will flash at 1Hz to notify user that indicated time could be in error.

The standby condition is detected by the failure of oscillator 2 to oscillate, therefore oscillator 2 is connected to the line-derived power source, not the battery.

It is assumed OSC 2 input has gone to zero volts.

To remove flash condition take S.T. or S.A. momentarily to zero.

Analog Sleep Control

A second oscillator is provided on IC whose frequency can be controlled by an RC network. The oscillator is identical to oscillator one (Standby oscillator) and occupies the same silicon real estate location ensuring that process variations, temperature variations and voltage variations have as nearly as possible identical effects on frequency stability. Oscillator 1, which is set to 8KHz is divided down to 50Hz (20.0 msecs) and is used as a gating time for oscillator 2 (Sleep Timer Source). The number of gated counts is loaded in the sleep timer (capacity 160 counts) and subsequently counted up at one per minute until 160 is reached.

The range of sleep time is controlled by varying OSC 2 resistance. At 4:1 change in resistance will give variation of 160 to 40 gated pulses, this giving a sleep time of 0 to 120 minutes.

NOTE:
Minimum sleep time to ensure correct snooze operation should be a minimum of 5 minutes.

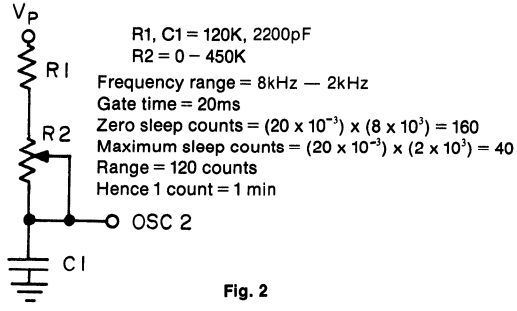


Fig. 2

To initiate the sleep timer both S.T. and S.A. must logically be the same, and INC HR/SIN must be momentarily at zero. (See later section).

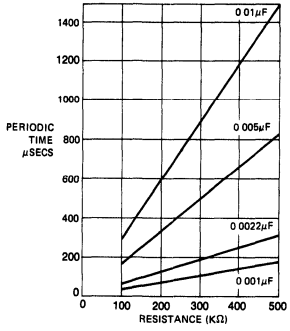


Fig. 3 OSCILLATOR CHARACTERISTICS FOR V_P = 10V

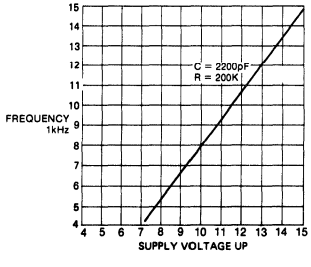


Fig. 4 OSCILLATOR CHARACTERISTICS WITH VOLTAGE

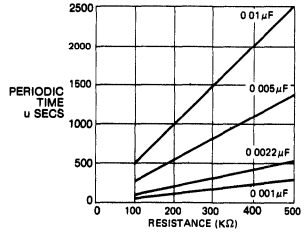


Fig. 5 OSCILLATOR CHARACTERISTICS FOR V_P = 7.5V

Operation Clock Radio Example
(showing some features and their use) - ref Figs.21 and 22.

Start-Up
Radio is connected to line for 1st time, then battery is inserted.

Assume following switch position RADIO OFF, SET TIME SWITCH = RUN

Actions
Display will illuminate and read 12:00 sleep indicator will flash at 1Hz. Set clock as indicated previously (Flashing will cease).

In 24hr mode 0:00 will illuminate with flashing sleep indicator.

Snooze Bar Action
IN RADIO OFF POSITION

1st button depression	Low volume radio (set required volume)
2nd button depression	Radio off
3rd button depression	Radio on low volume
4th button depression	Radio off

etc. . . .

IN RADIO ON POSITION
Radio comes on high volume (set wake volume required)

1st button depression	Low volume radio (mute facility)
2nd button depression	High volume
3rd button depression	as 1
4th button depression	as 2

Radio Auto
In auto, alarm is requested at "set alarm" time. If sleep is desired press button. Subsequent button pushes will have same effect as in radio "off" position.

Select Wake to Alarm Tone or Radio
Assume radio selected

At alarm time radio will come on at wake volume setting.

1st button depression	Radio will switch to low volume
2nd button depression	Radio will switch off
3rd button depression	Radio back a low volume

If after first depression radio is left untouched, radio will return to wake volume after five minutes.

If after 2nd depression radio is left untouched, radio will stay off for five minutes then return to wake volume.

This wake volume, if left, will be maintained for 80 mins unless radio is returned to radio ON or radio OFF switch position, changing switch momentarily from auto to ON or OFF and back to auto will reset alarm and re-request for same time next day. The above, repeating snooze, can be maintained indefinitely if button is pushed before 80 mins elapses.

Note: 80 mins is timed either from alarm time, if untouched, or 80 mins from last button depression

Select Wake to Alarm Tone
The alarm tone or buzzer is obtained by placing positive feedback around the audio amplifier or radio in such a manner that the desired sound can be achieved and the feedback can be stopped by open circuit one point in the network.

At alarm time buzzer will sound:

On 1st button depression	Buzzer will cease and radio will switch to low volume
2nd button depression	Radio and buzzer will be off

If after first depression radio is left untouched, radio will return to buzzer after 5 mins.

If after 2nd depression radio is left untouched, radio and buzzer will be off and at 5 mins BUZZER WILL AGAIN SOUND.

As for radio position—radio will reset after 80 mins for 24 hrs. At any time in buzzer sequencing, buzzer radio select can be changed over to radio, then the radio will alternate high-low volume with button. Cancelling in buzzer mode is identical to radio mode.

Typical Application
To combine the S.A. and S.T. functions to provide simple and rapid clock setting. It is suggested that the following is incorporated in the clock radio.

Two toothed wheels are placed over two separate sprung contacts and coupled to two concentric rotating knobs, (say 12 teeth each) along side is a three position switch labeled 'set time, run, set alarm'.

To set clock, select time or alarm and rotate Hrs knob, or mins knob, each click will result in one unit change of time, rapid rotation will result in 12 increments per revolution of knob.

The above procedure results in an easy to use system with the advantage over mechanical clocks of independent hrs and mins setting.

NOTE:
No carries from mins to hrs can occur during setting of time or alarm.

Use of Auto Tape
Fig.21 shows - the facility for automatically switching on an appliance (e.g. tape recorder) at a specific time and keeping appliance active for a period of time up to 120 mins. In this mode the wake output is made to start the sleep - timer at the wake time.

Use of 5 Min Delayed Alarm with Appliance Switching
In this mode of operation the wake 1 output is made to cancel the first alarm through the SC (inc hr) input such that radio or alarm time will only occur at the end of the first snooze period.

This result in appliance being activated at set alarm time and after 5 mins the alarm or radio will sound.

Fig.6 — shows a typical clock-radio block diagram
Fig.7 — shows the chip/display circuit.

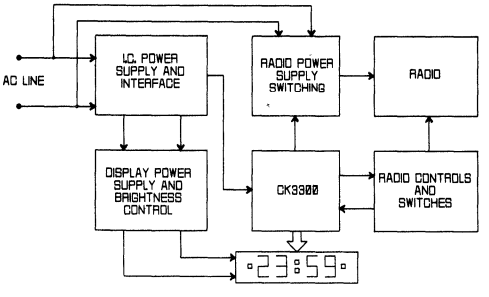


Fig. 6

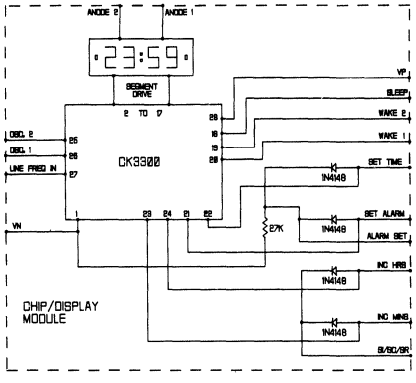


Fig. 7

Interface with a Radio

There are many possible configurations of clock radios in use today and a wide range of different radio chassis are employed in these units. It is necessary therefore that the clock radio I.C. be sufficiently flexible to allow simple interfacing to be accomplished.

The following section gives different options, features and interfacing to demonstrate some of the approaches possible with the CK3300.

Power Supply Interface

To enable any existing line operated radio chassis to be used with the minimum of changes it is suggested that the following power supply is used with the adoption of a 2nd line transformer. This will (a) reduce the need for a change at the existing transformer. (It is unlikely that the existing transformer will be capable of providing the additional power required of the display).

a. Allow the electronic clock movement to be self contained therefore, keeping the interface wiring to a minimum.

b. Allow the same electronic movement to be used with several radio chassis.

Options

1. Without battery standby facility Fig.8
2. With battery standby facility Fig.9

Display Interface and Power Source

Four options are shown

1. No brightness control Fig.10
2. Day/night brightness (two level) Fig.11
3. Manual brightness control Fig.12
4. Automatic brightness control Fig.13

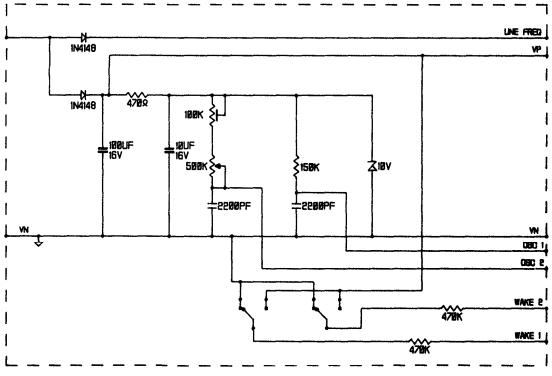


Fig. 8 POWER SUPPLY INTERFACE WITHOUT STANDBY

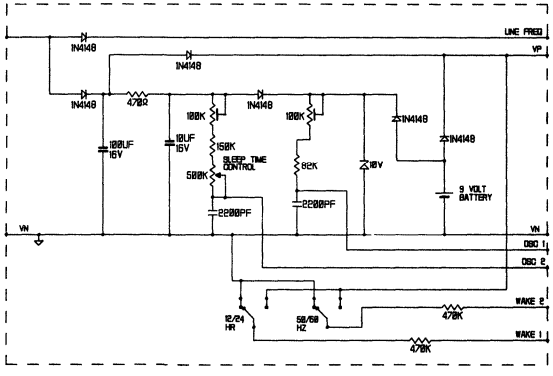


Fig.9 POWER SUPPLY INTERFACE WITH STANDBY OPTION

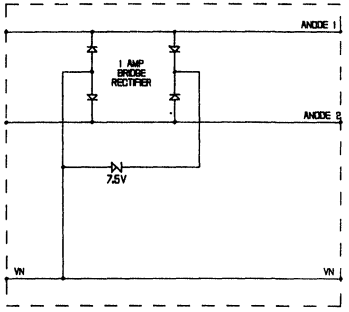


Fig.10 NO BRIGHTNESS CONTROL

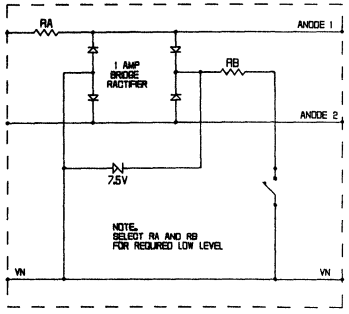


Fig.11 TWO LEVEL BRIGHTNESS CONTROL

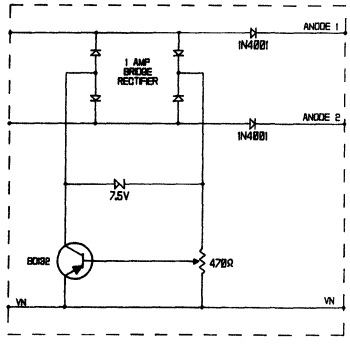


Fig.12 MANUAL BRIGHTNESS CONTROL

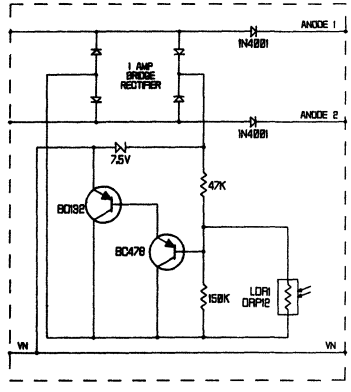


Fig.13 AUTOMATIC BRIGHTNESS CONTROL

GENERAL INSTRUMENT	CK3300

Radio Switching

Option 1 Push button operation (Fig.14)
Option 2 Rotary switch operation (Fig.15)

Radio Powering

Option 1(Fig.16A, 16B) Direct audio amplifier control (no active components)
Option 2 (Fig.17) Power supply switching using Transistor
Option 3 (Fig.18) Power supply switching using a relay

Tone Generation

Option 1 (Fig 19) Saw tooth generation independent of radio
Option 2 (Fig 20) Sine wave generation independent of radio
Option 3 (Fig.15,16B) Sine wave using the existing radio audio amplifier

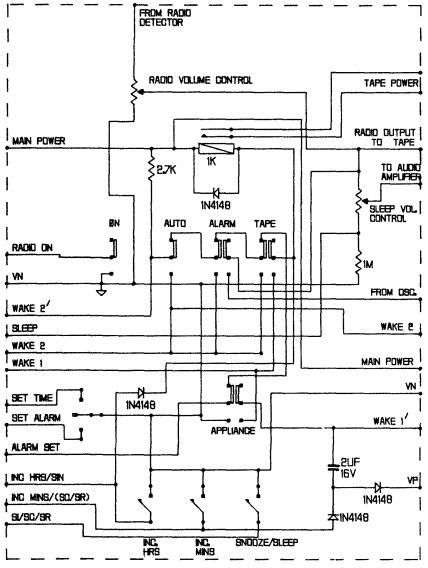


Fig.14 RADIO SWITCHING

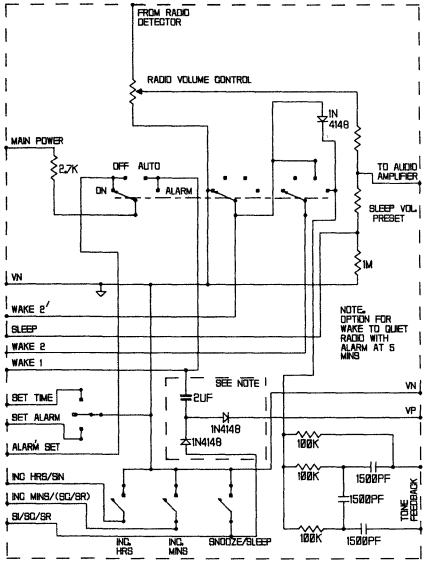


Fig. 15 RADIO SWITCHING

Additional Facilities

1. Automatic tape recording (Fig.21)
2. Appliance switching with delayed alarm (Fig.21)
3. Wake to normal radio with 5 minute alarm over-ride (Fig.21)
4. Wake to quiet radio with 5 minute alarm over-ride (Figs. 21 and/or 22)
5. Ratio muting during normal radio listening (Figs.21 and /or 22)

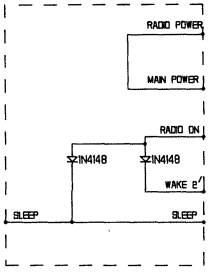


Fig. 16a RADIO SWITCHING BY BIAS CHANGE

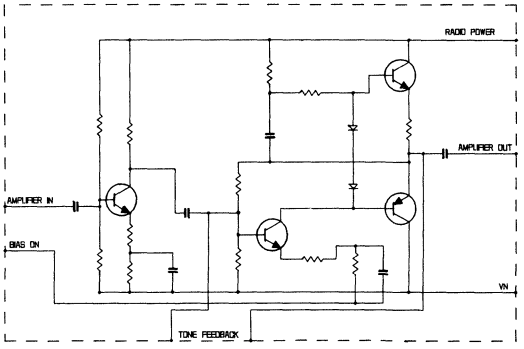


Fig. 16b TYPICAL TRANSFORMERLESS AUDIO AMPLIFIER

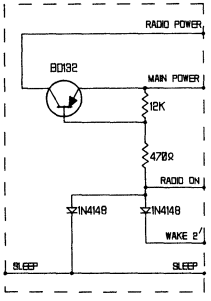


Fig.17 RADIO POWER SWITCHED BY TRANSISTOR

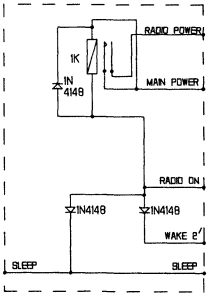


Fig.18 RADIO POWER SWITCHED BY RELAY

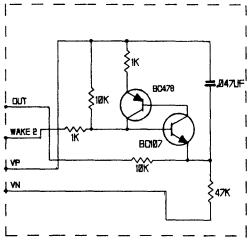


Fig.19 SAW TOOTH OSC

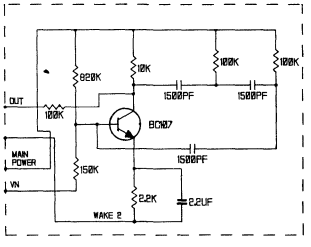


Fig. 20 SINE-WAVE OSC

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage any Pin with Respect to V_n ..... +20V
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −20°C to +70°C
Lead Temperature (Soldering 10 sec) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

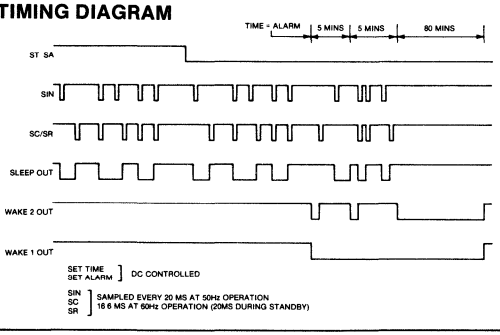
Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristic	Min	Typ**	Max	Units	Conditions
Power Supply Voltage	7	10	—	Volts	V_n = 0V
Supply Current	—	2	—	mA	
50/60Hz Input					
Frequency (must be identical to anodes)	0	50/60	50,000	Hz	V_p = 10V
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Inputs (Excl Oscillators)					
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Segments Out (on)	—	30	—	mA	V_{OUT} = 1.5V
(off)	—	10	—	μA	
Wake 1, 2, Sleep Out (on)	—	30	—	mA	V_{OUT} = 1.5V
(off)	—	10	—	μA	
Wake 1, 2 (As Inputs)					
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Oscillators 1 and 2					
Hi level	—	5.5	—	Volts	Free run
Lo level	—	3.5	—	Volts	
Reset Level	—	—	0.7	Volts	

Unless specified otherwise, characteristics are defined with V_p = 10V at T_A = +25°C.
**Typical values are at +25°C and nominal voltages.

NOTES:
1. Under no circumstances during IC operation must any pin either input or output be taken to a voltage more negative than V_n or IC malfunction will occur.
2. No input or output must be taken to a positive voltage greater than 20 volts or permanent damage can result.
3. No output must be allowed to dissipate a continuous power in excess of 100mW.
4. Total chip continuous power dissipation must not exceed 500mW.
5. The total current being returned to V_n through all device pins must not exceed 1 amp

TIMING DIAGRAM



Input and Output Characteristics

INPUTS
S.A.
S.T.
INC HR (SIN)
INC MIN (SC/SR)
} Active pull up's to V_p } 250KΩ
Operate level logic '0'

50/60Hz count input, active pull down
For correct operation duty cycle of 50/60Hz must be 1:1 ± 20%

OUTPUTS
Normally open circuit
Operate "on" (low impedance typically 50Ω)

INPUTS
Wake 1—as input '1' = 12hr '0' = 24hr
Wake 2—as input '1' = 60Hz '0' = 50Hz

CLOCK INPUT NOISE ELIMINATION TIMING
50/60Hz—strobed every 4ms internally for less than 1μs

Testing I.C. Facilities

1. Master reset: This can be activated by pulling OSC1 (Pin 26) and OSC 2 (Pin 25) to zero volts together.
2 Internal debounce and predivider logic may be bypassed if OSC 1 is taken to zero volts while OSC 2 is left running.
a. Under this condition Inc Hrs and Inc Mins pins are not debounced to allow fast incrementing for test purposes.
b Also in this mode the 50/60Hz input pin is directed straight to the main counters under control of the sleep pin. If Sleep pin at '0'—50/60Hz input clocks 120 minute sleep counter, and with Sleep at '1' it clocks the main minutes count by passing the debounce and divide by 50/60 counter Under this condition it also clocks the 5 minute snooze counter.

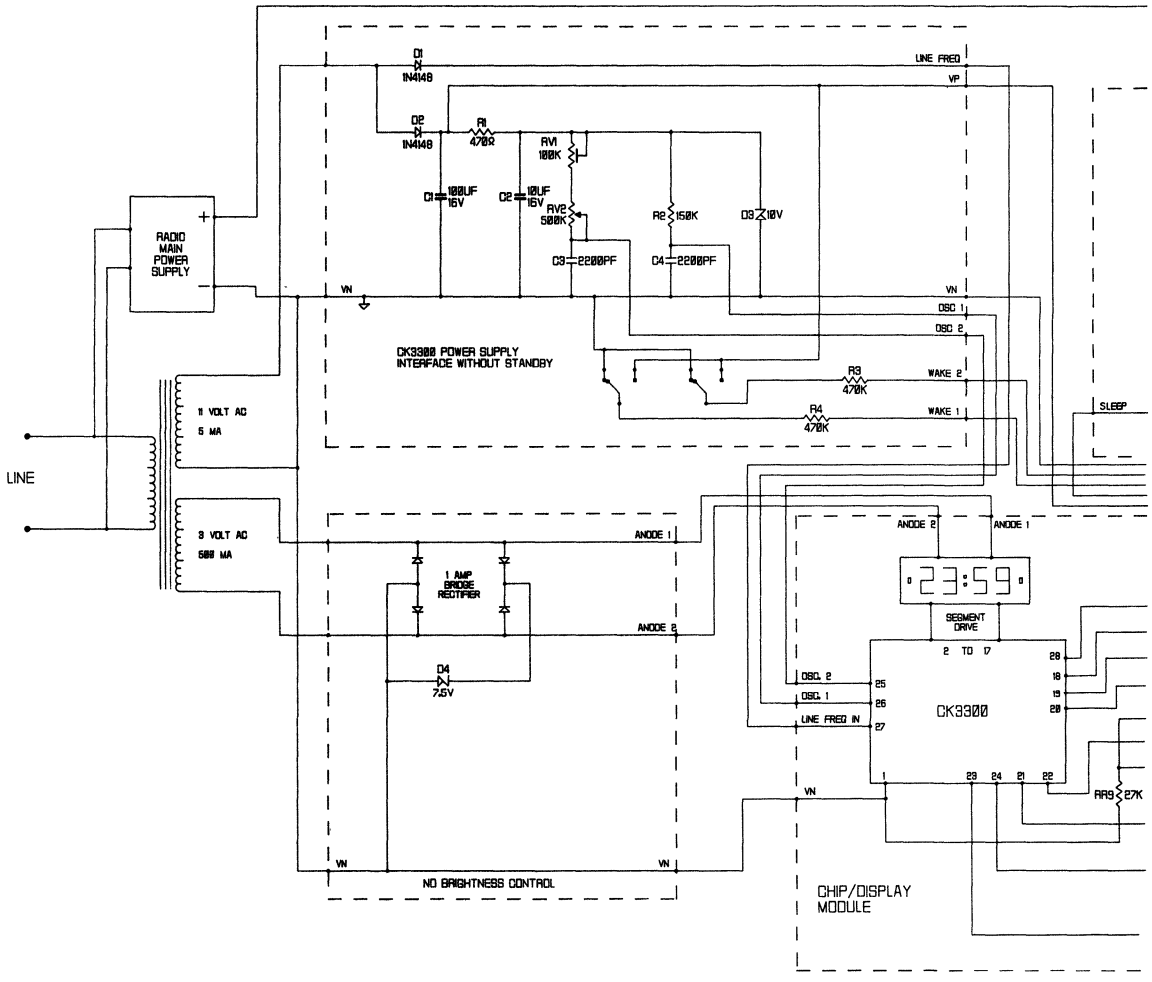


Fig. 21 (a) TYPICAL "BASIC" CLOCK RADIO CIRCUITRY

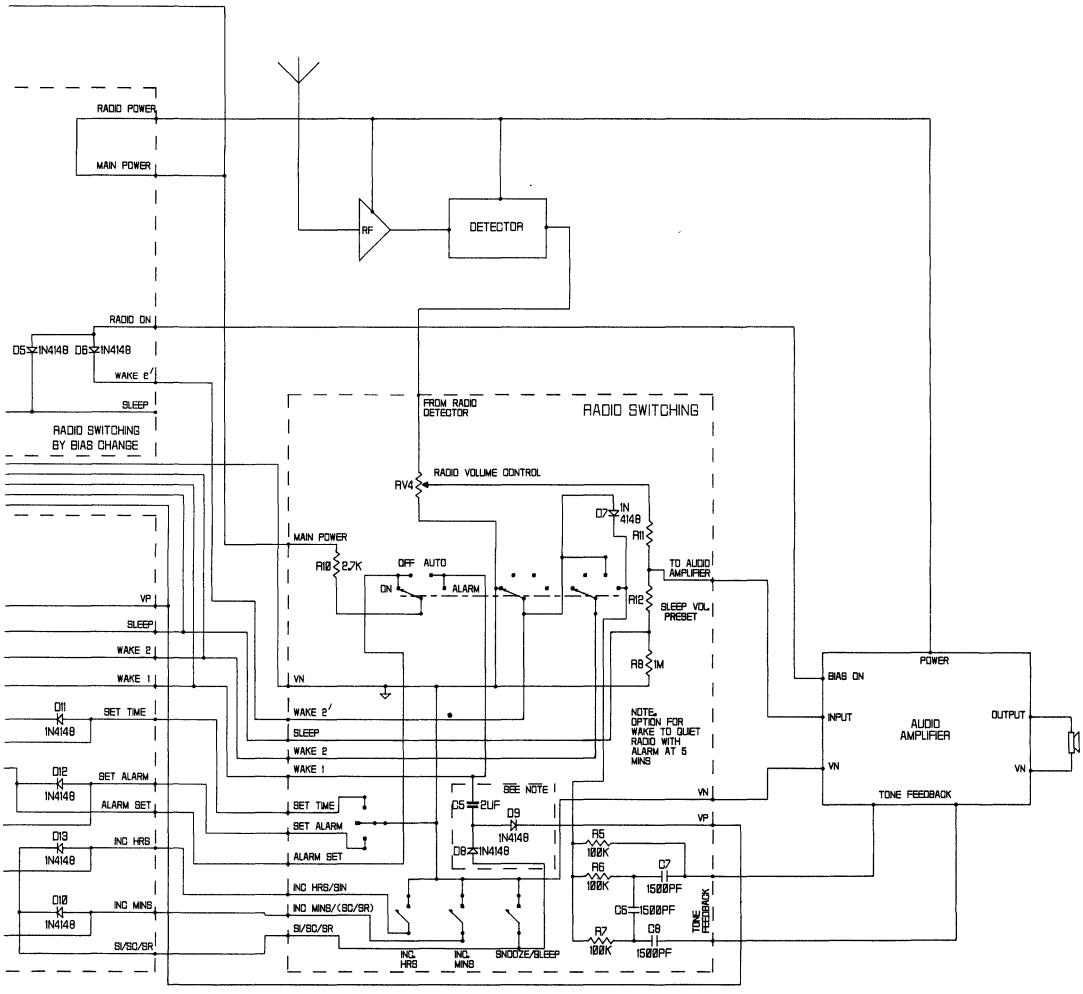


Fig. 21 (b) TYPICAL "BASIC" CLOCK RADIO CIRCUITRY

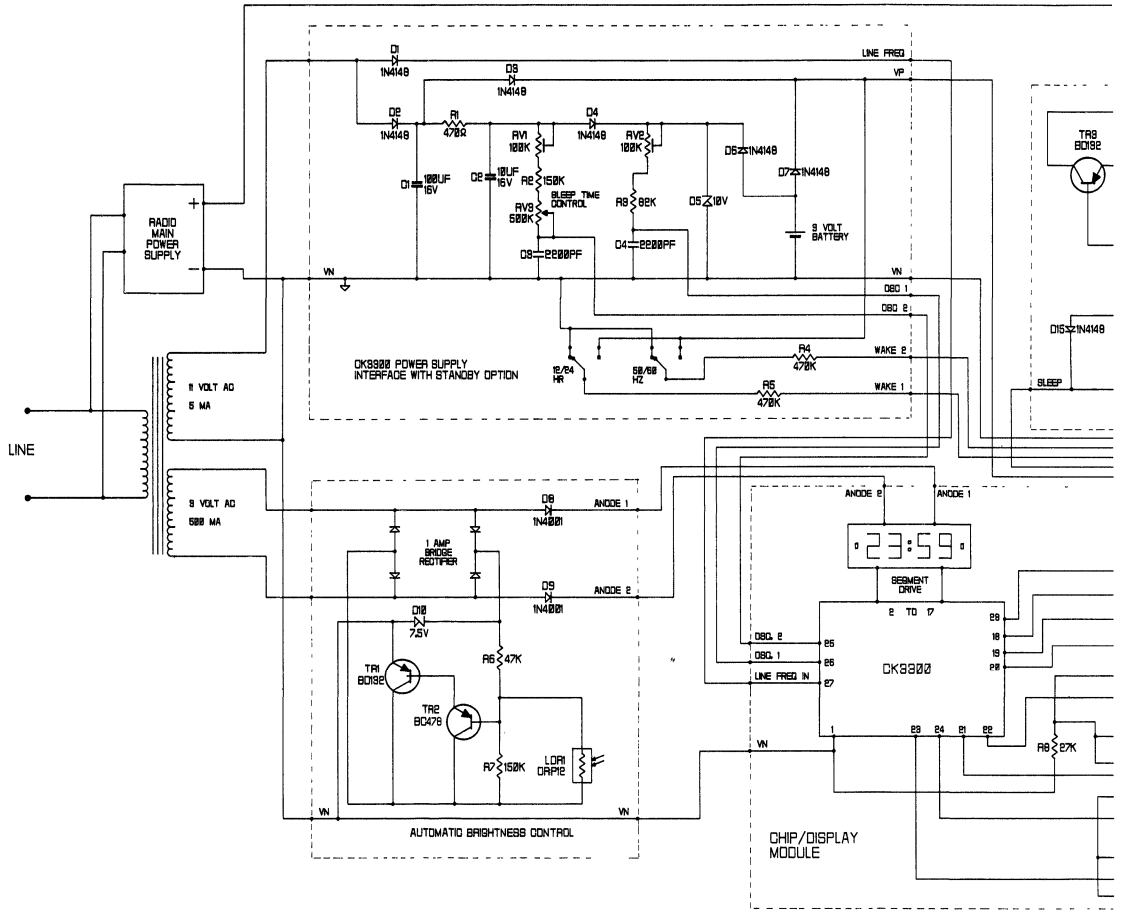


Fig. 22(a) TYPICAL "FULL-FEATURE" CLOCK RADIO CIRCUITRY

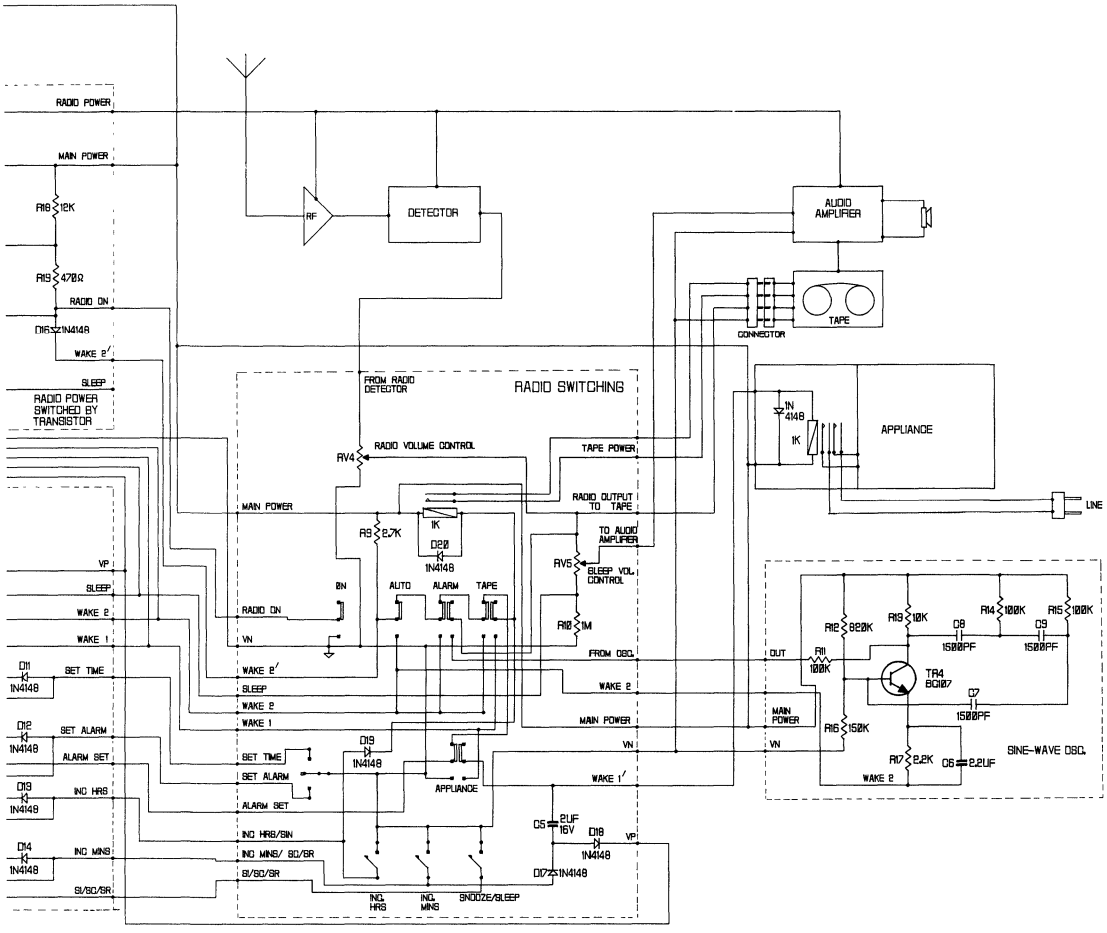


Fig.22(b) TYPICAL "FULL-FEATURE" CLOCK RADIO CIRCUITRY

Appliances

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
DIGITAL THERMOMETER	Digital thermometer and temperature controller.	AY-3-1270	7-32

GENERAL INSTRUMENT

AY-3-1270

Digital Thermometer and Temperature Controller

FEATURES

- Measurement and control range −399° C to +399° C (option 200° C to 499° C)
- Accuracy ±1.5° C, 0° C to −30° C using Thermistor temperature sensor
- Direct drive of liquid crystal displays
- Direct drive of 0.6" common anode L.E.D. displays
- 40 pin dual in line package
- Can be used as a digital voltmeter with digital autozero ±399 range
- 9 volt supply
- Leading zero blanking
- Power failure and over-range indication by flashing display
- Adjustable Hysteresis 0, 0.2, 0.4, 0.8, 2, 4, 8 degrees
- Two control/alarm outputs, HIGH and LOW

DESCRIPTION

The Digital Thermometer/Controller chip is an N-Channel MOS integrated circuit which when used in conjunction with a Thermistor, an L.E.D. or L.C.D display and a power supply forms a complete unit intended primarily for use in Deep Freezers, though it may also be used for the display and control of any parameter.

Two control outputs are provided, one which operates when the reading is higher than the set point and the other when the reading is lower. The switching hysteresis is presettable as required.

A power fail detector is incorporated on the chip. If power is removed for more than a specified time, the initial reading at restoration of power will be retained and the display will flash. The display will also flash if during normal operation an over-range condition occurs.

With minor changes to the peripheral circuitry, the chip can be used for other temperature ranges, or used as a 2¾ digit digital voltmeter.

OPERATION

The chip uses a single ramp conversion technique to measure the imbalance of a thermistor bridge temperature sensor. A digital autozero system which operates on every other measurement cycle, is employed to compensate for offsets in the comparators.

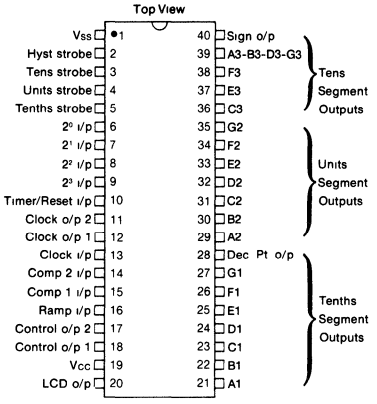
The chip may be used as a digital voltmeter by removing the thermistor network and connecting the signal to be measured between the two comparator inputs.

The set point circuitry compares the actual reading to the value presented to the set point inputs.

Two outputs are provided, one which operates at Set Point plus Hysteresis and the other which operates at Set Point minus Hysteresis. In addition, .05° display hysteresis has been introduced to prevent control output and L.S.D. jitter An optional power failure detection circuit is provided At power up the chip will read normally for about 10 sec—actual time determined by an external capacitor—then it will store the last reading and flash the display. In this condition the chip will continue to make measurements and operate the control outputs normally Operating the reset button will restore the normal display. If there is a short duration power failure the circuit will ignore it, if it lasts longer than 10 sec the alarm condition will occur

PIN CONFIGURATION

40 LEAD DUAL IN LINE



HIGH READING OPTION

For normal operation Pin 39 drives segments A3, B3, D3 and G3 in parallel. Pin 38 drives segment F3, Pin 37 drives segments E3 and Pin 36 drives segment C3.

For 20.0 to 49.9 range Pin 39 drives segment C3. Pin 38 drives segment E3, Pin 37 drives segment A3 and D3 and Pin 36 drives segment F3. Segments B3, G3 are connected to Pin 28 (Decimal Point).

PIN FUNCTIONS

Pin No.	Name	Description
1	V_{SS}	Negative Supply (0_V)
2	Hysteresis Strobe Output	Common output for Hysteresis and LED select switches
3	Tens Strobe Output	Common output for Tens and Sign select switches
4	Units Strobe Output	Common output for Units select switches
5	Tenths Strobe Output	Common output for Tenths select switches
6	Set Point 2^0 Input	Common input for 2^0 bit
7	Set Point 2^1 Input (Control & Hysteresis)	Common input for 2^1 bit
8	Set Point 2^2 Input (Control & Hysteresis)	Common input for 2^2 bit
9	Set Point 2^3 Input (Control & Hysteresis)	Common input for 2^3 bit
10	Timer Input/Reset Timer Input	Connected to a capacitor to V_{SS} and switch to V_{CC} for power failure detection and reset. The nominal delay time is 10 sec when a 10μF capacitor is used
11	Clock Output 2	Connected to frequency determining network
12	Clock Output 1	See Figure 1
13	Clock Input	
14	Comparator Input 2	Connected to nominal $V_{CC}/2$ reference
15	Comparator Input 1	Connect to thermistor network
16	Ramp Input	Connect to Resistor to V_{CC} and Capacitor to V_{SS}
17	Control Output 2 (HIGH)	Open drain output which turns ON when reading is greater than (Set Point + Hysteresis). Turns OFF again when reading equals Set Point
18	Control Output 1 (LOW)	Open drain output which turns OFF when reading equals (Set Point—Hysteresis)
19	V_{CC}	Positive supply (9V nom.)
20	LCD Backplate Output	Square wave output to drive backplate of LCD display
21	Segment A1 Output	
22	Segment B1 Output	
23	Segment C1 Output	
24	Segment D1 Output	
25	Segment E1 Output	
26	Segment F1 Output	
27	Segment G1 Output	
28	Decimal Point Output	
29	Segment A2 Output	Tens, Units and Tenths 7 segment outputs
30	Segment B2 Output	In LED mode these are open drain outputs
31	Segment C2 Output	designed to sink 12.5mA per segment
32	Segment D2 Output	In LCD mode these are push pull outputs
33	Segment E2 Output	
34	Segment F2 Output	
35	Segment G2 Output	
36	Segment C3 Output	
37	Segment E3 Output	
38	Segment F3 Output	
39	Segment A3, B3, D3, G,	
40	Sign Output	On for a negative reading

CLOCK OSCILLATOR

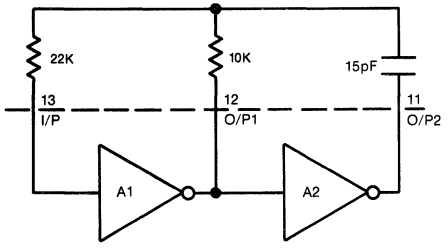
The Clock oscillator is designed to operate with an R-C network, an LC network or a Ceramic resonator. The choice will depend on the system Temperature and Voltage stability requirements.

As the thermometer reading is directly proportional to the clock frequency a ceramic resonator is recommended for frequency stability. In systems where only small variations in supply voltage and ambient temperature occur an R-C network could be used. The frequency variation over the specified operating range with an R-C is about ±22% (i.e. from 7V to 11V supply variation and −25° C to 70° C Temperature variation).

CHIP INTERFACE CIRCUITS

The input configuration on the Set Point inputs is shown in Fig. 2.

The circuit for the display drive is shown in Fig. 3. and shows the internal switching required to drive LED or LCD displays.



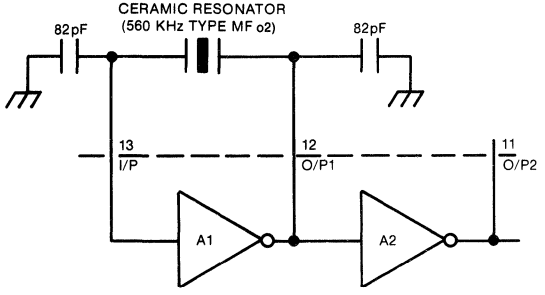


Fig. 1 TYPICAL OSCILLATOR CONFIGURATIONS

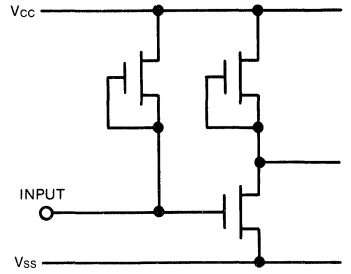


Fig. 2 SET POINTS INPUTS

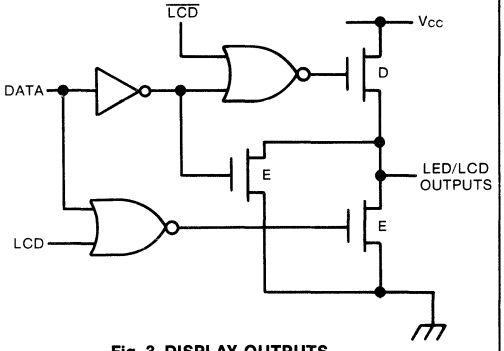


Fig. 3 DISPLAY OUTPUTS

ANALOG CIRCUITRY

The Temperature measuring circuit consists of a bridge network connected across the power supplies.

One side of the bridge (which is connected to comparator 2 input) consists of two equal value fixed resistors. These set up a reference potential of approximately $V_{CC}/2$ (4.5V). The other side of the bridge (which is connected to Comparator 1 Input) consists of a Thermistor and a series resistor connected to V_{CC} and a resistor connected to V_{SS}. A suitable thermistor is Mullard Type 640-90003.

The bridge is arranged to balance at 0°. As the temperature varies, the voltage at Comparator 2 input goes from approximately 3V (at −39.9°) to 6V (at +39.9°) in a non linear fashion.

A non linear ramp is generated by R and C and the time taken for the ramp voltage to change from one comparator input voltage to the other gives the temperature. R is varied to adjust the FSD. The non linearity of the ramp to a large extent compensates for the non linearity of the thermistor network.

For use with linear sensors or as a digital voltmeter the Resistor would be replaced by a current source.

Reading will be negative if comparator input 1 voltage < comparator input 2.

Typical circuit diagrams showing the AY-3-1270 displaying temperature in a freezer are shown in Fig 9 (with LED display) and Fig. 10 (with LCD display).

SET POINT PROGRAMMING

To set the control temperature, diodes are inserted in the program matrix with the cathodes connected to the strobe lines on pins 2, 3, 4. The code is B. C. D , and any temperature within the operating range can be selected by a suitable combination of diodes. For a negative temperature set point, a diode is inserted between pins 8 and 3

When an L.E D display is being used the diode between pins 9 and 2 is inserted, which inhibits the L.C D. backplate waveform This waveform is shown in Fig. 4.

A timing waveform for the strobe lines is shown in Fig. 5

2^0 (pin 6)	2^1 (pin 7)	2^2 (pin 8)	2^3 (pin 9)	
0.1	0 2	0.4	0.8	Tenths (pin 5)
1	2	4	8	Units (pin 4)
10	20	Minus	Do not Use	Tens (pin 3)
A	B	C	LED Display	Hysteresis (pin 2)

To set the hysteresis level, that is the temperature difference above and below the "set point" at which the control outputs operate, diodes are inserted in locations A, B, and C according to the following table Fig 6 shows the control output characteristics with temperature

	Hysteresis	A	B	C
	0			
	±0 2	*		
	±0 4		*	
	±0 8	*	*	
Note 2	±2	*		*
Note 2	±4		*	*
Note 2	±8	*	*	*

*indicates presence of a programming diode

NOTES:

1. Set points must consist of valid BCD codes or incorrect readings will occur
2. The ½° LSD Control and Display hysteresis should also be taken into account.
3. When in the "High Reading" mode it is necessary to program a set point 10° C lower than that required.
   e.g. To select 44° C diodes are inserted in the matrix between pins 6, 3/7, 3/8, 4
4. Nominal hysteresis value; for actual hysteresis obtained see table on following page.

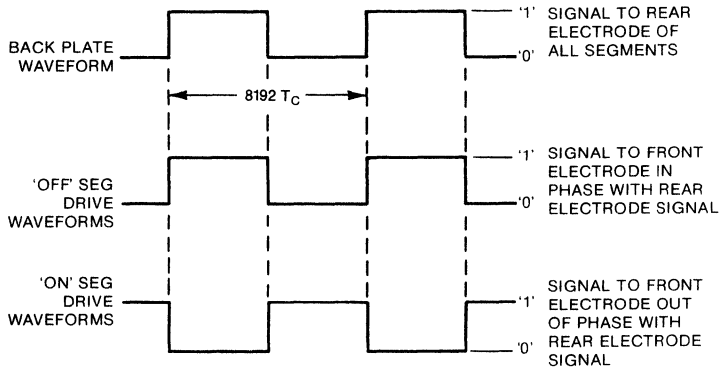
HYSTERESIS

When ±2, ±4 or ±8 is set the actual hysteresis obtained is as shown.

Set Temp.	Hyst. ±2	Hyst. ±4	Hyst. ±8
+XX9	+2 0/−1.9	+4.0/−3.9	+8.0/−7.9
+XX8	+2.1/−1.8	+4.1/−3.8	+8.1/−7.8
+XX7	+2.2/−1.7	+4.2/−3.7	+8.2/−7.7
+XX6	+2.3/−1.6	+4.3/−3.6	+8.3/−7.6
+XX5	+2.4/−1.5	+4.4/−3.5	+8.4/−7.5
+XX4	+2.5/−1.4	+4 5/−3.4	+8 5/−7 4
+XX3	+2.6/−1.3	+4.6/−3.3	+8.6/−7.3
+XX2	+2 7/−1.2	+4.7/−3.2	+8.7/−7.2
+XX1	+2 8/−1 1	+4.8/−3 1	+8.8/−7 1
+XX0	+2 9/−2.0	+4.9/−4.0	+8.9/−8.0
+000	+2.9/−2.9	+4.9/−4.9	+8 9/−8.9
−000	+2 9/−2 9	+4.9/−4.9	+8.9/−8 9
−XX0	+2 0/−2 9	+4 0/−4.9	+8.0/−8.9
−XX1	+1 1/−2.8	+3.1/−4 8	+7.1/−8.8
−XX2	+1 2/−2 7	+3.2/−4 7	+7 2/−8.7
−XX3	+1.3/−2 6	+3.3/−4 6	+7.3/−8 6
−XX4	+1.4/−2 5	+3.4/−4 5	+7 4/−8 5
−XX5	+1 5/−2 4	+3.5/−4 4	+7.5/−8.4
−XX6	+1 6/−2.3	+3.6/−4 3	+7.6/−8 3
−XX7	+1.7/−2.2	+3.7/−4 2	+7 7/−8 2
−XX8	+1.8/−2.1	+3.8/−4 1	+7 8/−8 1
−XX9	+1.9/−2 0	+3.9/−4 0	+7 9/−8 0

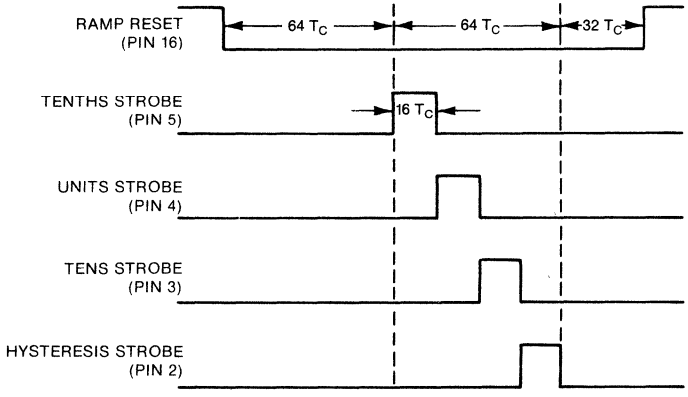
When ±2, ±4 or ±8 is set and the set point is less than or equal to the hysteresis setting then the actual hysteresis is given by the following table:

Set Temp.	Hyst. ±2	Hyst. ±4	Hyst. ±8
+XX9	+2.0/−2.8	+4.0/−4.8	+8.0/−8.8
+XX8	+2.1/−2.7	+4.1/−4.7	+8.1/−8.7
+XX7	+2.2/−2.6	+4.2/−4.6	+8.2/−8.6
+XX6	+2.3/−2.5	+4.3/−4.5	+8.3/−8.5
+XX5	+2.4/−2.4	+4.4/−4.4	+8.4/−8.4
+XX4	+2.5/−2.3	+4.5/−4.3	+8.5/−8.3
+XX3	+2.6/−2.2	+4.6/−4.2	+8.6/−8.2
+XX2	+2.7/−2.1	+4.7/−4.1	+8.7/−8.1
+XX1	+2.8/−2.0	+4.8/−4.0	+8.8/−8.0
+XX0	+2.9/−2.9	+4.9/−4.9	+8.9/−8.9
+000	+2.9/−2.9	+4.9/−4.9	+8.9/−8.9
−000	+2.9/−2.9	+4.9/−4.9	+8.9/−8.9
−XX0	+2.9/−2.9	+4.9/−4.9	+8.9/−8.9
−XX1	+2.0/−2.8	+4.0/−4.8	+8.0/−8.8
−XX2	+2.1/−2.7	+4.1/−4.7	+8.1/−8.7
−XX3	+2.2/−2.6	+4.2/−4.6	+8.2/−8.6
−XX4	+2.3/−2.5	+4.3/−4.5	+8.3/−8.5
−XX5	+2.4/−2.4	+4.4/−4.4	+8.4/−8.4
−XX6	+2.5/−2.3	+4.5/−4.3	+8.5/−8.3
−XX7	+2.6/−2.2	+4.6/−4.2	+8.6/−8.2
−XX8	+2.7/−2.1	+4.7/−4.1	+8.7/−8.1
−XX9	+2.8/−2.0	+4.8/−4.0	+8.8/−8.0



T_C = CLOCK PERIOD

Fig. 4 LCD DRIVE WAVEFORM



T_C IS CLOCK PERIOD

REPETITION RATE OF ABOVE CYCLES IS TWICE MEASUREMENT CYCLE

Fig. 5 STROBE OUTPUT TIMING

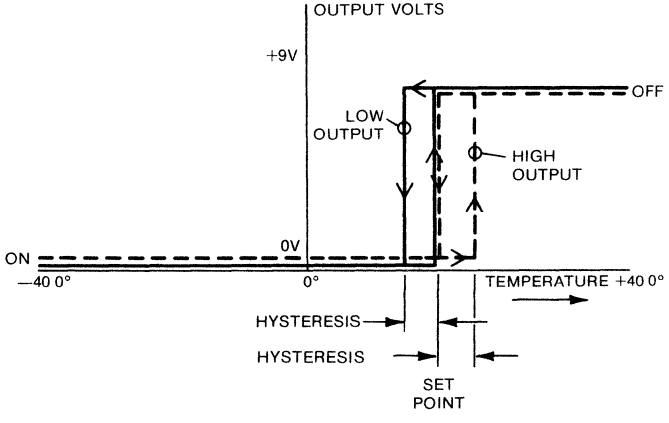


Fig. 6 SET POINT HYSTERESIS

MEASUREMENT AND READ CYCLE

In order to compensate for offsets in the comparators, a digital autozero cycle operates on every other measurement cycle Fig. 7 shows the internal ramp and comparator waveform.

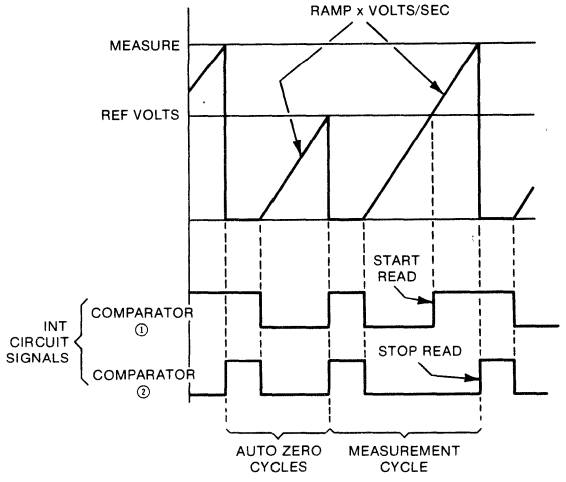


Fig. 7 TYPICAL MEASUREMENT/READ CYCLE

SYSTEM DIAGRAM

Fig 8 shows a block schematic of the AY-3-1270 circuit

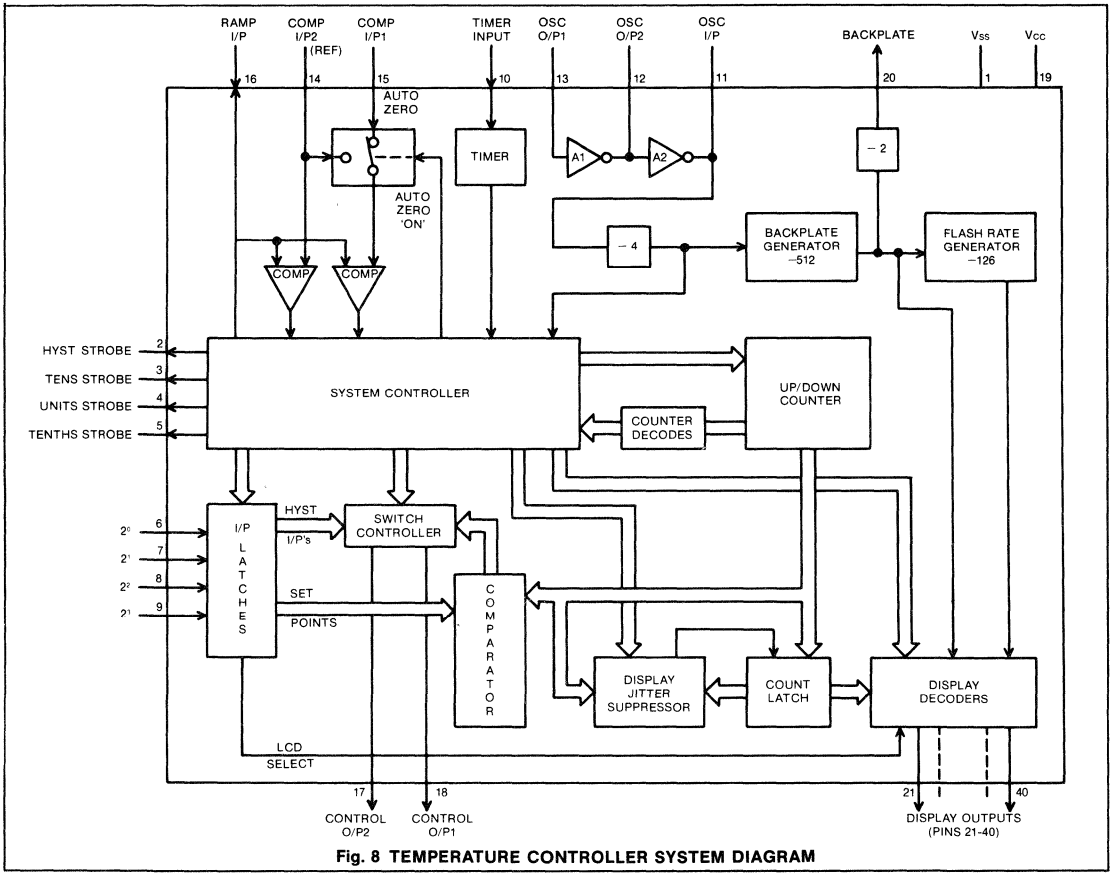


Fig. 8 TEMPERATURE CONTROLLER SYSTEM DIAGRAM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} ..... −0.3 to +18
Storage Temperature Range ..... −65°C to +150°C
Ambient Operating Temperature Range ..... −25°C to +70°C
Maximum Power Dissipation at 70°C 800mW
Maximum Segment Output Current (LED Mode) 20mA
Maximum Switch Output Current 30mA
Maximum Total Output Current 250mA

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):

V_{SS} = 0V V_{CC} = (7.2V to 10.8V) T_{amb} = −25°C to +70°C, positive logic convention

Characteristics	Min	Typ	Max	Units	Conditions
Segment, DP, Sign Outputs LED mode					
On resistance	—	—	120	Ω	V_{out} = +1.5V I_{sink} = 12.5mA
On resistance E3	—	—	60	Ω	V_{out} = +1.5V I_{sink} = 25mA
On resistance DP	—	—	40	Ω	V_{out} = +1.5V I_{sink} = 37.5mA
On resistance (A3, B3, D3, G3)	—	—	30	Ω	V_{out} = +1.5V I_{sink} = 50mA
Segment, DP, Sign Outputs LCD mode					
Logic '0' output	—	—	400	mV	Load = 50pF + 1M Ohm to
Logic '1' output	V_{CC}−400	—	—	mV	E3 load = 100pF + 500K DP load = 150pF + 330K A3, B3, D3, G3 load = 200pF + 250K Backplate load = 1000pF + 50K
Rise time	—	—	—	—	Under specified load conditions
Fall time	—	—	—	—	Under specified load conditions
Frequency	—	68	—	Hz	Clock (560kHz)
Control Outputs					
On resistance	—	—	75	Ω	V_{out} = +1.5V I_{sink} = 20mA
Off leakage	—	—	10	μA	V_{out} = +15 Volts
Strobe Outputs					
On resistance	—	—	400	Ω	V_{out} = +1V I_{sink} = 2.5mA
Off leakage	—	—	10	μA	V_{out} = V_{CC}
Frequency	—	—	—	—	2 x reading rate
Pulse width	—	28 6	—	μs	Clock frequency = 560kHz
Set Point Inputs					
Logic '0' level	V_{SS}	—	2	V	
Logic '1' level	6	—	V_{CC}	V	
Pull up resistance	20	—	100	KΩ	to V_{CC} V_{in} = V_{SS}
Comparator Inputs					
Leakage current	—	—	1	μA	V_{in} = V_{CC}
Resolution	5	—	—	mV	
Common Mode Range	0.1	—	V_{CC}−3V	V	
Impedance between either input and ramp input	1	—	—	MΩ	Clock frequency = 560kHz
Ramp Input					
Discharge resistance	—	—	100	Ω	V_{out} = +1V I_{sink} = 10mA See note 1
Leakage current	—	—	1	μA	V_{in} = V_{CC}
Timer Input					
Flash Threshold	0 5V_{OC}	—	0.7V_{OC}	V	
Reset Threshold	—	—	6	V	
Pull up resistance	500	—	2500	KΩ	to V_{CC} (V_{in} = V_{SS})
Pull down resistance	50	—	250	KΩ	to V_{SS} (V_{in} = V_{CC})
Open circuit input voltage (V_{OC})	2	2.6	3.5	V	
Clock					
Frequency	300	—	800	kHz	
Gain to output 1 (A1)	3	—	—	—	small signal open loop
Gain to output 2 (A2)	3	—	—	—	AC gain, F = 560kHz
Input capacitance	—	—	12	pF	
Count frequency	—	6.25	—	kHz	Clock (560kHz) ÷ 32 see note 2
Flash rate, Overrange and Power Fail	—	1	—	Hz	Clock (560kHz) ÷ 158048
Supply current	—	25	—	mA	V_{CC} = 9V, T_{amb} = 25°C
	—	—	45	mA	V_{CC} = 11V, T_{amb} = − 25°C

NOTES 1 Minimum resistance to V_{CC} = 1KΩ Maximum capacitance to V_{SS} = 10μf.

2. Reading is measurement time divided by Count Frequency period Measurement time depends on both the voltage difference at the Comparator inputs and ramp speed at pin 16.

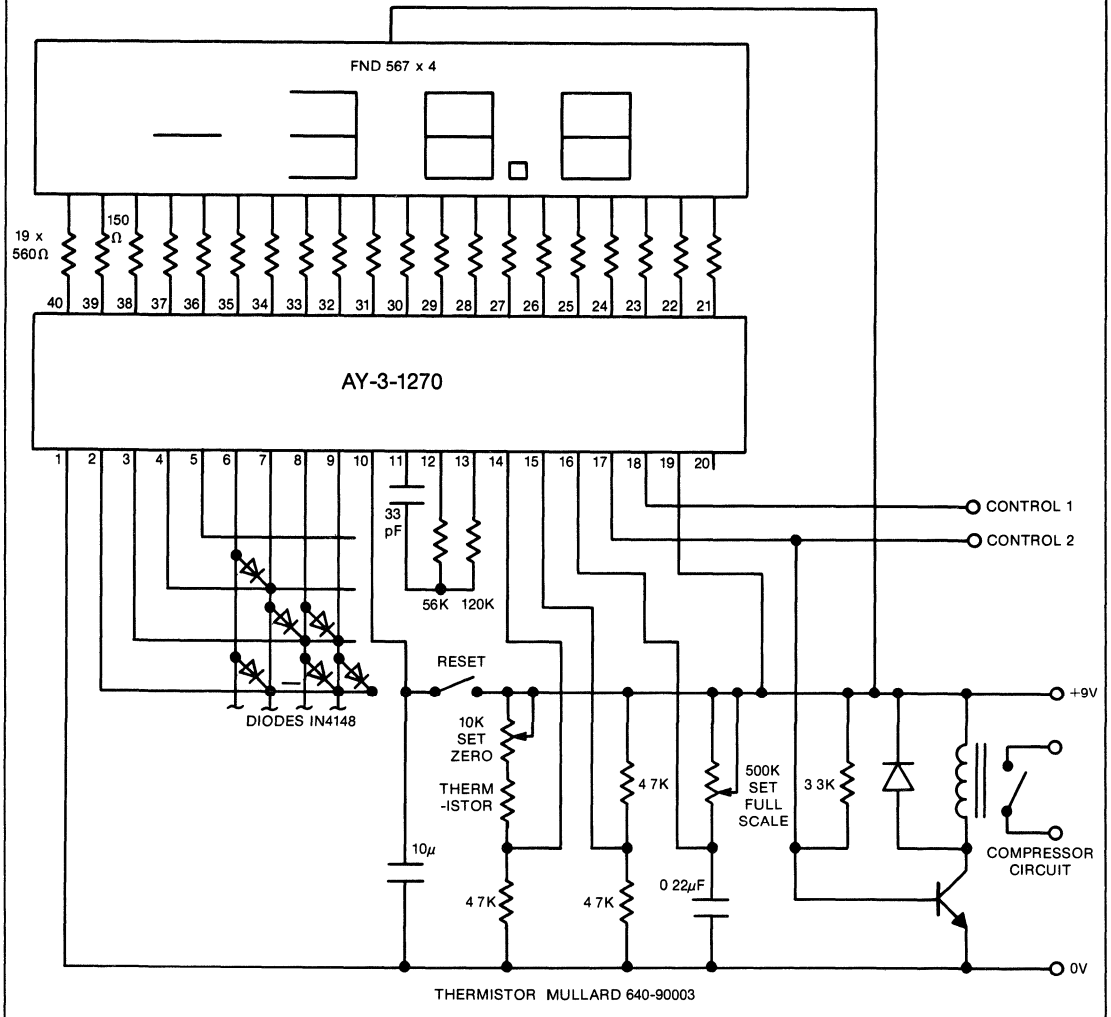


Fig. 9 THERMOMETER WITH LEAD DISPLAY

Remote Control

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
REMOTE CONTROL TRANSMITTER	256 Command PCM infrared transmitter	AY-3-8470	7-42
REMOTE CONTROL RECEIVER	256 Command PCM infrared receiver	AY-3-8475	7-48

GENERAL INSTRUMENT

AY-3-8470

256 Command Infrared Remote Control Transmitter

FEATURES

- 256 Commands (possibly 32 commands by 3 bit address)
- Low Standby current (<20μA)
- Low duty cycle (< 8%)
- 6/9 Volt battery operation
- Simple RC defined on chip Oscillator
- 22 pin DIL package
- Single shot or continuous operation
- Transmission format ensuring error free reception

DESCRIPTION

The AY-3-8470 transmitter together with AY-3-8475 receiver, an infrared link and an amplifier, forms a complete remote control system Control of standard functions of radios and televisions is possible together with TV games, Teletext and Viewdata applications

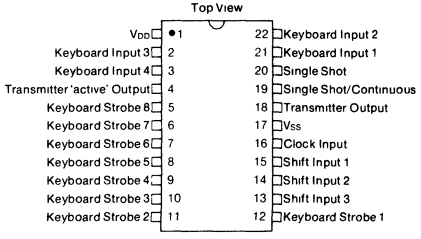
Complementary MOS technology for this device allows low voltage battery operation with a very low standby current.

256 output commands are possible which can be simply activated by a standard 8 x 4 keypad together with 3 shift inputs.

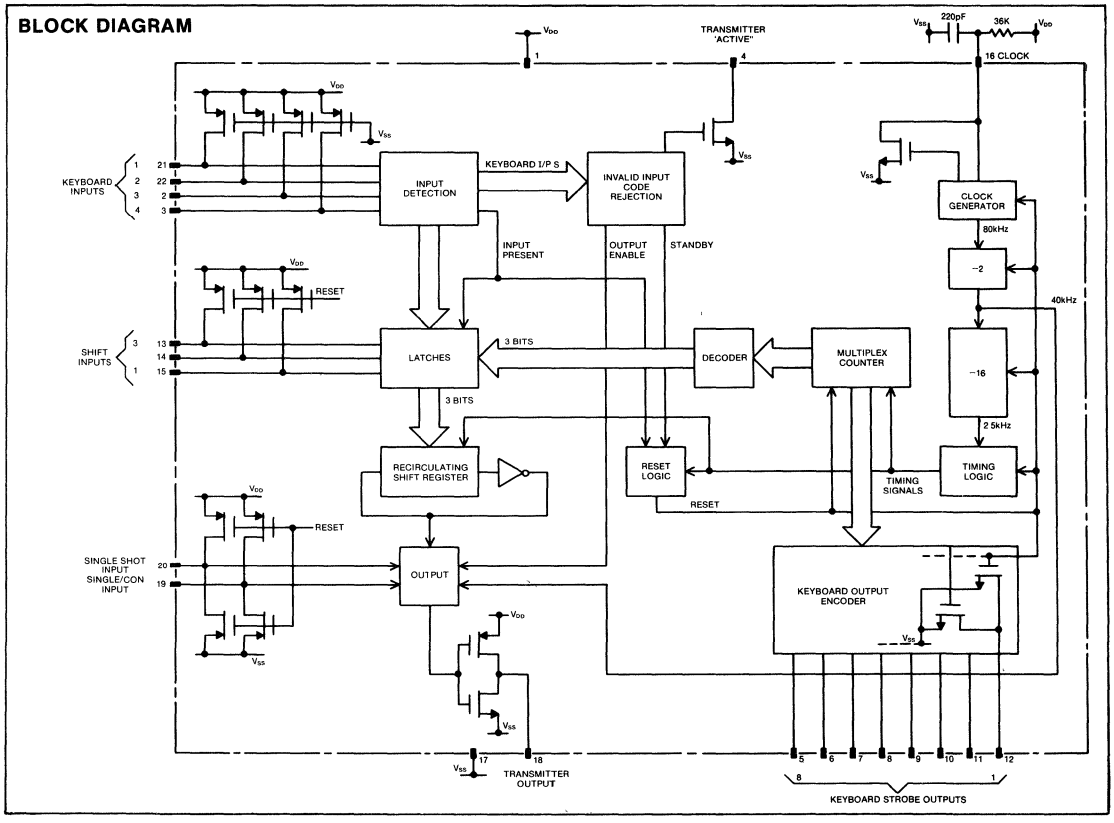
A non critical, simple RC oscillator is used to fix the transmitter frequency

PIN CONFIGURATION

22 PIN DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} ..... −0.3 to +12V
Ambient Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

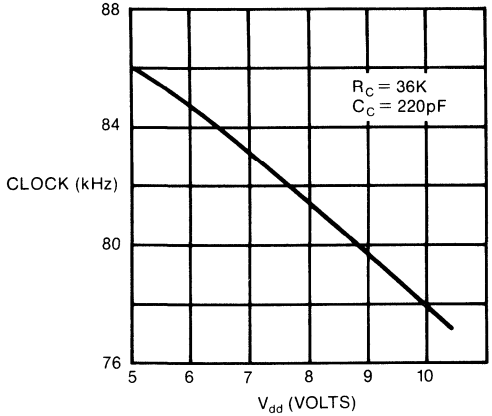
Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated)

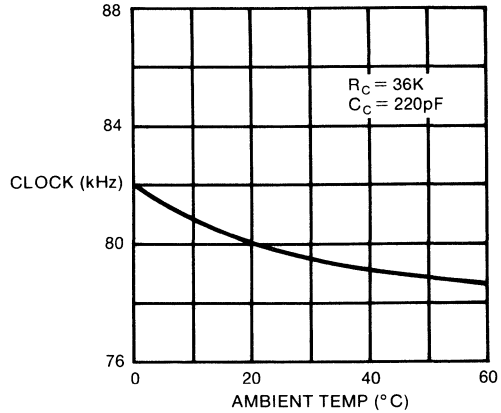
V_{SS} = 0 Volts
V_{DD} = +5 5 to +10 Volts
Temperature = 0° C to 70° C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Clock Frequency (16)	Fc	60	80	100	kHz	V_{DD} = 5.5 to 10.0 V, T = 25° C Cc and Rc at typical values and Cc Rc tolerance ±5%
Resistor to V_{DD}	Rc	12	39	100	KΩ	
Capacitor to V_{SS}	Cc	—	220	—	pF	
Leakage to V_{SS}	—	—	—	2	μA	Clock "OFF" in 'standby' and V_{out} = V_{DD} = 10 0 Volts
Shift (13, 14, 15), Keyboard (2, 3, 21, 22) and Single Shot (19, 20) Input Thresholds						
Low Level	V_{IL}	V_{SS}	—	1.5	V	V_{DD} = 5 5 Volts
	V_{IL}	V_{SS}	—	2 5	V	V_{DD} = 10.0 Volts
High Level	V_{IH}	V_{DD}-1 5	—	V_{DD}	V	V_{DD} = 5 5 Volts
	V_{IH}	V_{DD}-2 5	—	V_{DD}	V	V_{DD} = 10.0 Volts
Pull Up to V_{DD}						
Low Level Source	I_{IL}	—	—	50	μA	V_{IN} = 1.5 Volts, V_{DD} = 5.5 Volts
	I_{IL}	—	—	200	μA	V_{IN} = 2.5 Volts, V_{DD} = 10 0 Volts
High Level	—	V_{DD} -1.5	—	—	V	I_{IH} = 2μA source
Transmitter Output (18)						
Low Level	V_{OL}	—	—	0 5	V	I_{OL} = 75μA sink
High Level	V_{OH}	V_{DD}-0.5	—	—	V	I_{OH} = 1.0mA source
Keyboard Strobe Outputs (5-12)						
Low Level	V_{OL}	—	—	0 5	V	I_{OL} = 150μA sink, V_{DD} = 5.5 Volts
	V_{OL}	—	—	1 5	V	I_{OL} = 600μA sink, V_{DD} = 10.00 Volts
Off Leakage to V_{SS}	—	—	—	2 0	μA	V_{OUT} = V_{DD} = 10.0 Volts
Transmitter 'Active' Output (4)						
Low Level	V_{OL}	—	—	1 5	V	I_{OL} = 1 5mA sink
Off Leakage to V_{SS}	—	—	—	2	μA	V_{OUT} = V_{DD} = 10 0 Volts
Single Shot (20), Single Shot/Continuous (19) Inputs						
Standby Pull Down to V_{SS}	V_{OL}	—	—	0 5	V	I_{OL} = 10μA sink
Supply Current V_{DD} (1)	I_{DD}	—	1	3	mA	V_{DD} = 10 0 Volts
Standby Current V_{DD} (1)	I_{DD}	—	5	20	μA	V_{DD} = 9 0 Volts, T= 25° C

NOTES 1 Pull Ups are configured with Enhancement FET's
2 Current from the device is defined as 'source' current, current into the device is 'sink' current



TYPICAL CLOCK VERSUS V_{dd} @ 25°C



TYPICAL CLOCK VERSUS TEMPERATURE FOR V_{dd} = 9 VOLTS

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{DD}	Positive Supply 5.5 to 10 0 Volts
2	Keyboard Input 3	Together with Pins 21, 22, these are the 4 keyboard inputs which under normal operations may only go active low one at a time
3	Keyboard Input 4	
4	Transmitter 'active' output	Output goes low during a cycle in which a transmission is output
5	Keyboard O/P 8	The 8 Keyboard Outputs are active low which strobe the Keyboard every transmission cycle (i e every 102 4ms for 80kHz clock) (See Fig. 1) The outputs are open drain.
6	Keyboard O/P 7	
7	Keyboard O/P 6	
8	Keyboard O/P 5	
9	Keyboard O/P 4	
10	Keyboard O/P 3	
11	Keyboard O/P 2	
12	Keyboard O/P 1	
13	Shift 3	The Shift inputs correspond directly to the 3ms Bits of the output word. These inputs are active low.
14	Shift 2	
15	Shift 1	
16	Clock Input	Connect a resistor to V_{DD} and a capacitor to V_{SS} to determine the clock frequency
17	V_{SS}	Connect to 0 Volts
18	Transmitter Output	This output is in the form of a high going pulse stream at half clock rate modulated by the output code (See Fig. 1)
19	Single/Continuous Select	With this input low, Pin 19 high, and Shift 3 low, single shot is selected
20	Single Shot I/P	Connection low puts chip into single shot mode for all commands
21	Keyboard Input 1	
22	Keyboard Input 2	

OPERATION

Standby

Standby mode is entered when power is applied to the chip In this mode the 'clock' is inhibited, 'pull ups' are inactive (except Keyboard inputs), and all the Keyboard outputs are low (active)

Any key depression will now be immediately recognized, the chip will come out of standby and the 'all Keyboard outputs active' condition will be removed

Keyboard outputs now strobe the keyboard and detect which key is depressed At the end of a complete keyboard scan the relevant output is transmitted Keyboard scans continue and the relevant outputs transmitted, until a full keyboard scan occurs detecting no key depression, the chip then reverts to standby

Invalid Inputs

Invalid inputs occur due to multiple key depressions, they are·

(a) More than one Keyboard input active during a single keyboard output strobe time

(b) More than one keyboard input active during different keyboard output strobe times within a 'full' keyboard scan

The above inputs are rejected as invalid and no output code is transmitted although the chip remains active scanning the keyboard until it·

(a) receives a valid input which can be transmitted or

(b) it detects no keys pressed and reverts to standby

Output Code

Figure 1 shows a typical output code sequence and the relevant strobe timings

The output code takes the form of an 8 bit word followed by its inverse so ensuring a 'secure' infrared link The infrared receiver being able to distinguish this 'data' from spurious inputs

An example of the data is shown below Note the L S Bit is transmitted first

e g 0 0 1 1 0 1 0 0 (LSB) — INVERSE

1 1 0 0 1 0 1 1 (LSB) — TRUE

Each '0' bit is comprised of 32 pulses and each '1' bit 48 pulses The complete command consists of 16 bursts of 32 or 48 pulses The pulses have a nominal period of 25μs (i e 40kHz repetition rate) A burst takes 1.6ms and 16 bursts 25 6ms. During the 76 8ms the transmitter is inactive

Output Code Derivation —'the 8 bit word'

Figure 2 identifies the binary output codes associated with the 'basic' keyboard matrix

Binary codes can be expanded up to 255 by means of the shift inputs The table Figure 3 shows the states of these inputs for relevant output codes

Single Shot Operation

In this mode the code is transmitted only once after a key 'ON' is detected The key must now be released, the chip enters standby mode and is then ready for a further key depression. Commands can be entered up to a rate of 5 per second

An application for this mode of operation would be for transmitting page numbers for the General Instrument Teleview System.

The following table Fig. 4 shows the Single Shot modes of operation

Keyboard Implementations

Figure 5 shows how diodes can be employed to expand the basic 8 x 4 matrix to 128 keys The further Shift input expands the matrix to 256 commands

Figure 6 shows how a simple 8 way switch can be used to enable 256 commands from the basic 8 x 4 matrix

Transmitter

The circuit of Figure 6, employs 3 transmitting diodes pulsed at approximately 300mA, giving a range of up to 20 meters Average battery current for transmission is around 20mA with a standby current of only 20μA.

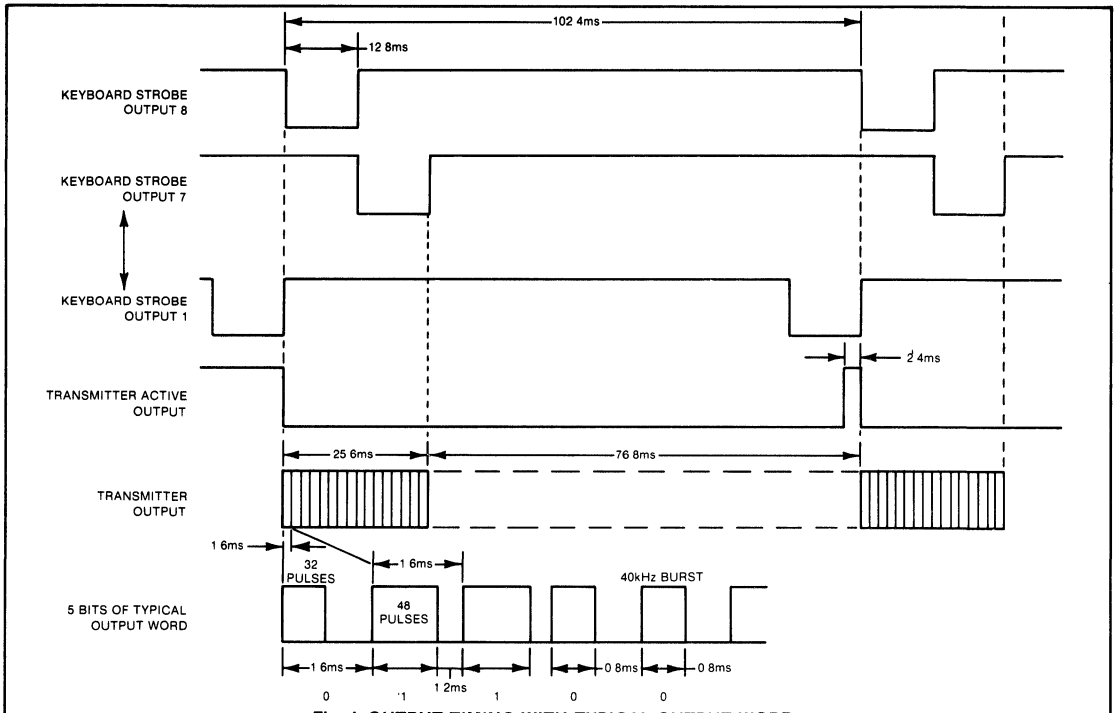
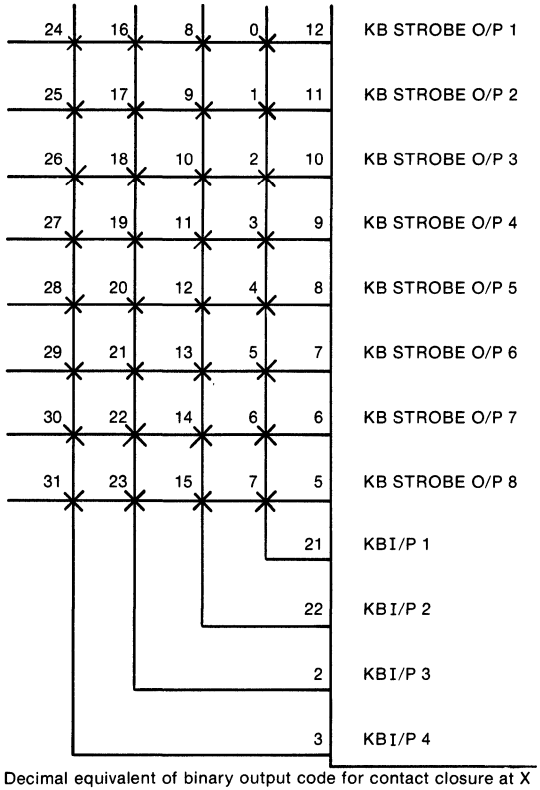


Fig. 1 OUTPUT TIMING WITH TYPICAL OUTPUT WORD



Decimal equivalent of binary output code for contact closure at X

Fig. 2 MATRIX FORMAT

Shift Input 3 (13)	Shift Input 2 (14)	Shift Input 1 (15)	Output Codes
H	H	H	0 to 31
H	H	L	32 to 63
H	L	H	64 to 95
H	L	L	96 to 127
L	H	H	128 to 159
L	H	L	160 to 191
L	L	H	192 to 223
L	L	L	224 to 255

H signifies High Level
L signifies Low Level

Fig. 3 SIGNIFICANCE OF SHIFT INPUTS

Single Shot Input (20)	Single Shot/ Continuous (19)	Mode
H	H	Continuous on all Codes.
L	'Don't care'	Single Shot on all Codes.
H	L	Codes 0 to 127 continuous. Codes 128 to 255 Single shot

NOTE: During Standby Single Shot Input (20) and Single Shot/ Continuous Input (19) are pulled low internally

Fig. 4 SINGLE SHOT MODES OF OPERATION

Code Allocations

Transmitted Code*	Receiver Functions (Using the AY-3-8475)
0	Program 1
1	Program 2
2	Program 3
3	Program 4
4	Program 5
5	Program 6
6	Program 7
7	Program 8
8	Program 9
9	Program 10
10	Program 11
11	Program 12
12	Program 13
13	Program 14
14	Program 15
15	Program 16
16	Volume Increase
17	Volume Decrease
18	Color Increase
19	Color Decrease
20	Brightness Increase
21	Brightness Decrease
22	Spare Increase
23	Spare Decrease
24	Normalize
25	Mute
26	ON/OFF to OFF
27	Spare 1 On
28	Spare 1 Off
29	Spare 1 Toggle
30	Spare 2 On
31	Spare 2 Off
32-47	Program 17-32
48-255	Spare

*Decimal equivalent of 8 bit binary word listed for convenience

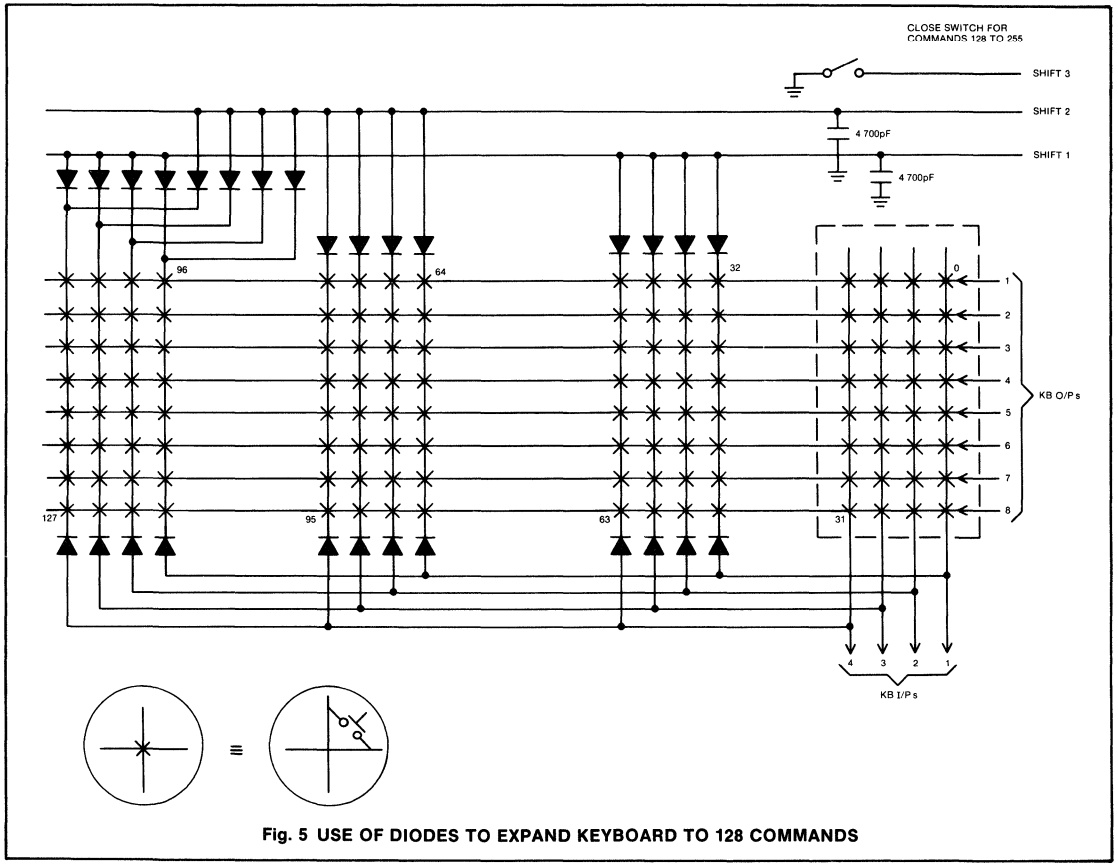


Fig. 5 USE OF DIODES TO EXPAND KEYBOARD TO 128 COMMANDS

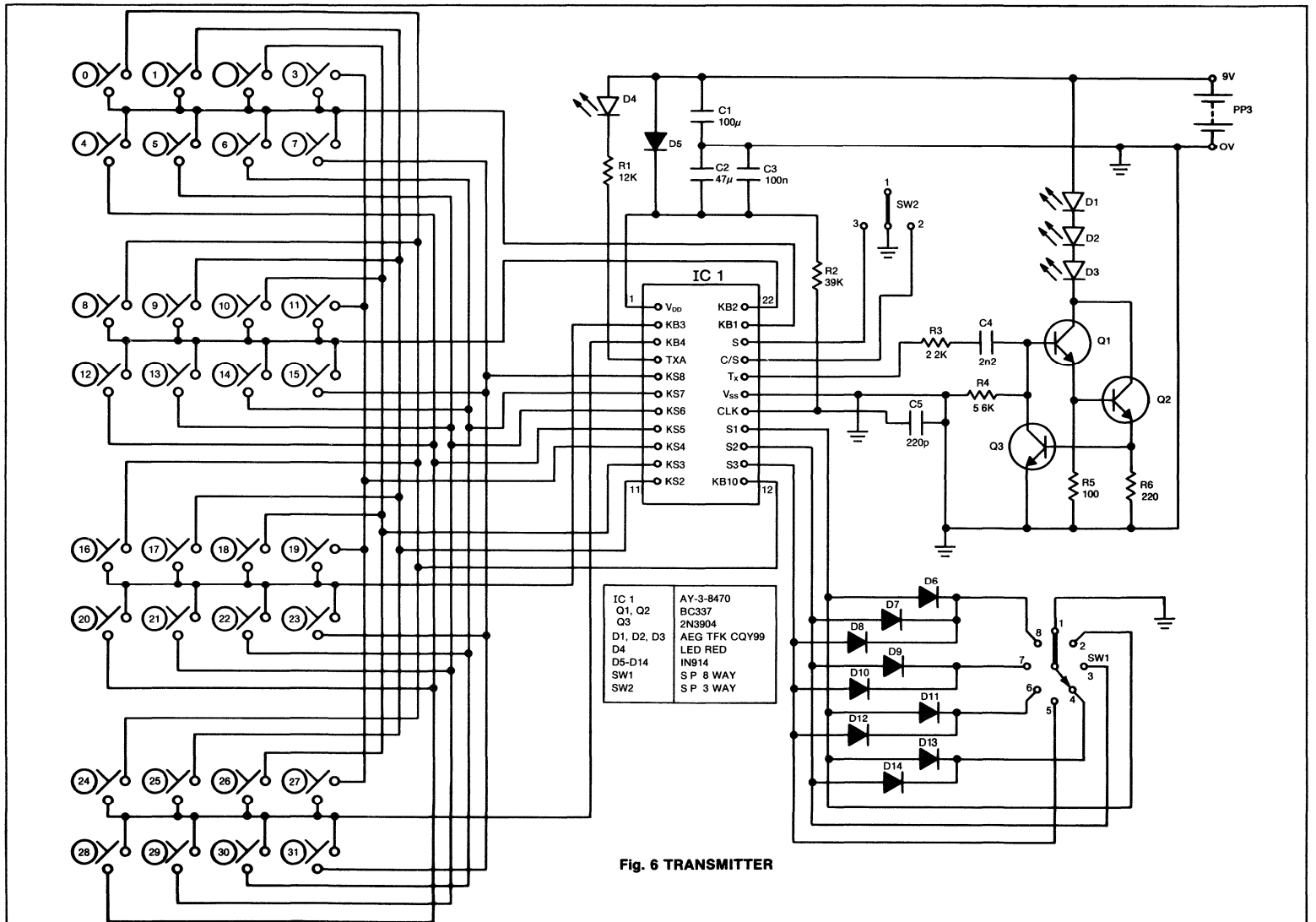


Fig. 6 TRANSMITTER

GENERAL INSTRUMENT

AY-3-8475

256 Command Infrared Remote Control Receiver

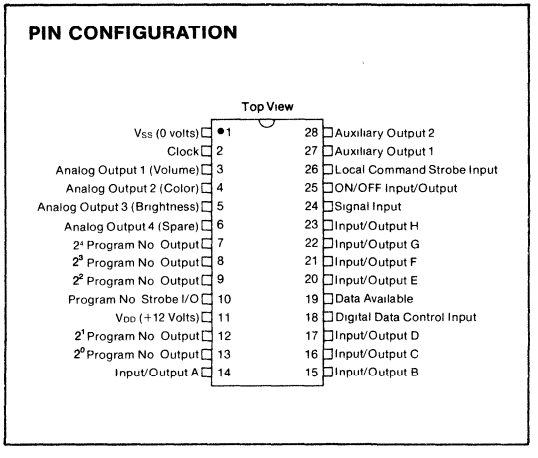
FEATURES

- 256 Commands
- Latched program number outputs
- 32 Programs
- 4 Analog Channels—62 step
- ON/OFF facility
- Normalize command on analog functions (except volume)
- 2 Auxiliary ON/OFF outputs (one with toggle facility)
- Local control of all 256 commands
- CPU Databus interface
- Direct Interface with General Instrument Teleview System
- Direct Interface with Economega TV and Radio Tuning Systems
- Command fully error checked ensuring secure link

DESCRIPTION

The AY-3-8475 receiver together with the AY-3-8470 transmitter forms a complete 256 command infrared remote control system Applications include both radios and television. Control of normal TV functions is possible together with Teletext/Viewdata. Direct interface is possible with the Economega electronic tuning systems.

PIN CONFIGURATION



OPERATION

All operations, repetition rates, set-up times and resolutions are related to the "Clock" Frequency of 2 5MHz unless otherwise stated.

Power On

When power is applied to the chip a power on reset is generated and outputs are as follows NOTE. power on to reset delay about 3μs

(a) Program Number Outputs set to 1 (00000) and Program No Strobe goes low for approximately 50ms.
(b) Analog outputs set to a mark space ratio of 32 31
(c) ON/OFF I/O set to OFF
(d) Auxiliary Outputs set to OFF
(e) Data Available set low.
(f) Input/Outputs A-H set low Note this data will only be presented to the output pins under control of the Digital Data Control input.

Any program command or a local ON command will turn on the ON/OFF output It will remain on until an 'OFF' command is received.

Normalization

The Normalize command sets analog outputs 2, 3 and 4 (color, brightness and Spare), to a mark space ratio of 32 31 Analog Output 1 (Volume) is not affected by the normalize command.

Muting

Analog Output 1 (Volume) is set low when a mute command is received. It is returned to its previous mark space ratio by·

(a) A further mute command
(b) Reception of any program command
(c) Switching on the ON/OFF output
(d) Reception of either the Volume increase, or Volume decrease commands

For a remote mute command the command is repeated every 100ms as long as the transmitter remains active. Only one mute command is actioned The transmitter must cease transmitting for at least 0 5 secs before a further mute command can be received, to toggle the function.

Signal Input

Figure 1 shows a typical command input from the IR Transmitter A Valid input takes the form of an 8 'bit' word followed by its inverse The L S Bit 'arrives' first

e g.	INVERSE								TRUE							
	0	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1
							LSB								LSB	

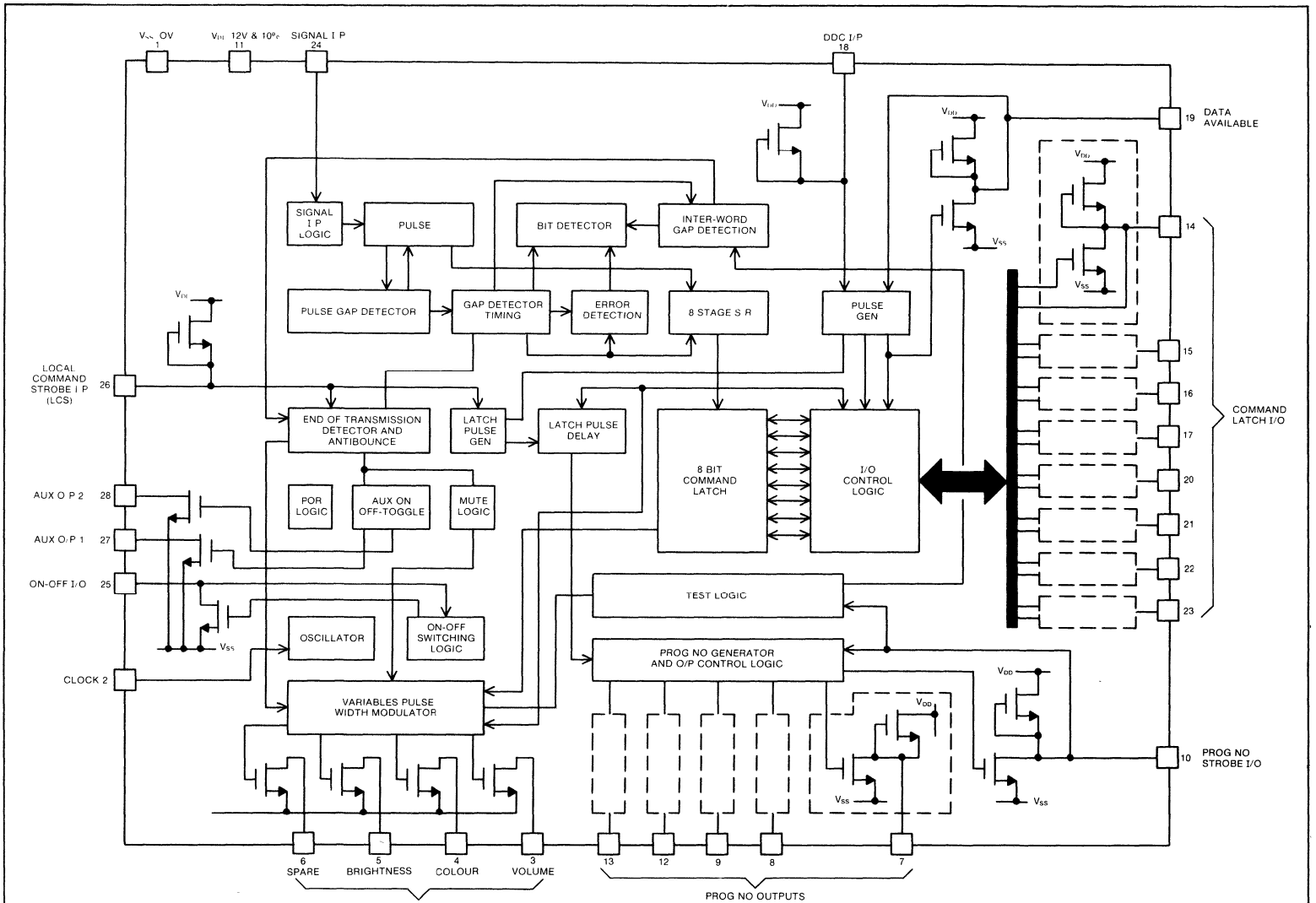
Each '0' bit is comprised of 32 pulses and each '1' bit of 48 pulses The complete command therefore consists of 16 bursts of 32 or 48 pulses. The pulses have a nominal period of 25μs (i e 40kHz repetition rate) A burst takes 1.6ms and 16 bursts 25.6ms. During the remaining 76 8ms the transmitter is inactive

The receiver will decode input frequencies in the range 30kHz to 50kHz for its specified operating range of Clock Frequencies The mark space ratio of the input waveform is not critical, however the mark or space interval should be at least 2μs.

The receiver has an error margin of ±8 pulses in each burst i.e. a '0' will be decoded if 25-40 pulses are received and a '1' will be decoded if 41-56 pulses are received.

The receiver 'looks for' a valid data bit i.e. a burst of pulses. The decoder synchronizes to this valid data bit and then looks for further 'bits' and inter-bit 'gaps'. If a sequence of an 8 bit word occurs, followed by its inverse then this is decoded as a command. Any erroneous bits or their inverses cause the decoder to reset and await resynchronization

Command data outputs A-H correspond directly to the 8 'bit' word.



BLOCK DIAGRAM

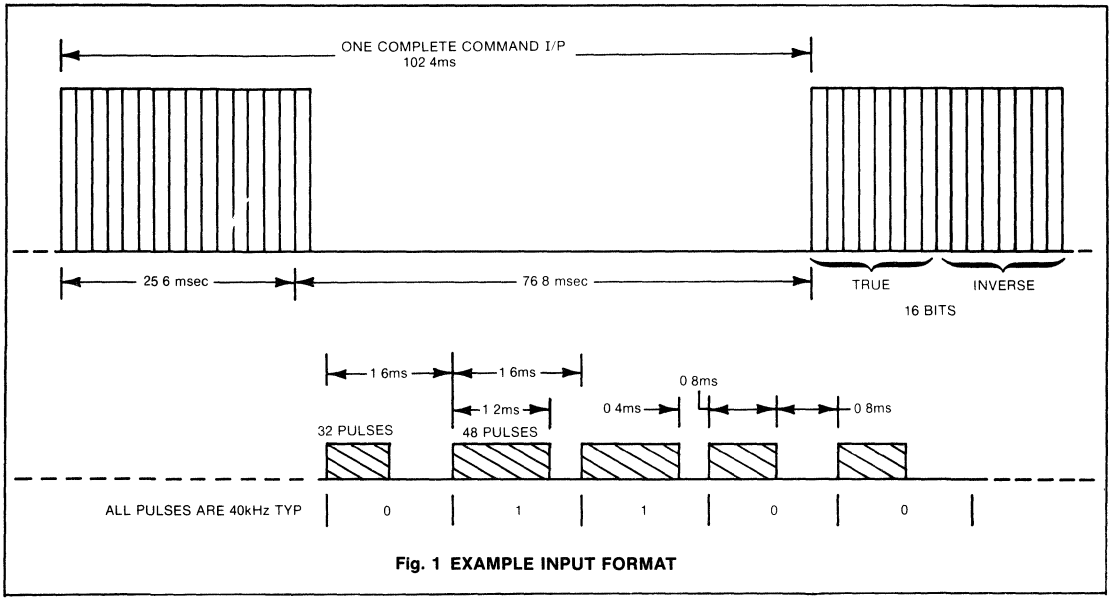


Fig. 1 EXAMPLE INPUT FORMAT

COMMAND DECODING

Transmitted code and Output code (A-H)*	Receiver Functions	Transmitted code and Output code (A-H)*	Receiver Functions
0	Program 1	25	Mute
1	Program 2	26	ON/OFF to OFF
2	Program 3	27	Spare 1 On
3	Program 4	28	Spare 1 Off
4	Program 5	29	Spare 1 Toggle
5	Program 6	30	Spare 2 On
6	Program 7	31	Spare 2 Off
7	Program 8	32	Program 17
8	Program 9	33	Program 18
9	Program 10	34	Program 19
10	Program 11	35	Program 20
11	Program 12	36	Program 21
12	Program 13	37	Program 22
13	Program 14	38	Program 23
14	Program 15	39	Program 24
15	Program 16	40	Program 25
16	Volume Increase	41	Program 26
17	Volume Decrease	42	Program 27
18	Color Increase	43	Program 28
19	Color Decrease	44	Program 29
20	Brightness Increase	45	Program 30
21	Brightness Decrease	46	Program 31
22	Spare Increase	47	Program 32
23	Spare Decrease	48-255	Spare
24	Normalize		

*Decimal equivalent of 8 bit binary word is listed for convenience.

Command 'Outputs' appear approximately 120μs after the last bit of the 16 bit word has been input to the receiver Analog commands may be up to a maximum of 180μs For the case of Local commands the outputs appear approximately 16μs after the 20ms debounce strobe. Analog commands may be up to a maximum of 70μs.

Analog Outputs

The Analog outputs are variable mark space ratio outputs at a frequency of typically 20kHz. The mark space ratio defines the analog level and can be varied from 1:62 to 62:1. Power on reset sets the outputs to mark space of 32.31 Analog outputs 2 to 4 can also be set to 32:31 with the Normalize command Analog output 1 (Volume) can be muted.

Remote commands cause analog channels to increment or decrement at the transmitter repetition rate. For local commands the rate will be approximately ten steps per second.

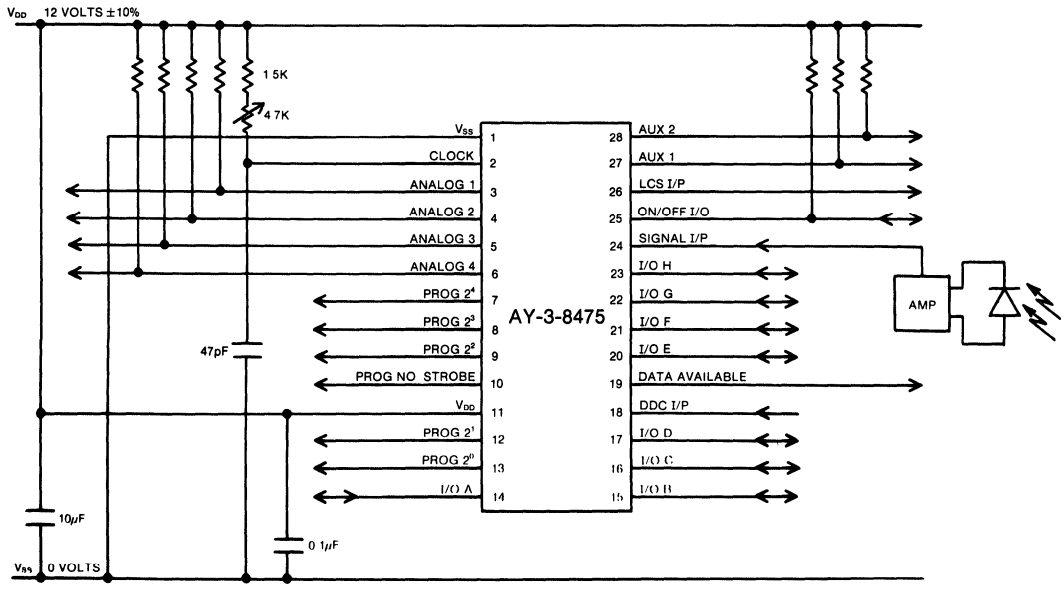


Fig. 7 BASIC SYSTEM SCHEMATIC

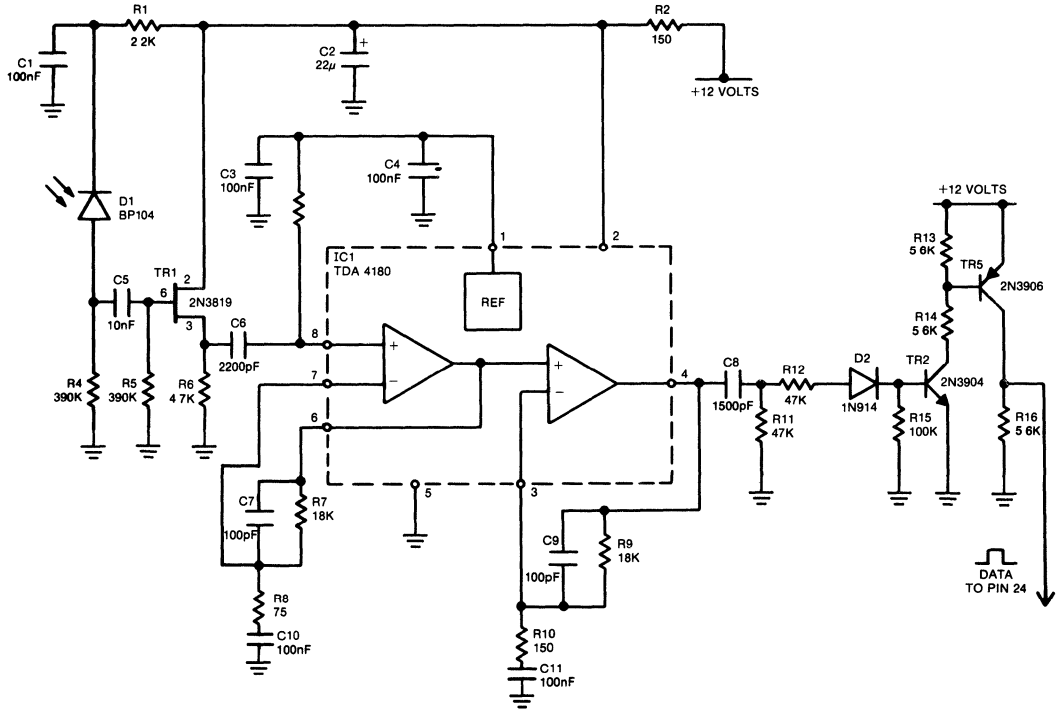


Fig. 8

Local Commands

Local Command Strobe input low converts I/O's A-H to input mode and after a debounce period of 20ms the local data is read in, decoded, and Data Available set to high. Input data must be 'valid' during the strobe time shown.

Local Command Strobe high outputs this new data on the I/O lines.

Analog functions decrement or increment approximately once every 100ms while the command is input.

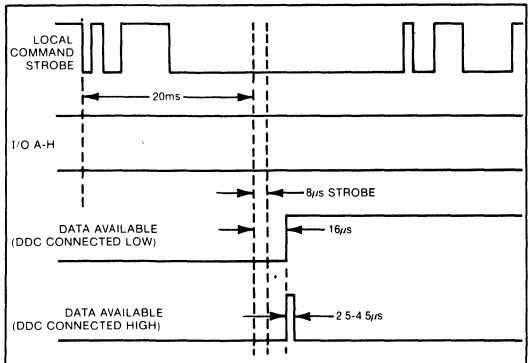


Fig. 2 LOCAL COMMAND TIMING

Program Strobe Output Timing

For the case where the Program Strobe I/O is not connected low externally, then on reception of a Program Command the strobe output will go low for approximately 50ms. The strobe output goes low once only for each Program Command received even though the transmitter is repeating the command. The transmitter key must be released for at least 0.5 sec. (at typical receiver frequency) before a further Program Command can be received.

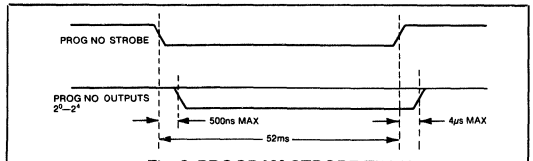


Fig. 3 PROGRAM STROBE TIMING

Interface with CPU Databus

The receiver interfaces directly with the General Instrument Teleview System, Teletext and Viewdata. Interface with any CPU is possible however.

(a) Remote Control has exclusive use of the data bus. Data Available I/O and Digital Data Control input are connected together. Data Available high signals the CPU, the CPU reads in the data and then pulls Data Available and Digital Data Control input low for a minimum of 3μs. Data Available is now reset low If the CPU does not reply to the Data Available the next remote command received will reset Data Available low and then back again to high.

(b) The remote control outputs share a databus with other peripherals. Data Available to high signals the CPU, the CPU sets the Digital Data Control Input high which outputs the remote control data onto the bus. Data is now read and then the CPU resets Digital Data Control Input low which resets Data Available to low. If the CPU does not reply then the next remote transmission resets Data Available back to low and then high.

(c) With Digital Data Control input held high, Data is output on the bus permanently. At each command Data Available pulses high to act as a strobe for loading auxiliary latches.

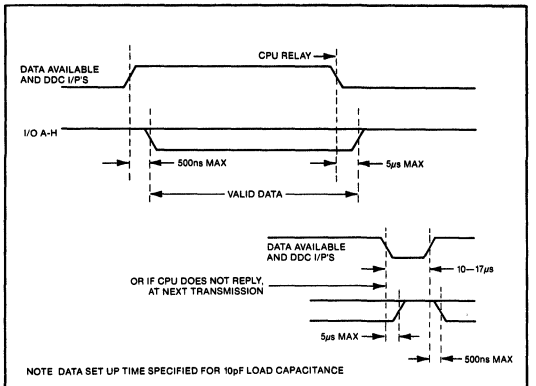


Fig. 4 INTERFACE WITH C.P.U. DATABUS

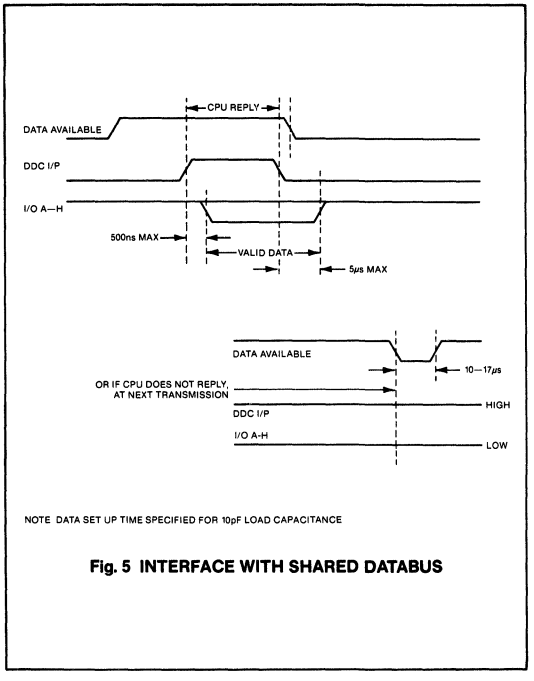


Fig. 5 INTERFACE WITH SHARED DATABUS

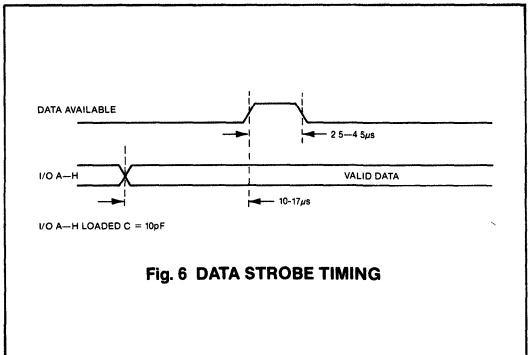


Fig. 6 DATA STROBE TIMING

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} Pin ..... +3.0 to +16V
Ambient Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

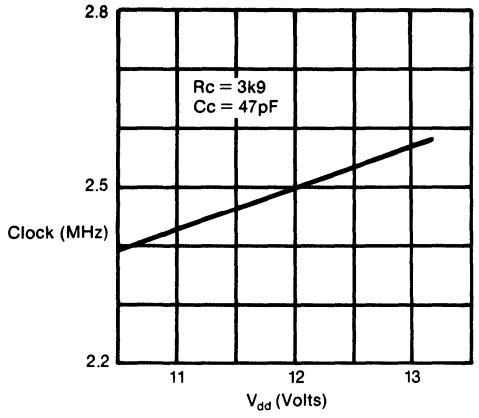
Standard Conditions (unless otherwise noted)

V_{DD} = +12 Volts ±10% (10 8 to 13.2)
V_{SS} = 0 Volts
Operating temperature T_A = 0°C to +70°C

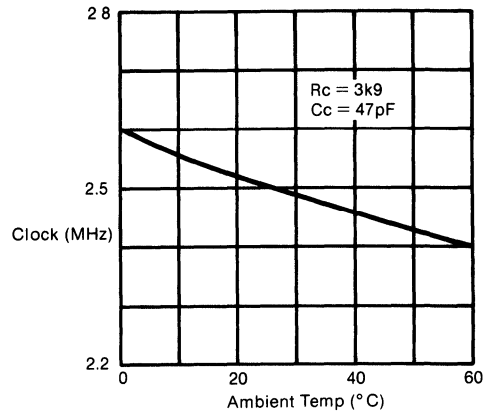
Characteristic	Min	Typ	Max	Units	Conditions
Clock (2)					
Frequency	1 5	2.5	2.8	MHz	Note 2
External resistor to V_{DD}—R_C	1.2	3.9	—	KΩ	
External capacitor to V_{SS}	—	47	250	pF	
Local Command Strobe (26) Input					
Low Level	V_{SS}	—	0.8	V	
High Level	2 2	—	V_{DD}	V	
Pull up to V_{DD}					
Low Level Source	—	—	300	μA	V_{IN} = 0.4 Volts
High Level	2 4	—	—	V	I_{SOURCE} = 30μA
Digital Data Control Input (18)					
Low Level	V_{SS}	—	0.8	Volts	
High Level	3.0	—	V_{DD}	Volts	
Pull-up to V_{DD}					
Low Level Source	—	—	300	μA	V_{IN} = 0.4V
High Level Source	3 2	—	—	Volts	I_{SOURCE} = 20μA
Signal Input (24)					
Low Level	V_{SS}	—	0.8	V	
High Level	3.0	—	V_{DD}	V	
Leakage to V_{SS}	—	—	10	μA	V_{IN} = V_{DD}
Input/Output A-H (14-17 and 20-23)					
Input Low Level	V_{SS}	—	0.8	V	
Input High Level	2 2	—	V_{DD}	V	
Pull-up to V_{DD}					
Low Level Source	—	—	300	μA	V_{IN} = 0.4 Volts
High Level	2.4	—	—	V	I_{SOURCE} = 30μA
Output Low Level	—	—	0 5	V	I_{SINK} = 1.6mA
Output High Level	As above Pull Up High Level				
Program No Outputs (7-9 and 12, 13)					
Low Level	—	—	0 5	V	I_{SINK} = 1.6mA
High Level	2.4	—	—	V	I_{SOURCE} = 30μA
Outputs 'OFF' Pull Up to V_{DD}					
Low Level Source	—	—	300	μA	V_{IN} = 0.4 Volts
High Level	As above Output High Level				
Program No Strobe I/O (10)					
Input Low Level	V_{SS}	—	0.8	V	
Input High Level	3 0	—	V_{DD}	V	
Pull up to V_{DD}					
Low Level Source	—	—	300	μA	V_{IN} = 0.4 Volts
High Level	8	—	—	V	I_{SOURCE} = 10μA
Output Low Level	—	—	0 5	V	I_{SINK} = 2mA
Output High Level	As above Pull Up High Level				
Strobe Duration	40	52	70	ms	
Analog Outputs (3-6)					Open Drain
Frequency	15	20	25	kHz	
Low Level	—	—	0 5	V	I_{SINK} = 2mA
OFF Leakage to V_{SS}	—	—	10	μA	V_{OUT} = V_{DD}

Characteristic	Min	Typ	Max	Units	Conditions
Data Available Output (19)					
Low Level	—	—	0.5	V	$I_{SINK} = 1.6mA$
High Level	2.4	—	—	V	$I_{SOURCE} = 30\mu A$
Aux 1 and Aux 2 Outputs (27, 28)					
Low Level	—	—	0.5	V	$I_{SINK} = 2mA$
OFF Leakage to V_{SS}	—	—	10	μA	$V_{OUT} = V_{DD}$
ON/OFF I/O (25)					
Input Low Level	V_{SS}	—	0.8	V	
Input High Level	3.0	—	V_{DD}	V	
Output Low Level	—	—	0.5	V	$I_{SINK} = 2mA$
OFF Leakage to V_{SS}	—	—	10	μA	$V_{OUT} = V_{DD}$
Supply Current V_{DD} (11)	—	—	50	mA	at 70° C and $V_{DD} = 13.2V$

NOTES:
1. Pull Up's are configured with Depletion FET's with Gate connected to Source. They have non-linear VI characteristics.
2. System compatibility with the AY-3-8470 infra-red transmitter guaranteed for this range of frequencies.



TYPICAL CLOCK VERSUS V_{dd} @ 25°C



TYPICAL CLOCK VERSUS TEMPERATURE FOR V_{dd} = 12 VOLTS

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	0 Volts. Source/substrate connection.
2	Clock	Connect a resistor to V_{DD} and a capacitor to V_{SS}. Nominal frequency 2.5MHz.
3	Analog Output 1	Open drain pulse width modulated outputs. Mark space ratio variable from 1:62 to 62:1. Outputs increment one step for each command received. Increment rate approximately one step every 100ms for continuous commands.
4	Analog Output 2	
5	Analog Output 3	
6	Analog Output 4	
7	2^4 Program No Output	Outputs under control of the Program StrobeI/O. Program 1 = 00000. With Program StrobeI/O connected low, latched program data is available.
8	2^3 Program No Output	
9	2^2 Program No Output	
12	2^1 Program No Output	
13	2^0 Program No Output	
10	Program Number StrobeI/O	Goes low for approximately 50ms when program data has been received. While low the Program Number Outputs are enabled. While high the Program Number outputs are all high. When this output is held low externally the Program Number outputs are permanently enabled.
11	V_{DD}	Positive power supply 12 Volts ±10%.
14	I/O A	256 Command data under the control of the Digital Data Control input. A is the LS Bit. Local commands may be entered on the A-H lines under control of the Local Command Strobe Input.
15	I/O B	
16	I/O C	
17	I/O D	
20	I/O E	
21	I/O F	
22	I/O G	
23	I/O H	
18	Digital Data Control Input	When high the 8 outputs A-H are enabled. This input also resets the Data Available output when taken low. When low outputs A-H are all high.
19	Data Available Output	This output is set high when new data is available. It remains high until reset by the Digital Data Control input going low. If the Digital Data Control input is permanently held high then Data Available output is a high going strobe pulse of typically 4μs.
24	Signal Input	This input should normally be low under no signal conditions. High going pulses are input when a remote command is triggered.
25	ON/OFFI/O	Open drain output used for switching 'ON' the television or radio, etc. This output is turned on by any one of the 32 program commands and turned off by the OFF command. The output can be latched on locally by connecting low for at least 128μs. When 'OFF' increment and decrement commands on the Analog channels are inhibited. Connect to 0 volts if not used.
26	Local Command Strobe Input	When low, I/O's A-H are in the input mode and the Signal Input is inhibited. Local commands may now be entered. When high are under control of the Digital Data Control input.
27	Auxiliary Output 1	Open drain outputs, turned on or off as required. In addition Auxiliary Output 1 can be toggled. Remote toggle commands have to be spaced at least 0.5 secs apart similar to the Mute toggle, see later Muting.
28	Auxiliary Output 2	

NOTES

ULAs 8

High Speed CMOS Uncommitted Logic Arrays (ULAs)

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
Uncommitted Logic Arrays			
HIGH SPEED CMOS UNCOMMITTED LOGIC ARRAYS	Single mask, 5ns gate delay, single supply voltage, CMOS technology, on-chip power-on reset.	LA03	8-3
		LA05	8-3
		LA10	8-3
		LA15	8-3
		LA20	8-3

High Speed CMOS Uncommitted Logic Arrays

FEATURES

- Offers advantages of custom design without the development cost or time
- "PC board on a chip" approach allows simple, easy to design technique by customer or General Instrument
- Single mask commitment pattern
- 5ns gate delay
- Single supply voltage (3V to 6V)
- Low power dissipation due to silicon gate CMOS technology
- Available on-chip power-on reset option
- Full design package for customer designs available
- Short turnaround time, typically 6-8 weeks from layout to prototypes

WHAT ARE GENERAL INSTRUMENT ULAs?

The General Instrument Uncommitted Logic Arrays consist of a matrix of pre-processed basic logic and peripheral cells which require only a single layer of metal interconnections to be made into a custom designed circuit

The design process consists of interconnecting, via the extensive interconnection highway, standard cells selected from the comprehensive cell library (Each standard cell being constructed from one or more basic cells) This simple procedure, which requires no special semi-conductor design experience, is similar to printed circuit board layout and may be undertaken either by the customer or by General Instrument

ARRAY DESCRIPTION

The gate array consists of rows of basic logic cells with interconnection highways between each row On the edge of the chip, surrounding the logic cells, are basic peripheral cells with an interconnection highway between the peripheral and the logic cells The peripheral cells buffer signals into and out of the chip See Figure 1.

The customer's circuit is built up using fully characterized standard cells selected from the large, comprehensive cell library Each standard cell is constructed from one or more of the basic logic cells (or from one basic peripheral cell in the case of the standard peripheral cells)

THE GENERAL INSTRUMENT ARRAYS

Type No.	No. of Gates	No. of I/O Pads	Minimum Package Size
LA03	324	32	14
LA05	560	40	16
LA10	950	52	16
LA15	1440	64	22
LA20	2014	76	24

1 gate = 1 basic logic cell
= 2 N-Channel + 2 P-Channel transistors configurable as a dual inverter, 2 input NAND gate, transmission gate etc

Note: Pin count includes 2 power pins.

The cell library includes
- Simple gates (AND, OR, NAND, NOR, exclusive OR etc)
- Latches
- Decoders
- Shift Registers
- Arithmetic Elements
- Input Buffers
- Output Buffers

A complete list of standard cells appears at the end of this data sheet and includes a cross-reference to standard 4000 series CMOS integrated circuits

The interconnection between the standard cells is done in the interconnection highways, each of which can carry up to ten tracks Extensive cross-under facilities are provided in these highways to allow tracks to cross each other in order to connect to the standard cells

The metal interconnections inside standard cells are held on the General Instrument graphics system and are automatically added to the interconnections between the cells at the digitization stage

BASIC LOGIC CELL

The basic logic cell consists of 4 MOS transistors (2 N-Channel and 2 P-Channel) connected together as shown in Figure 2

The gate connections are in polysilicon, are continuous through the cell and are available at the metal contacts both at the top and the bottom of the cell

The two P-Channel transistors each have one common source (drain) and one isolated source (drain) each of which may be connected to the metal contacts at the top of the cell

Similarly the N-Channel transistors have their source and drain at the bottom of the cell

The power supply lines are taken through every cell in metal

The internal connections of the cell (which convert the four separate transistors of one (or more) basic logic cells into a standard cell) are made in metal. See Figure 3.

The interconnections between standard cells are made to the metal contacts at the top and bottom of the cells

BASIC PERIPHERAL CELL

The basic peripheral cell consists of an input section and an output section See Figure 4

The input section has two MOS transistors (one N- and one P-Channel) connected to form an inverter A resistor in series with the gates plus two catching diodes gives input static protection A 2kΩ and a 15kΩ pull-up resistor are available which may be, optionally, connected to the input

The output section also has two MOS transistors (one N- and one P-Channel) which may be connected to form either an open drain, totem pole or tri-state output stage Two catching diodes are provided to give output static protection

The peripheral cell also has a bonding pad which is linked, inside the cell, to the input and/or output sections and is the point to which the external bond wires to the chip are connected

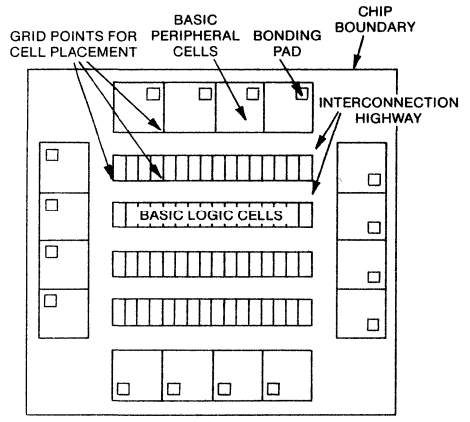


Fig.1 BASIC GATE ARRAY LAYOUT

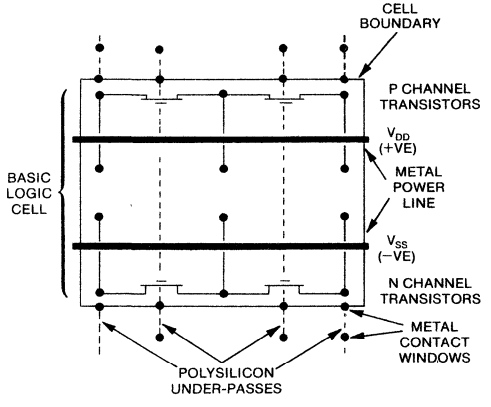


Fig. 2 BASIC LOGIC CELL SCHEMATIC

INTERCONNECTION HIGHWAY

The interconnection highways between the rows of cells can accommodate up to ten tracks. See Figure 5

Connections across the highway may be made via the polysilicon underpasses as shown in Figure 5, where track 7 (marked start) is connected via the underpasses (which pass under tracks 1 to 6) to the contact window (marked end)

Connections are made between the metal tracks and the polysilicon underpasses only at the contact windows.

DESIGN PROCESS

Designing with the General Instrument ULAs is no more complicated than designing in 4000 series CMOS or 7400 series TTL. Instead of a CMOS or TTL data book, the reference is the extensive General Instrument cell library of fully characterized logic and peripheral cells Choosing the appropriate element is as easy as looking up a CMOS catalog for the desired gate. If the design is already in standard CMOS, a quick cross-reference to the nearest equivalent in the ULA library is provided.

Once logic design is complete, the design process is reduced to one which very closely resembles a PC board layout and wiring operation. General Instrument provides a sheet of temperature-stable mylar material with the cell placement grid and polysilicon underpasses drawn on it at a scale of 250:1. A portion of the grid is shown in Fig. 6.

In addition to the grid, adhesive backed logic decals are available from General Instrument for each of the library cells. Cell placement simply involves choosing the correct decal and locating it on the grid by aligning the registration marks on the decal with those on the grid. Fig. 6 also illustrates this process and Fig. 7 shows examples of the decals. As can be seen, the decals are drawn at the logic symbol level, no transistor-level information is provided, nor is it necessary for interconnecting one cell with another. The only other information available from the decals is the position of the input and output connections. When properly aligned with the grid registration points, these inputs and outputs appear precisely at the correct polysilicon underpasses.

Interconnections between cells are made by drawing metal tracks in the spaces provided in the interconnection highway or, alternatively, placing tape between the appropriate contacts Tape of the correct width is provided in the General Instrument design package and offers a better solution than pencil since it leaves no residual marks when removed.

This "PC board on a chip" concept makes for a highly flexible design technique and one which is ideal for customer designs since MOS knowledge and transistor-level acquaintance with the array layout are not prerequisites for undertaking a design.

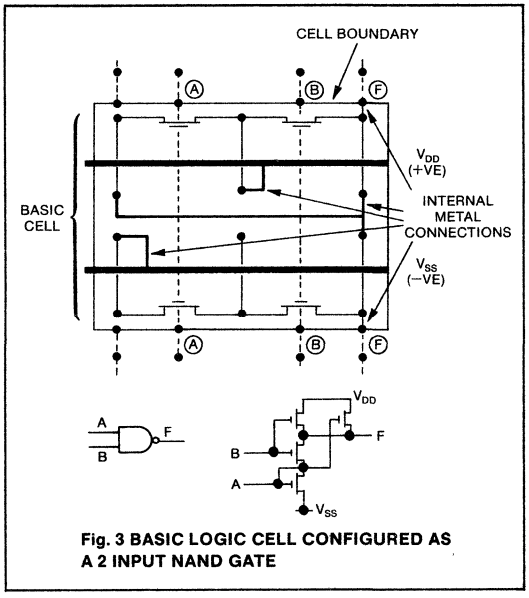


Fig. 3 BASIC LOGIC CELL CONFIGURED AS A 2 INPUT NAND GATE

As an alternative to the manual design method described, a Computer Aided Design (CAD) technique is available from General Instrument. This approach facilitates ease and speed of design through the use of a Calma compatible software data base containing all necessary design information.

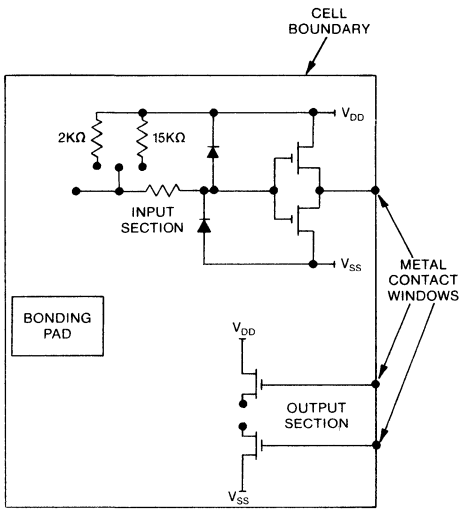


Fig. 4 BASIC PERIPHERAL CELL SCHEMATIC

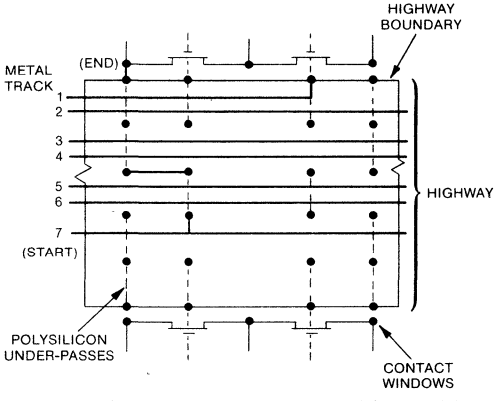


Fig. 5 INTERCONNECTION HIGHWAY SCHEMATIC

CUSTOMER INTERFACES

There are three possible design routes which may be taken up to the prototype stage

I) General Instrument designs the ULA from the customer's logic diagram This interfacing route will follow the flow chart of Figure 8

II) Customer designs in ULA format as shown in Figure 9

III) Customer takes design through layout General Instrument's involvement begins at the Digitization stage prior to mask generation Figure 10 defines this design route

Variations on these basic design routes are possible in consultation with General Instrument

AVAILABLE FROM GENERAL INSTRUMENT

1 Data sheets and brief explanation of ULA design procedures

2 Detailed specification and design manual

3 Full design package including
- Cell library of fully characterized logic elements with complete electrical specification for each cell
- Mylar layout grid
- Set of logic decals
- Interconnection tape
- Calma data base

4 Training and advice on design procedures and interpretation of logic simulation results

5 Complete design capability

BUDGETARY QUOTATIONS

To enable General Instrument to perform a realistic appraisal of a proposed ULA design, the following information, at a minimum, must be supplied

1 A clearly defined logic diagram of the proposed ULA chip with a brief description of its operation

2 An electrical specification for important parameters including operating voltage range

3 Temperature range of operation

4 I/O definition and input/output impedances

5 Required package type

6 Proposed prototype delivery date.

7 The level of customer involvement, that is, which of the three design routes will be followed

8 Intended production volume

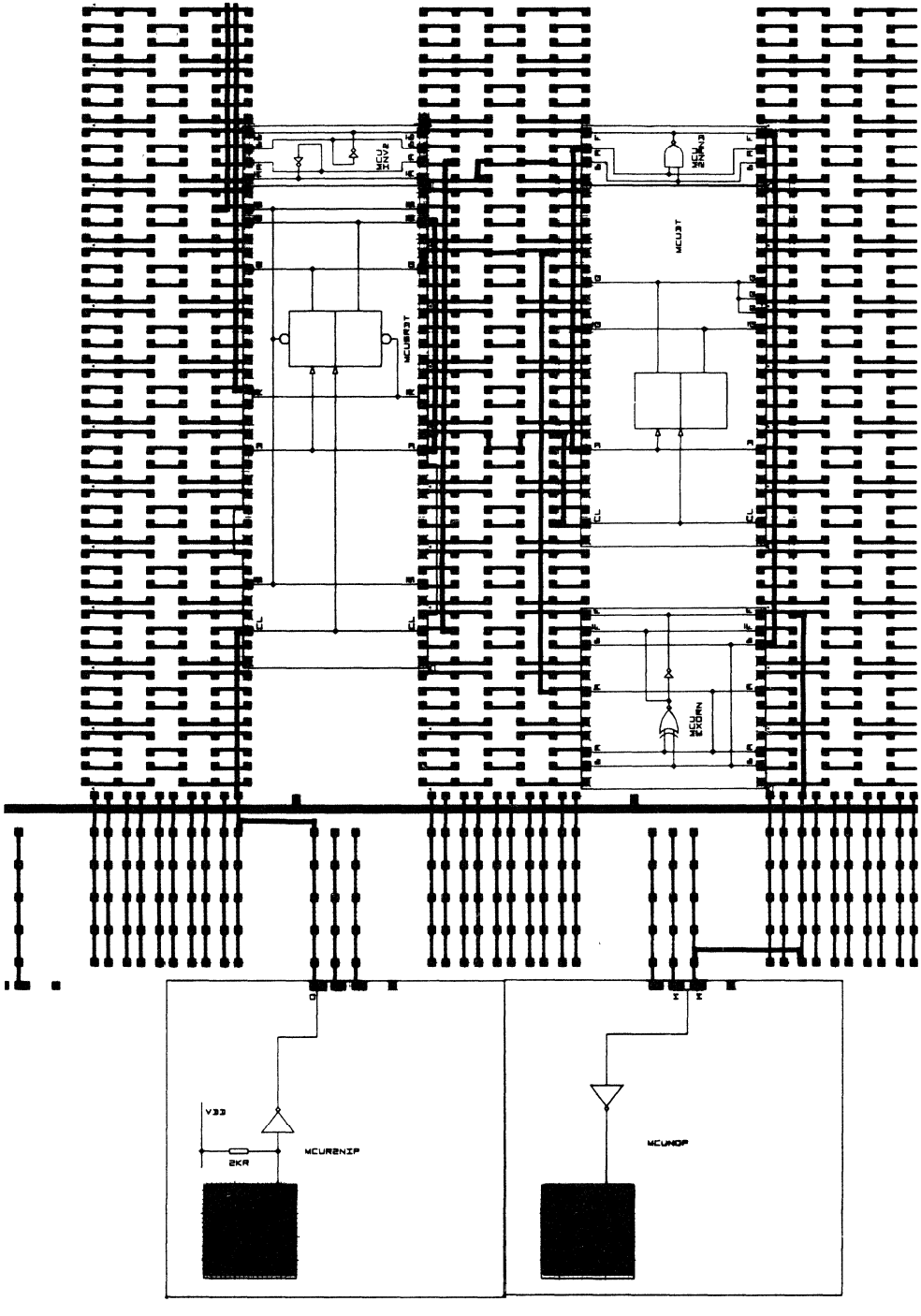
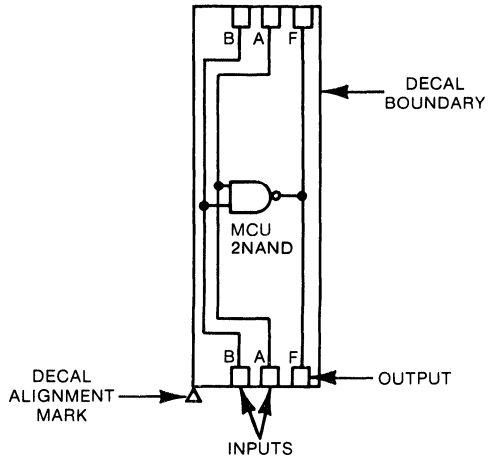
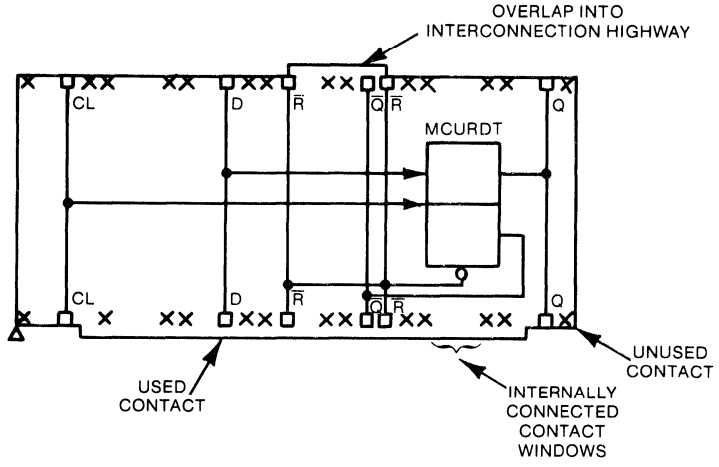


Fig. 6 SECTION OF TYPICAL LAYOUT

(a)



(b)



(c)

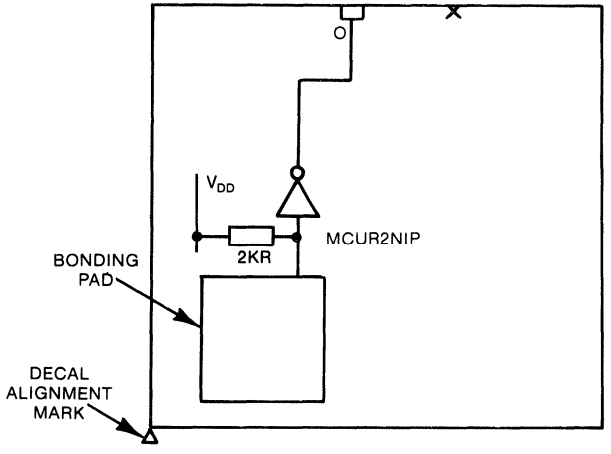


Fig. 7 TYPICAL LAYOUT DECALS

PROCEDURE I GENERAL INSTRUMENT DESIGNS ULA

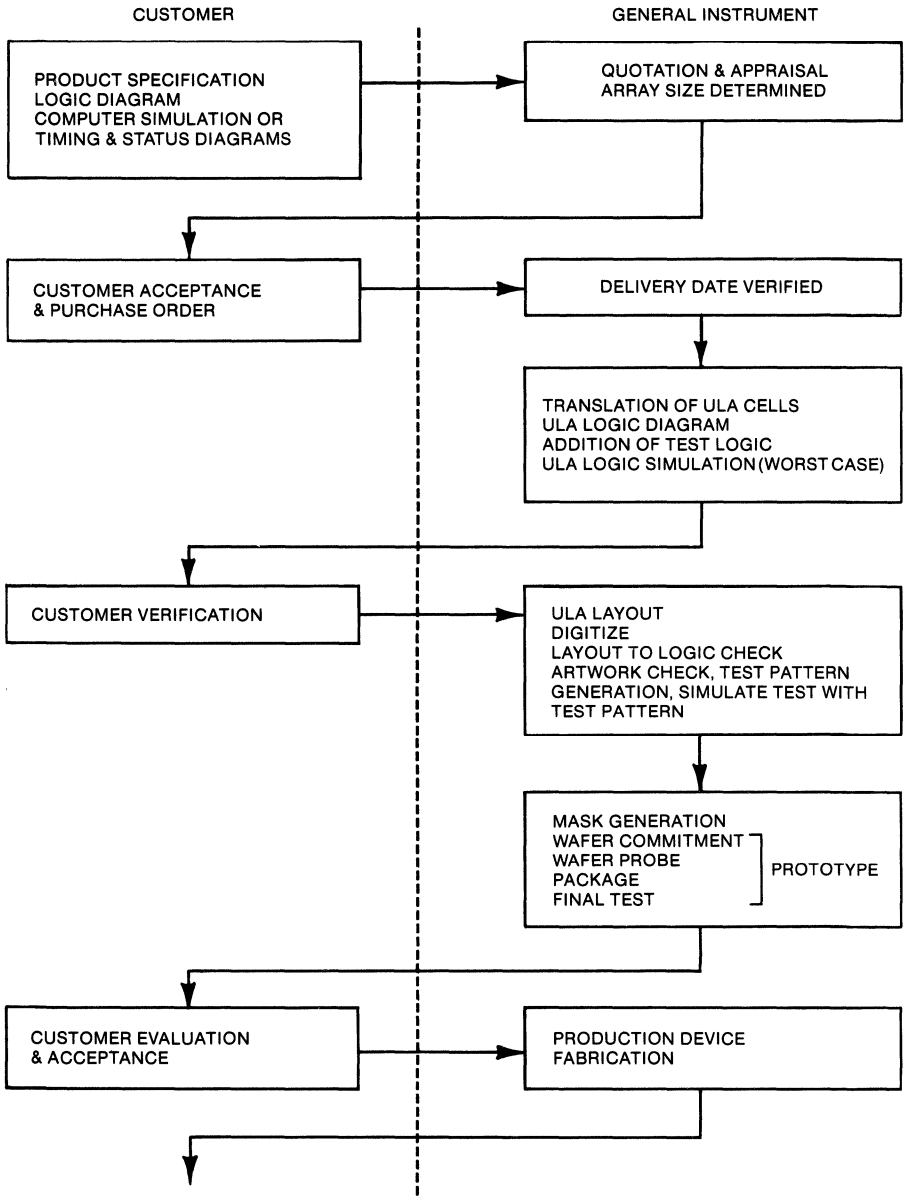


Fig. 8 DESIGN INTERFACE

PROCEDURE II CUSTOMER DESIGNS IN ULA FORMAT

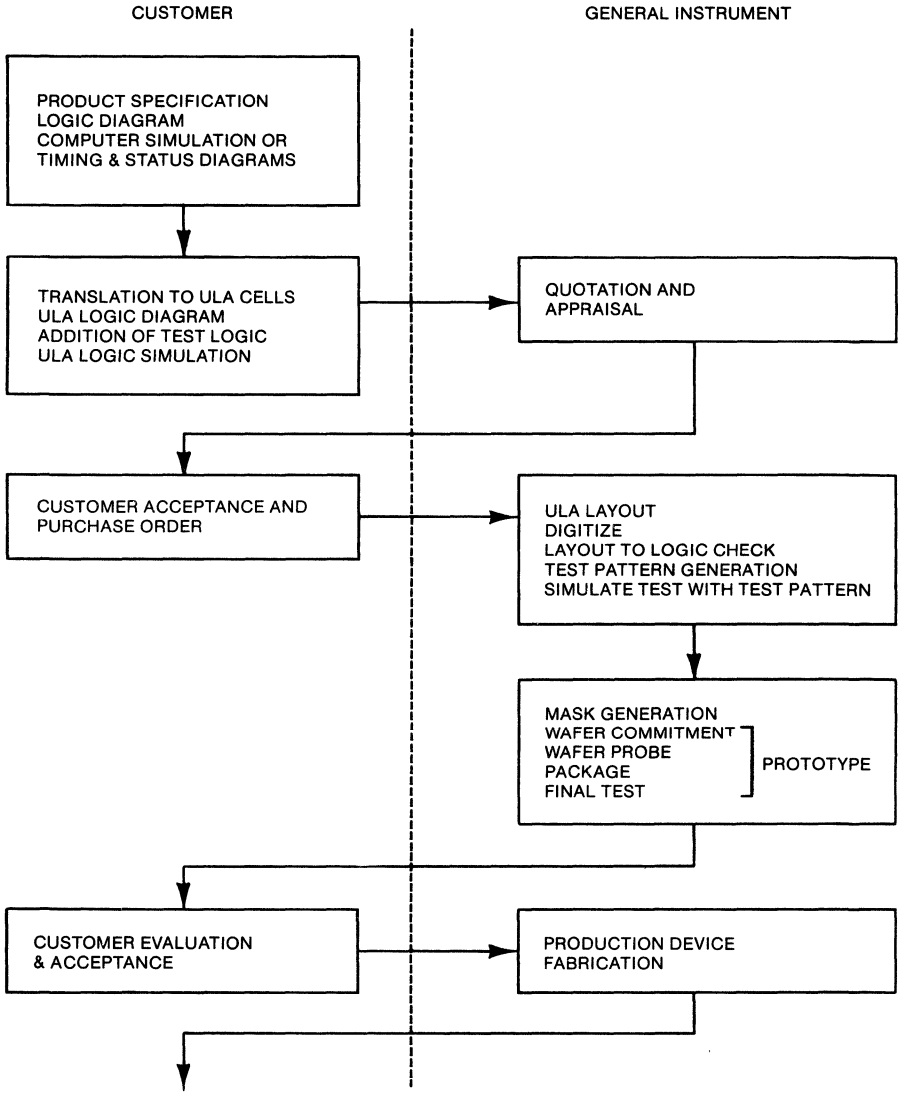


Fig. 9 DESIGN INTERFACE

PROCEDURE III CUSTOMER DESIGNS ULA

(a) GENERAL INSTRUMENT DIGITIZES (b) CUSTOMER DIGITIZES

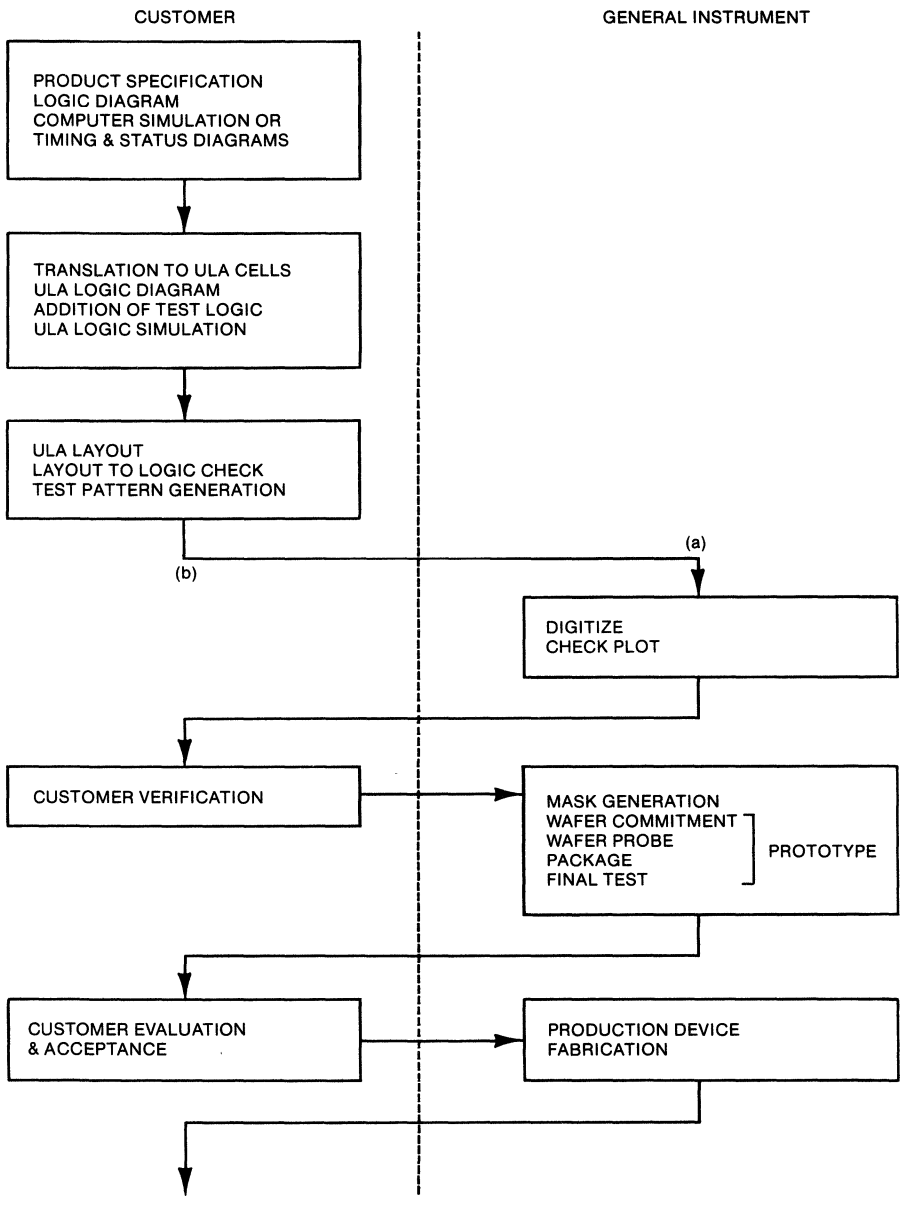


Fig. 10 DESIGN INTERFACE

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to GND) .....−0 3V to 7V
Storage Temperature ..... −65° C to +150° C
Operating Temperature ..... −55° C to +125° C
Soldering Temperature of leads (10 seconds) ..... +300° C

Standard Conditions (unless otherwise stated)·

Operating Voltage Range +3V to +6V
Operating Temperature Range 0° C to +70° C
−40° C to +85° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied — operating ranges are specified in Standard Conditions Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

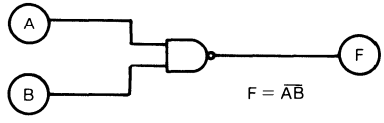
Data labeled "typical" is presented for design guidance only and is not guaranteed

Typical gate delay at 25° C and +5V is 5ns However, the characteristics of each logic element are specified independently for each of the library cells Two examples are shown below

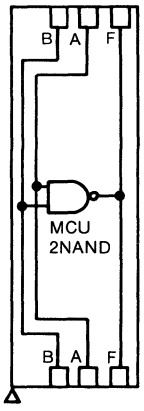
CELL LIBRARY SPECIFICATIONS

EXAMPLE 1:

2 INPUT NAND GATE (MCU2NAND)



LOGIC

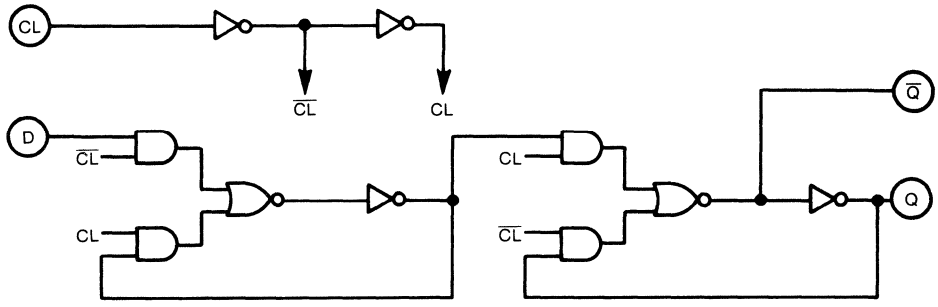


BLOCK SCHEMATIC

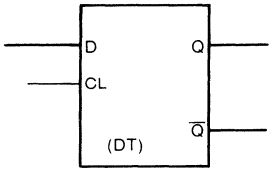
Characteristics	Min	Typ	Max	Units	Conditions
Propagation Delay Time					
High to Low Level	—	0	0	ns	
Propagation Delay Time					
Low to High Level	—	0	0	ns	
Transition Time					
High to Low Level	—	4	5 2	ns/pF	
Transition Time					
Low to High Level	—	4 5	5 8	ns/pF	
Input Capacitance	—	35	.5	pF	
Inherent Output Capacitance	—	7	9	pF	

EXAMPLE 2:
D-TYPE FLIP-FLOP (MCUDT)

LOGIC



POSITIVE EDGE TRIGGERED FLIP-FLOP

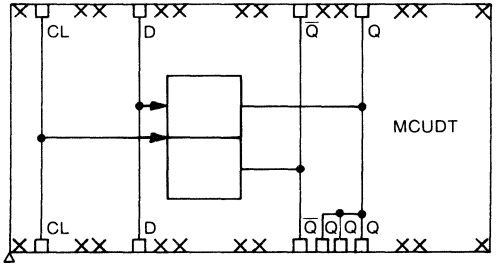


TRUTH TABLE

IN		OUT	
CL	D	Q	$\overline{Q}$
↗	0	0	1
↗	1	1	0
↘	X	Q	$\overline{Q}$

NO CHANGE

BLOCK SCHEMATIC



Characteristics	Min	Typ	Max	Units	Conditions
Propagation Delay Time: Clock to Q	—	20	34	ns	
Clock to $\overline{Q}$	—	7	12	ns	
Transition time					Note 1
High to Low Level Q	—	2.0	2 6	ns/pF	
$\overline{Q}$	—	4 0	5 4	ns/pF	
Low to High Level Q	—	4.5	5 8	ns/pF	
$\overline{Q}$	—	9	11 7	ns/pF	
Clock Input Frequency (Q & $\overline{Q}$ Unloaded)	dc	—	17	MHz	
Data Set Up Time	30	—	—	ns	
Data Hold Time	12	—	—	ns	
Clock Rise or Fall Time	—	—	1000	ns	
Input Capacitance. Node CL	—	35	5	pF	
D	—	35	5	pF	
Inherent Output Capacitance: Node Q	—	85	1 1	pF	Note 2
$\overline{Q}$	—	1 35	1 8	pF	

NOTES.
1. If $\overline{Q}$ is loaded total propagation delay time to Q = propagation delay time to Q + additional transition time to $\overline{Q}$.
2. If Q or $\overline{Q}$ has to drive a switched load (eg. D input to MCUTRI) then outputs must be buffered with inverter cell.

STANDARD CELL LIST

Cell Description	Cell Name	No. of Gate Equivalents	Nearest CMOS Equivalent
Gates			
Inverter Fast	MCUINV1	1	4069
Dual Inverter	MCUINV2	1	4069
21P NAND Gate	MCU2NAND	1	4011
21P NAND/AND Gate + Inverter	MCU2AND	2	4018
31P NAND/Gate + Inverter	MCU3NAND	2	4023
31P NAND/AND Gate	MCU3AND	2	4073
41P NAND Gate	MCU4NAND	2	4012
41P AND/NAND Gate + Inverter	MCU4AND	3	4082
21P NOR Gate	MCU2NOR	1	4001
21P NOR/OR Gate + Inverter	MCU2OR	2	4071
31P NOR Gate + Inverter	MCU3NOR	2	4025
31P NOR/OR Gate	MCU3OR	2	4075
41P NOR Gate	MCU4NOR	2	4002
41P NOR/OR Gate + Inverter	MCU4OR	3	4072
2 AND 2 NOR Gate	MCU2ANNO	2	4085
2 AND NOR/OR Gate + Inverter	MCU2ANOR	3	4019
Transfer (Tri-State) Gate + Inverter	MCUTRI	2	4070
Exclusive OR/NOR Gate	MCUEXORN	3	4077
Arithmetic			
Half Adder + Inverter	MCUHAD	4	
Full Adder	MCUFAD	7	4008
Registers & Latches			
Set-Reset D Type Flip Flop	MCUSRDT	8	4013
Reset D Type Flip Flop	MCURDT	7	4013
Set D Type Flip Flop	MCUSDT	7	4013
D Type Flip Flop	MCUDT	6	4013
Set-Reset D Latch	MCUSRDL	5	
Reset D Latch	MCURDL	4	
Set D Latch	MCUSDL	4	
D Latch	MCUDL	4	4042
NOR S/R Latch	MCUNOSR	3	4043
NAND S/R Latch	MCUNASR	3	4044
D Register (First Bit)	MCUDREGF	5	
D Register (Middle Bit) Dual	MCUDREGM	5	4042
D Register (End Bit)	MCUDREGE	3	
Shift Register (First Bit)	MCUSHRF	10	
Shift Register (Middle Bit)	MCUSHRM	5	4015
Shift Register (End Bit)	MCUSHRE	5	
Half Parallel Loading Shift Reg Clock Drivers	MCUHPLSF	8	
Half Parallel Loading Shift Reg First and Middle Bit	MCUHPLSM	7	4021
Half Parallel Loading Shift Reg End Bit	MCUHPLSE	7	
Decoders			
Expandable 7-Segment Decode Segment a	MCU7SGA	7	
Expandable 7-Segment Decode Segment b	MCU7SGB	7	
Expandable 7-Segment Decode Segment c	MCU7SGC	5	
Expandable 7-Segment Decode Segment d	MCU7SGD	8	4055
Expandable 7-Segment Decode Segment e	MCU7SGE	5	
Expandable 7-Segment Decode Segment f	MCU7SGF	8	
Expandable 7-Segment Decode Segment g	MCU7SGG	8	
Service Elements			
2 Row Interconnect	MCU2INT	1	
Peripheral			
Input Buffer Inverting	MCUNIP		
Input Buffer Inverting with 15kΩ Pull Up Resistor	MCURINIP		
Input Buffer Inverting with 2kΩ Pull up Resistor	MCUR2NIP		
Output Buffer Inverting	MCUNOP		
Output Buffer Inverting Open Drain	MCUODNOP		
Tri-State Output Buffer plus Inverting Input Buffer	MCU3IO		
Dummy Pad	MCUDUM		

NOTES

Video 9

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
		Video Display	
TELEVIEW SYSTEM	The Teleview system is a powerful system to display information on a TV receiver. It can store data from either telephone lines or TV RF signal information.	TELEVIEW System	9-4
		PIC1650A	9-9
		PIC1650-536	9-15
		AY-3-9710	9-28
		AY-3-9735	9-33
		Video Graphics	
PERSONAL TERMINAL	The 8900 system is a programable video display system, capable of detailed graphics definition and manipulation.	General Information	9-42
		CP1610	9-22
		AY-3-8900	9-43
		AY-3-8900-1	9-43
		RO-3-9502	9-46
		RO-3-9503	9-49
		RO-3-9600	9-51
		RO-3-9504	9-54
		AY-3-8910	9-56
		AY-3-8912	9-56
		AY-3-8913	9-56
		AY-3-8915	9-57
		Video Games	
BALL & PADDLE	Six selectable games for one or two players, with vertical paddle motion.	AY-3-8500	9-60
		AY-3-8500-1	9-60
8600 SERIES	The 8600 series games consist of a set of single chip TV game integrated circuits.	General Information	9-63
ROADRACE	One or two player games where racing skill in "traffic" generates the highest score.	AY-3-8603	9-64
WARFARE	One or two player games featuring subs, destroyers, cargo ships, and spaceships.	AY-3-8605	9-65
WIPEOUT	One or two player games where players "wipe out" objects by controlling a ball in the play area.	AY-3-8606	9-66
SHOOTING GALLERY	Twelve games for one or two players using external photocell rifles for shooting.	AY-3-8607	9-68
SUPERSPORT	Ten selectable games for one or two players, with vertical and horizontal paddle motion.	AY-3-8610	9-70
MOTOR CYCLE	One player cycle game with variable skill selection.	AY-3-8765	9-72

GENERAL INSTRUMENT

Video Display

	DESCRIPTION	PART NUMBER	PAGE NUMBER
TELEVIEW SYSTEM	The Teleview system is a powerful system to display information on a TV receiver. It can store data from either telephone lines or TV RF signal information.	TELEVIEW System	9-4
		PIC1650A	9-9
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GENERAL INFORMATION

INTRODUCTION

Teletext and Viewdata are the generic names for two basically similar systems for displaying pages of information on a TV screen

Teletext (otherwise known as Ceefax, Oracle, Videotext).

In the Teletext system the data is coded onto normally unused lines of a television transmission It has the following features.

(a) Being a broadcast system, the data flow can be one way only. 'Pages' of data are sent continuously, on a rotating basis. The decoder will grab the required page as it passes.

(b) The number of spare TV lines is limited. For a reasonable access time the data bank is restricted to 100-800 pages per channel.

(c) Being broadcast the data may be 'live', it may update very rapidly and everyone receives the data simultaneously. Sub-titles and newsflashes are good examples of live data.

Viewdata (otherwise known as Prestel, Bildschirmtext)

In the Viewdata system the decoder is connected to the users telephone line and uses the public telephone network in order to transmit information to and from a computerized data bank It has the following features.

(a) There is a direct and individual connection to the user and the data flow may be two way The user thus requests the page he wants directly.

(b) The data bank may be as large as desired, there are no system limitations.

(c) Being an individual connection the service may be a personal one and the data content may reflect this, and may indeed be restricted to a selected group of users

TELEVIEW

Teleview is a General Instruments' 3 chip integrated circuit kit which forms the basis of an inexpensive, comprehensive Viewdata and Teletext system.

Other optional circuits provide additional features such a Infra Red Remote Control, Viewdata modem, Autodialer and Terminal identifier, and various TV Digital Tuning Systems

The kit provides switchable Viewdata or Teletext operation with automatic selection of "on" and "off hours" operation. Provision has been made for addressing up to 8 pages of memory thus giving great flexibility and economy of operation.

The system is organized around parallel Data and Address highways, this allows easy expansion of the system and the connection of other equipment such as Home Computers and Disc Memories.

A single chip microcomputer is used to control the system and to interface to the user The microcomputer allows easy alteration of the system features enabling manufacturers to have personalized systems if desired

As far as possible adjustable and critical components have been eliminated and the circuitry has been designed to facilitate the use of single sided printed circuit boards.

TELEVIEW FEATURES

- Switchable Viewdata — Teletext, 625 line system with 24 rows of 40 characters
- Up to 8 page stores
- Microcomputer controlled, gives system flexibility
- Data bus organization for easy system expansion
- On/Off hours operation
- Don't care digit feature in Teletext
- Half page expansion feature
- Black/White output for Monochrome TV and Printers
- Special Graphics feature for high resolution
- Boxed clock capability in Teletext
- Selectable character rounding
- Simple printed board layout
- 4 x 4, ASCII, REMOTE Keyboard options
- Low power consumption typically +12V at
  +12V at 100mA
  + 5V at 400mA
  − 5V at 10mA
  } for a single page store

SYSTEM DESCRIPTION

The system consists of four basic blocks.

(a) Data Acquisition
This block acquires data from either the TV IF (Teletext) or the telephone line (Viewdata) and after verification passes it to the Page Store

(b) Page Store
The page store, of which there may be up to 8, is the repository for the information to be displayed. It is written into by the Data Acquisition block and read by the Video Generator.

(c) Video Generator
The Video Generator reads the information in the store, decodes it into a dot pattern and outputs video signals to TV tube.

The information to be displayed is chosen by the user via the Controller

(d) Controller
The Controller (which is a single chip microcomputer) is primarily the interface between the operator and the system.

Fig. 1 shows a typical complete system broken up into the blocks described.

An important feature to note is the way that each block in the system communicates to the others by means of a 10 bit Address highway and an 8 bit Data Highway The interchange of data is controlled by the signals TS1 and TS2 which are provided by the Video Generator.

KEY FUNCTIONS

Picture Text—Repeated operation of this key switches the system between Picture and Text modes

Mix—Repeated operation of this key switches the system between Mix and Normal modes. In the Mix Mode Captions, Subtitles and Newsflashes are inset into the picture.

Half Page—Repeated operation of this key cycles the system from Normal to Upper Half Expanded to lower Half Expanded back to Normal. Operation of the P key restores Normal Mode

Store Select—Operating Store Select and Digit 1-8 selects a new store for display (assuming that more than one is provided).

Box Clock—Operation of this key when in Picture Mode causes the Clock to be Boxed into the picture in Double Height Characters. A second operation cancels the command.

Hold—Operation of this key will hold displayed the current one of a set of rotating pages. If more than one store is provided the remainder of the set will be automatically stored in the unselected stores. In Viewdata mode it disconnects the Telephone line.

Reveal—Repeated operation of this key Reveals and Conceals concealed information.

Update (Clear)—Operation of this key removes the information from the display until the page is updated. A second operation restores the display.

Update (Clear)—Operation of P or Store Select also restores the display (In Viewdata mode this key acts as a Clear)

Roll Headers—Operation of this key starts the Teletext headers rolling.

Cursor OFF } Operation of these keys switch the cursor
Cursor ON } ON and OFF in Viewdata mode.

Rounding OFF—Operation of this key removes the character rounding and inhibits the flashing of characters. Normally used when printing. Reception of a new page or operation of Cursor ON or OFF restores rounding.

P(*) Page No. Key Operation of this key primes the system to accept a 3 digit page number (* in Viewdata mode).

T(#) Time Key. Operation of this key primes the system to accept a 4 digit time code. (// in Viewdata mode).

INITIALIZATION

At Power Up the page stores are cleared and up to 10 characters of text are inserted in the middle of the page.

For PIC1650A-518 TELEVIEW in White is displayed and Picture mode is selected.

For PIC1650A-532 (IR) TELEVIEW in Yellow is displayed and Picture mode is selected.

For PIC1650A-532 (ASCII) TELEVIEW in Cyan is displayed and Picture mode is selected

Page No.X00 is selected to be stored in store 7 (so that the Teletext index is immediately available) (Note: alternative initialization can be provided).

For PIC1650A-519 TELEVIEW in Yellow on Blue is displayed. Text mode and Store 1 are selected.

For PIC1650A-533 TELEVIEW in Yellow on Blue is displayed. Text mode and Store 1 are selected.

PAGE SELECTION

In Teletext mode pages are selected by pressing the P key and entering a page number. Televiev has the ability to accept don't care digits (-) as well as normal digits (0-9). Operation of the Update Key (which has no use at this time) enters the (-) so, if for instance, 1-0 were keyed every tenth page starting at page 100 would be displayed as soon as it was transmitted (approximately at 2 sec intervals).

Operation of the time code Key T terminates the page no entry and fills any unentered page digits as blanks.

The rolling of pages described above can be stopped by pressing Store Select or Hold. If the Hold key is pressed and more than one store is provided subsequent pages will automatically be stored. The P key will also stop rolling but the page may be erased.

Page selection may also take place in the Picture mode in which case the page header will be boxed (in double height characters) for 5 seconds after each digit is pressed.

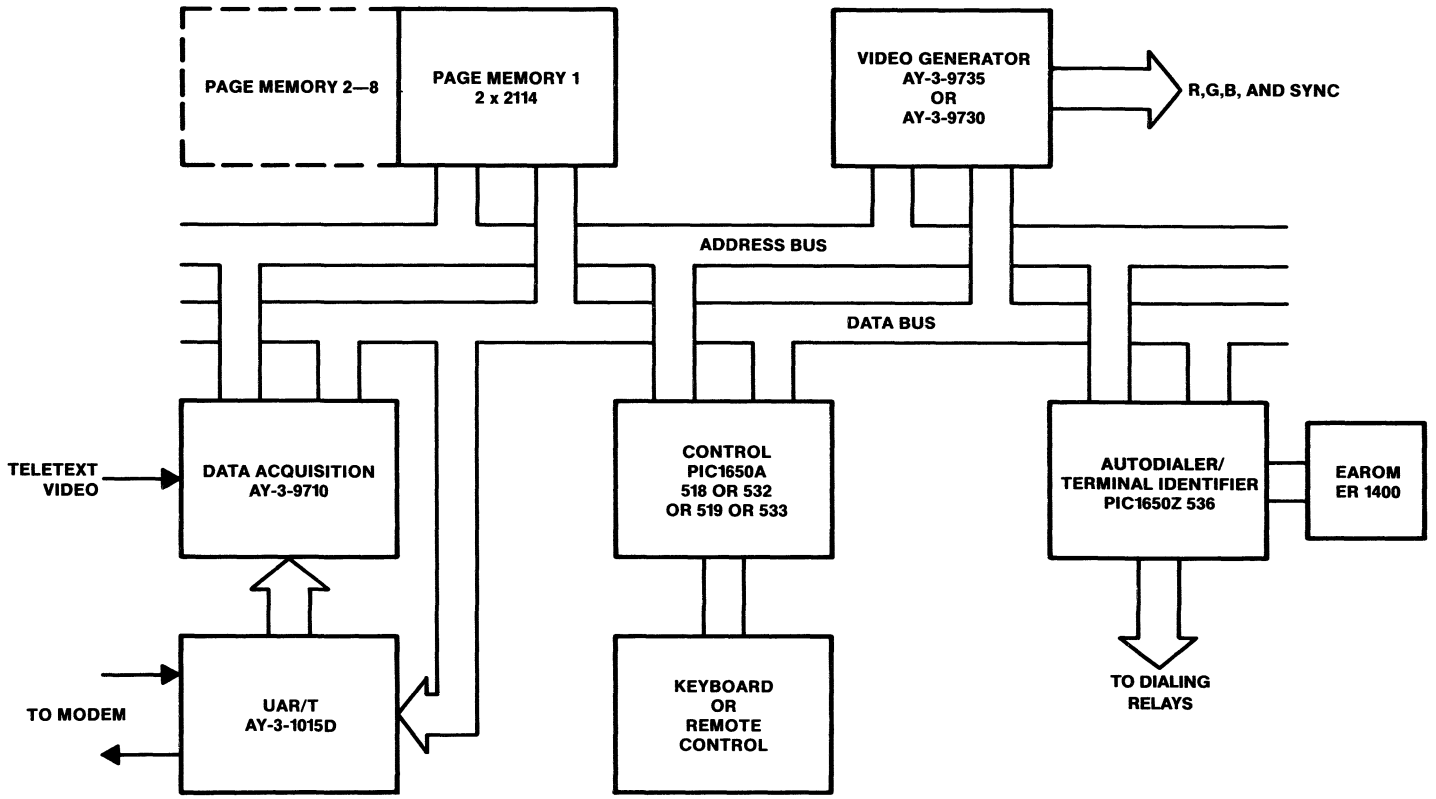


Fig. 1 TELEVIEW BLOCK DIAGRAM

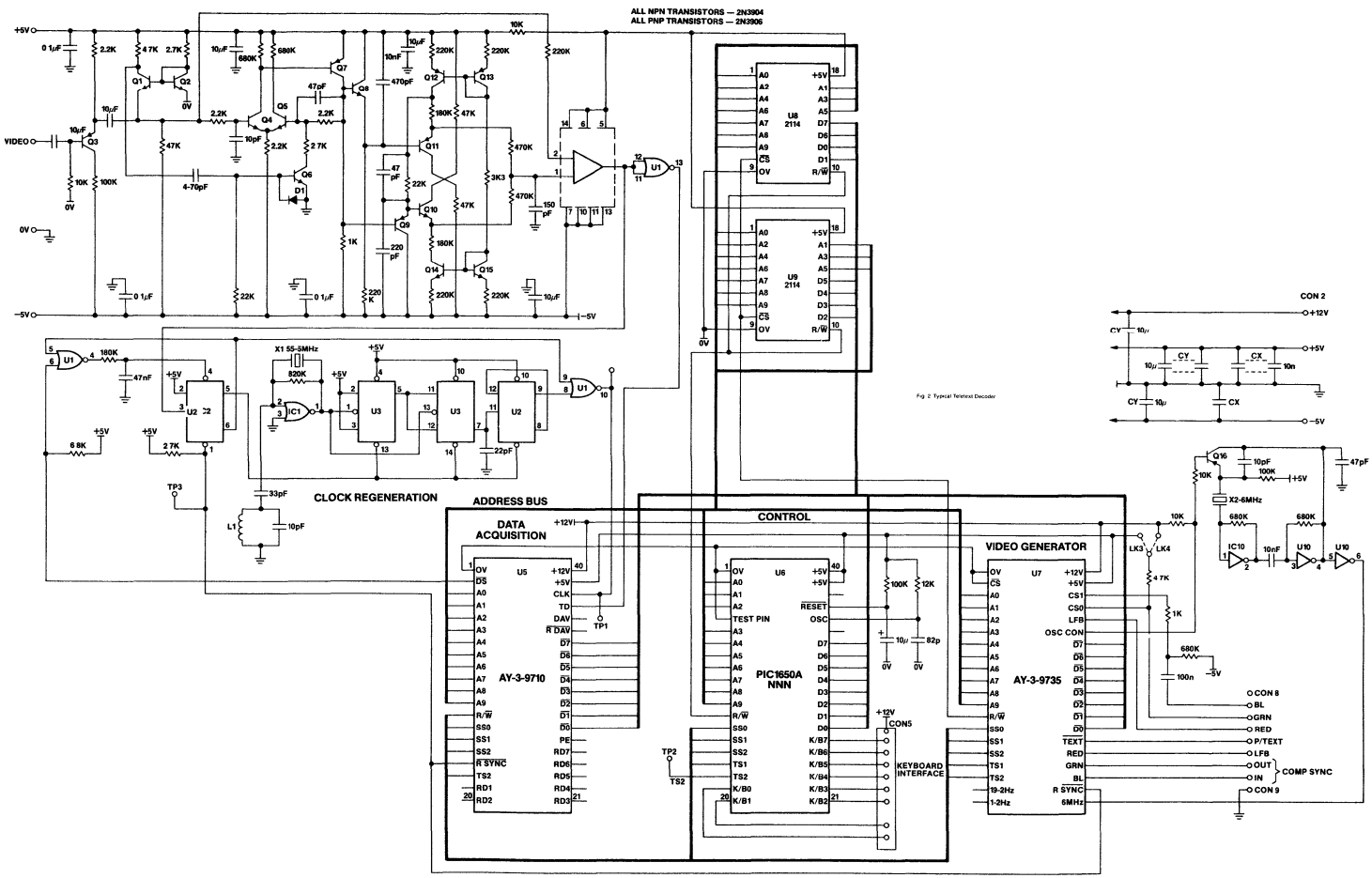
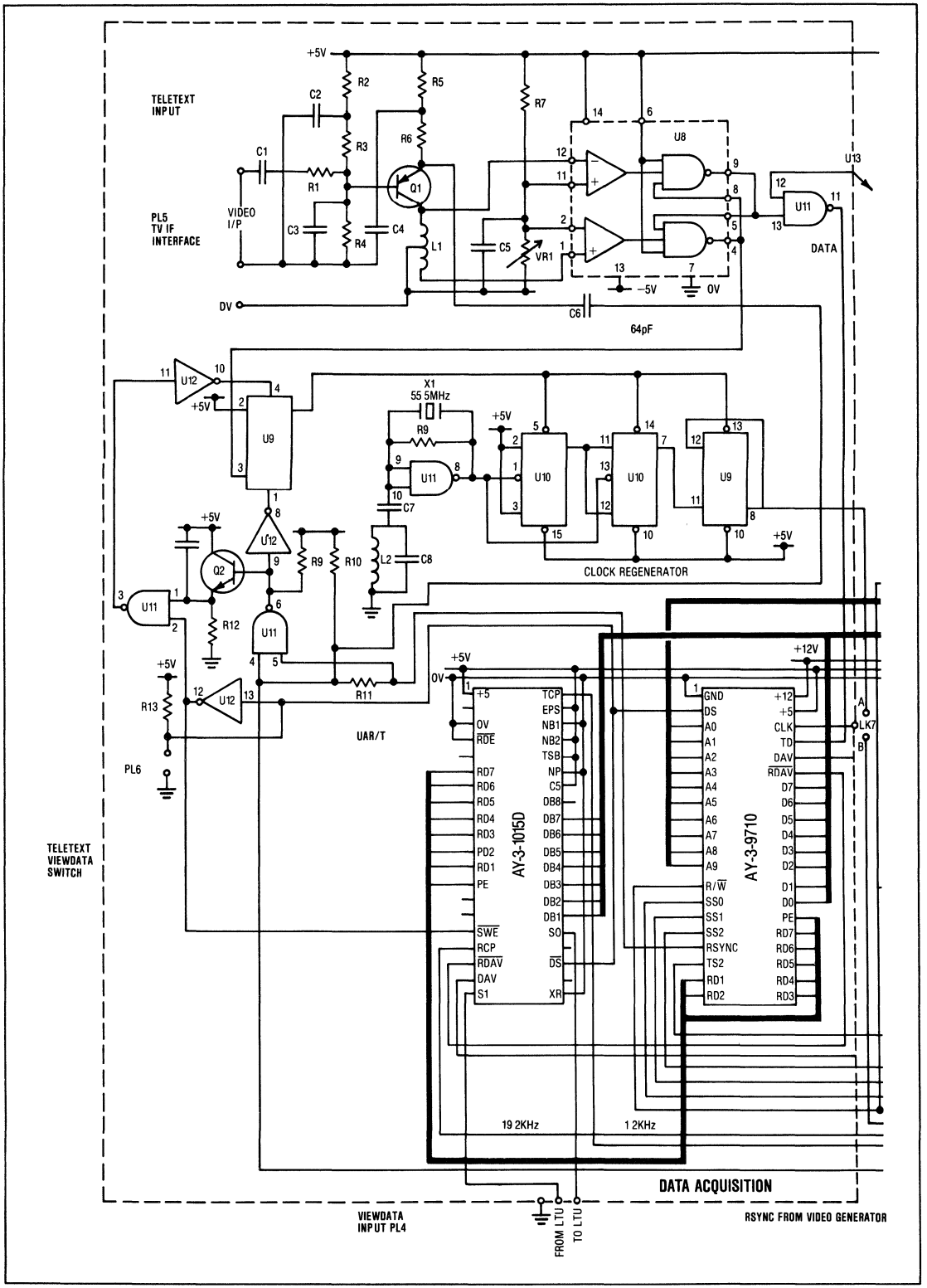


Fig. 2 TYPICAL TELETEXT DECODER


TELETEXT INPUT
PL5 TV IF INTERFACE
VIDEO I/P
+5V
R1
R2
R3
R4
R5
R6
R7
C1
C2
C3
C4
C5
C6
64pF
VR1
Q1
L1
U8
U11
U13
DATA
-5V
0V
DV
X1
55 5MHz
R9
U9
U10
U12
C7
C8
L2
R10
CLOCK REGENERATOR
Q2
R12
R13
PL6
UAR/T
R11
+12V
AY-3-1015D
AY-3-9710
TCP
EPS
NB1
NB2
TSB
NP
C5
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
S0
XR
SWE
RCP
RDAV
DAV
S1
RD7
RD6
RD5
RD4
RD3
PD2
RD1
PE
RDE
GND
DS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
R/W
SS0
SS1
SS2
RSYNC
TS2
RD1
RD2
CLK
TD
DAV
RDAV
D7
D6
D5
D4
D3
D2
D1
D0
PE
LK7
19 2KHz
1 2KHz
DATA ACQUISITION
TELETEXT VIEWDATA SWITCH
VIEWDATA INPUT PL4
FROM LTU
TO LTU
RSYNC FROM VIDEO GENERATOR

TELEVIEW Control Chip

FEATURES

- Interfaces user to Teleview system
- Initializes Teleview system
- PIC1650A-518 4 x 4 Keyboard, Teletext and Viewdata
- PIC1650A-519 4 x 4 Keyboard, Viewdata only, local programing of EAROM
- PIC1650A-532 ASCII or IR remote, Teletext and Viewdata
- PIC1650A-533 ASCII or IR remote, Viewdata only, local programing of EAROM

DESCRIPTION

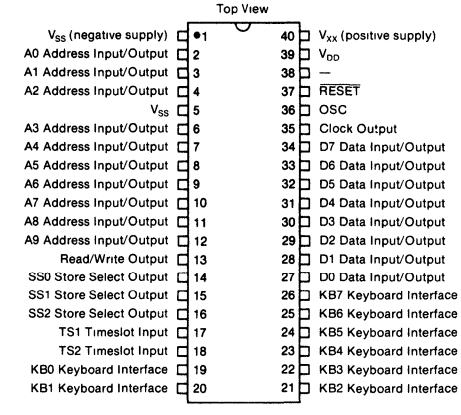
The Teleview control chip PIC1650A interfaces the user to the Teleview system and generally organizes the operation of the system.

It is available in several versions each providing alternative user inputs and operating features.

Customized versions can be provided if required.

The features of the various versions are shown in the appendices.

PIN CONFIGURATION



PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	Negative supply (Ground).
2-12	A0-A9	Address Input/Outputs which are connected to the Teleview Address Bus.
5	V_{SS}	Test pin — connect to V_{SS}.
13	Read/$\overline{\text{Write}}$	Control output connected to the Teleview R/W input.
14-16	SS0-SS2	Store Select outputs.
17, 18	TS1, TS2	Time Slot Inputs from Video Generator.
19-26	KB0-KB7	Keyboard Interface, may be Inputs, Outputs or Inputs/Outputs depending upon the version.
27-34	D0-D7	Data Inputs/Outputs which are connected to the Teleview Data Bus
35	Clock Output	Not used except to check the Clock frequency (output frequency $f_X/4$).
36	Oscillator	Oscillator resistor and capacitor connected to this pin
37	$\overline{\text{Reset}}$	Master reset input which must be kept at ground potential until the V_{DD} power is within specification.
38		Not used.
39	V_{DD}	Positive power supplies +5V Nom.
40	V_{XX}	

VIDEO

ELECTRICAL CHARACTERISTICS

(See PIC1650A Data Sheet for full specification).

Maximum Ratings*

Voltage on any pin with Respect to V_{SS} pin ..... −0.3V to +15V
Ambient Operating Temperature Range..... 0° C to +70° C
Storage Temperature Range ..... −55° C to +150° C

Standard Conditions (unless otherwise stated):

$V_{SS} = 0V$
$V_{DD} = +5V \pm 10\%$
$V_{XX} = +5V \pm 10\%$
$F_{clock} = 1MHz$
$T_A = 0° C$ to $+70° C$

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed

Characteristic	Min	Typ	Max	Units	Conditions
Clock Frequency	0.8	—	1	MHz	
Input Low Voltage	−0.2	—	0.8	V	
Input High Voltage	2.4	—	—	V	
Input High Voltage ($\overline{\text{Reset}}$)	$V_{DD}-1$	—	—	V	
Input Low Current	−200	—	−1600	μA	$V_{IL} = 0.4V$
Input High Current	−100	—	—	μA	$V_{IH} = 2.4V$
Input Leakage Current (Reset)	−10	—	10	μA	
Output Low Voltage	—	—	0.4	V	$I_{OL} = 1.6$ mA
Output High Voltage	2.4	—	—	V	$I_{OH} = -100\mu A$
Supply Current: I_{DD}	—	—	55	mA	
I_{XX}	—	—	5	—	

APPENDIX 1/PIC1650A-518

This version interfaces with a 4 x 4 keyboard and provides basic Teletext/Viewdata operation. It replaces pattern 514.

INPUT 4 x 4 matrix keyboard
POWER UP MODE Picture
POWER UP DISPLAY Teleview White
POWER UP PAGE XOO in Store 7
KEYBOARD INTERFACE

KB0 pin 19	Row Input/Output
KB1 pin 20	Row Input/Output
KB2 pin 21	Row Input/Output
KB3 pin 22	Row Input/Output
KB4 pin 23	Column Input/Output
KB5 pin 24	Column Input/Output
KB6 pin 25	Column Input/Output
KB7 pin 26	Column Input/Output

KEYBOARD CODES

KB0/KB4	7	KB2/KB4	1
KB0/KB5	8	KB2/KB5	2
KB0/KB6	9	KB2/KB6	3
KB0/KB7	Picture/Text	KB2/KB7	Reveal/Conceal
KB1/KB4	4	KB3/KB4	Page/*
KB1/KB5	5	KB3/KB5	0
KB1/KB6	6	KB3/KB6	Time/#
KB1/KB7	Update	KB3/KB7	Store Select

NOTES:

1. Details of the operating features are contained in the general Teleview documents.
2. Two double key operations are recognized:
   (a) Store Select 9 is equivalent to Box Clock.
   (b) Store Select 0 is equivalent to Hold.

APPENDIX 2/PIC1650A-532

This version interfaces either with an ASCII return to zero keyboard or with an AY-3-8475 remote control receiver. It replaces pattern 516.

INPUT (a) ASCII Return to zero
(b) Binary Return to zero (from local keyboard or AY-3-8475 remote control)
POWER UP MODE Picture
POWER UP DISPLAY (a) ASCII Teleview Cyan
(b) Binary Teleview Yellow
POWER UP PAGE XOO in Store 7
KEYBOARD INTERFACE

KB0 pin 19	LSB Input
KB1 pin 20	LSB Input
KB2 pin 21	LSB Input
KB3 pin 22	LSB Input
KB4 pin 23	LSB Input
KB5 pin 24	LSB Input
KB6 pin 25	MSB Input
KB7 pin 26	ASCII/Local Binary Input or Remote Acknowledge

KEYBOARD CODES

(a) ASCII
Standard 7 Bit ASCII (These codes are only acted upon in Viewdata Mode)

(b) Binary (Local or Remote)

Binary Code MSB LSB	Key Meaning
1100000	Picture/Text
1100001	Mix
1100010	Half Page Expansion
1100011	Store Select
1100100	7
1100101	8
1100110	9
1100111	Box Clock
1101000	4
1101001	5
1101010	6
1101011	Hold (Store Rotating Pages) (Release Line)

VIDEO

Binary Code MSB LSB	Key Meaning
1101100	1
1101101	2
1101110	3
1101111	Reveal/Conceal
1110000	Page (or * in Viewdata)
1110001	0
1110010	Time (or # in Viewdata)
1110011	Update/Clear
1110100	Rounding + Flash Off
1110101	Cursor ON
1110110	Cursor OFF
1110111	Roll Headers

NOTES:

1. During initialization the PIC1650A-532 decides whether an ASCII keyboard or an AY-3-8475 remote control receiver is being used. If all Keyboard Interface inputs are low an ASCII keyboard is assumed.
   (a) ASCII Mode
   Return to zero signalling is employed, the KB7 input being used to switch from full ASCII to local Binary.
   With KB7 equal to 1 the other 7 bits are read as standard ASCII. (Note this input must be pulsed with the other bits).
   With KB7 equal to '0' the other 7 bits are read as binary with meanings detailed above.
   (b) Remote Mode
   In this case the same binary codes are used but an acknowledgement routine is performed by the PIC1650A-532. See AY-3-8475 data sheet for details.
   The connections between the PIC1650A-532 and the AY-3-8475 are made as follows:

PIC1650A-532	AY-3-8475
KB0 pin 19	I/O A pin 14
KB1 pin 20	I/O B pin 15
KB2 pin 21	I/O C pin 16
KB3 pin 22	I/O D pin 17
KB4 pin 23	I/O E pin 20
KB5 pin 24	I/O F pin 21
KB6 pin 25	I/O G pin 22
KB7 pin 26	Digital Data Control + Data Available (pins 18, 19).

2. The codes should be valid for a minimum of 20ms. In the ASCII mode if the two key operation SS0 is used the Second code (0) should only be valid for a maximum of 120ms to avoid changing keyboard modes.
3. The double key operations are recognized:
   (a) Store Select 9 is equivalent to Roll Headers.
   (b) Store Select 0 is equivalent to Reset (Clear Stores)

APPENDIX 3/PIC1650A-519

This version interfaces with a 4 x 4 keyboard and as such may replace pattern 518.

It provides control of Viewdata functions only, together with local programing of Telephone numbers via PIC1650-536.

INPUT	4 x 4 matrix keyboard
POWER UP MODE	Text (picture mode not available) Cursor off
POWER UP DISPLAY	Double height Teleview in yellow on blue
POWER UP STORE	Store 1 (binary 000)
KEYBOARD INTERFACE	
KB0 pin 19	Row Input/Output
KB1 pin 20	Row Input/Output
KB2 pin 21	Row Input/Output
KB3 pin 22	Row Input/Output
KB4 pin 23	Column Input/Output
KB5 pin 24	Column Input/Output
KB6 pin 25	Column Input/Output
KB7 pin 26	Column Input/Output

KEYBOARD CODES

0/4	7	2/4	1
0/5	8	2/5	2
0/6	9	2/6	3
0/7	Hold/Disconnect	2/7	Reveal/Conceal
1/4	4	3/4	Star
1/5	5	3/5	0
1/6	6	3/6	Square
1/7	Half page expansion	3/7	Store Select

Operation

(a) Star, Square and digits 0-9 transmitted to line via UAR/T and MODEM. If 536 autodialer fitted then the square key plus digits 1-4 are used to dial.

(b) Hold. If 536 autodialer fitted this key will cause the telephone line to be released while maintaining the display.

(c) Print The two key sequence SS.9 is used to alternately put the system into MIX mode and back to normal Mix mode enables monochrome video to be generated and removes colored backgrounds. When entering mix mode character rounding and flashing are inhibited until a new page is received (only for AY-3-9735)

(d) Reveal/Conceal Alternately reveals and conceals concealed characters. Reveal mode off when new page received or new store selected

(e) Store select Followed by digits 1-8 will select one of eight possible Stores for display. If 536 autodialer fitted and system in "link-back" mode then local programing of telephone numbers may be enabled by selecting Store zero. SS0 will clear screen and digits 1-4 may be pressed to enable the programing of the appropriate telephone number. The numbers entered using digits 0-9 (0 displayed as :), star for access pause (displayed as ,) and square for formatting and space filler (displayed as ?) to complete all 16 digits. SS0 followed by Reveal will display all the telephone numbers on the screen.

APPENDIX 4/PIC1650A-533

This version interfaces either with an ASCII, return to zero keyboard or with an AY-3-8475 remote control receiver and as such may replace pattern 532.

It provides control of Viewdata functions only together with Local Programing of Telephone numbers via PIC1650-536.

INPUT	ASCII return to zero or binary return to zero from local keyboard or direct connection to remote receiver
POWER UP MODE	Text, Cursor off
POWER UP DISPLAY	Double height Teleview in yellow on blue
POWER UP STORE	Store number 1 (binary 000)
KEYBOARD INTERFACE	
KB0 pin 19	LSB Input
KB1 pin 20	LSB Input
KB2 pin 21	LSB Input
KB3 pin 22	LSB Input
KB4 pin 23	LSB Input
KB5 pin 24	LSB Input
KB6 pin 25	MSB Input
KB7 pin 26	ASCII/Local Binary Input or Remote Acknowledge

KEYBOARD CODES

(a) ASCII

Full 7 bit ASCII set

(b) Binary (Local or Remote)

Binary Code	Key Meaning
1100000	Picture/Text
1100001	Print
1100010	Half page expansion
1100011	Store Select
1100100	7
1100101	8
1100110	9
1100111	(not used)
1101000	4
1101001	5
1101010	6
1101011	Hold/Disconnect line
1101100	1
1101101	2
1101110	3
1101111	Reveal/Conceal
1110000	Star
1110001	0
1110010	Square
1110011	Clear (inhibit display)
1110100	Rounding & Flashing off
1110101	Cursor ON
1110110	Cursor OFF
1110111	Reset

Notes 1 and 2 as for pattern 532.

Operation

(a) ASCII codes transmitted directly to line via UAR/T and MODEM. If 536 autodialer fitted, square and digits 1-4 will enable dialing.

(b) Picture/Text. Switches display alternately between picture and text. If 536 autodialer fitted this key will drop the telephone connection

(c) Print. Alternately puts system into MIX mode and back to normal. Mix mode enables monochrome video to be generated and removes colored backgrounds. When entering mix mode character rounding and flashing are inhibited until new page received (only for AY-3-9735).

(d) Store/Select. Followed by digits 1-8 will select one of eight possible Stores for display. If 536 autodialer fitted and system in "link-back" mode then Local Programing of telephone numbers may be enabled by selecting store zero. SS0 will clear screen and digits 1-4 may be pressed to enable the programing of the appropriate telephone number. The number is entered using digits 0-9 (0 displayed as :) star for access pause (displayed as ;) and square as formatter and space filler (displayed as ?) to complete all 16 digits. SS0 followed by Reveal will display all the telephone numbers on the screen.

(e) Hold. If the 536 autodialer is fitted this key will drop the telephone line.

(f) Reveal/Conceal. Will alternately reveal and conceal concealed characters. Initialized to conceal state for new page or new Store.

(g) Clear. Clears the screen of all text. Display restored by second depression of the key and by reception of a new page.

(h) Rounding and Flashing Off. Character rounding and flashing may be inhibited in AY-3-9735 until a new page is received.

(i) Cursor ON/OFF. The cursor may be locally controlled by these codes.

(j) Reset. Simulate the power-on reset. All stores are cleared and initialized to "Teleview"

TELEVIEW Autodialer/Terminal Identifier

FEATURES

- Non-volatile storage of 4 telephone numbers of 16 digits
- 10 ips loop disconnect dialing
- Non-volatile storage of Identity Code of 16 digits
- Full remote programing capability
- Optional local programing
- Easy connection to Teleview system
- Spare memory locations

DESCRIPTION

The Autodialer/Terminal identifier is an extension to the TELEVIEW system that is designed to perform the Autodialing function of a Viewdata system, to transmit the terminal identification (ID) code and to allow the remote programing of all the stored numbers.

The system consists of a PIC1650-536 attached to the TELEVIEW address and data highways, an ER1400 EAROM for non-volatile storage of the ID and telephone numbers and relays for controlling the telephone line

PACKAGES

ER1400	— 14 lead DIL plastic
PIC1650-536	— 40 lead DIL

ABSOLUTE MAXIMUM RATINGS

See ER1400 and PIC1650 Data Sheets for details.

ELECTRICAL CHARACTERISTICS

See ER1400 and PIC1650 Data Sheets for details.

OPERATION

Autodialer — The system responds to inputs via the TELEVIEW keyboard in order to initiate the automatic dialing of the Viewdata telephone numbers. There are 4 stored telephone numbers that may be accessed by 4 keys as described in the Prestel Terminal Specification

Each Telephone number can consist of up to 16 digits including access pauses and formatting codes.

The system may be operated fully automatically or with manual dialing.

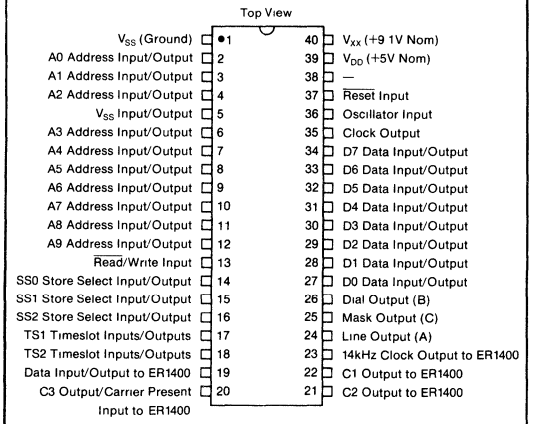
Automatic Dialing — With the system off-line and in the Viewdata mode the initial action is to press the Square (#) key. The Televiev system will be put in the Text mode and the currently displayed Store will be cleared. The telephone line will be looped and the audio should be switched to a loudspeaker.

Once dialing tone is heard a digit is pressed according to the Viewdata service required.

Digit 1 — will give the Prestel service. (Block 2)
Digit 2 — will give a second number for the Prestel service. (Block 3)
Digit 3 — will give the third number. (Block 6)
Digit 4 — will give the fourth number. (Block 7)

If a digit is not pressed for 30 seconds after the Square (#) key the line will be released. The digits will be put onto the screen as they are being dialed and if formatting characters had been loaded in the digit store the display will be spaced accordingly.

PIN CONFIGURATION TV 1650



If a pause had been programed, for access to a further dial tone for example, the system will put a * on the screen and wait for release. To release the access pause the appropriate digit is pressed again and dialing will continue. If the system does not receive a manual release it will continue after a time-out of four seconds

If at the end of dialing the call fails, pressing the Square (#) key will clear the call and then start again by relooping the line.

When the required incoming carrier tone is received the modem will return its appropriate tone to the Viewdata computer which may then send the first page of data and initiate terminal identification.

If the carrier tone is not received for any reason the line will be released after 30 seconds.

Once a satisfactory connection is made to the Viewdata computer (i.e. carrier is detected), the keypad will revert to normal Viewdata mode and dialing will not be possible.

Manual Dialing — If the required telephone number is not stored within the terminal the call may be made using the normal telephone. The system should start off-line and in the Viewdata mode. The number is dialed using the telephone in the normal way and when dialing is complete the Square (#) Key is pressed. This will put the system into the Text mode, erase the currenty displayed store and hold the line. The telephone handset is replaced and once the carrier tone is received the procedure is as before.

Connection Release — If at any time the carrier detection logic detects that the carrier is lost the connection will be immediately released.

The connection will also be released when the Televiev system is switched to the Picture or Teletext modes, or if the Hold Key is pressed (if available).

Alternatively the appropriate computer log off procedure may be used.

In all cases the content of the Teleview Stores will remain as they were at the moment of disconnection

Remote Programing — The Teleview highways will be monitored for those special ESC sequence codes that indicate the entry into the Program-Verify mode as described in the Prestel Terminal Specification.

In the Teleview System the Data Acquisition chip receives data from the Viewdata computer and normally loads data to the display store. Any codes, particularly ESC sequences, that it does not use, it puts out onto the Teleview highway system where the remote programing device may receive them.

The basic programing sequences are as described in the Prestel Specification except that the data for programing the EAROM will initially be put into the display store by the DA chip. The programing device will read the digits from this store and erase them after checking that they are all valid codes. The display will be blanked during programing.

Local Programing — For system security, particularly in the domestic environment, the local programing of telephone numbers and identity codes is not encouraged.

However, the Teleview system has been designed such that it may "talk to itself" and by doing this and having some additional keys (especially ESC, ENQ, ?, : and ;) a very secure local programing mode is available.

The UAR/T transmit and receive clocks are connected to a single frequency, the output joined to the input and the carrier present input is forced and true. The standard programing sequences may then be input to the system to read out and/or modify the content of the digit store.

Spare Storage — While only the first 7 blocks of storage are defined (as ID code plus 6 telephone numbers) a further 4 blocks are available and may be accessed by the Program/Verify sequences if required. They could, for example, be used to store alternative identity/security codes for private Viewdata systems.

Programing Routine — (The following is an extract from the Prestel Terminal Specification.)

The programing Routine is entered by a 4 character sequence ESC1 ESC2. This puts the terminal into Program-Verify mode (See Fig. 1). The memory is divided into seven 16 character blocks. A skip block command ESC 3 is used to skip through the blocks. Default is block 1 at entry to Program-Verify mode After a number (0-6) of skip block commands, Verify mode may be selected by ENQ, or Program mode may be selected by ESC 4.

Entry of Verify mode shall cause the terminal to transmit down the telephone line the contents of the current block (excluding any space-filling characters) and 75 bit/s and then revert to normal mode

Program data shall follow ESC 4 using the numbers 0-9 for the Identity Code and the codes given below for telephone numbers. Character 3/15 (?) will be used as a space filling character after valid data characters to make the total number of characters in a block equal to 16. 3/15 (?) may also be used between parts of the number to identify "natural" breaks. It may then be displayed as a space if the number is displayed for the user, e.g.:1?618?1111????? displayed as 01 618 1111.

After receiving these 16 characters the terminal reverts to normal mode.

Dialer Codes **DIALED DIGIT**	(only for blocks 2-7) **RECEIVED IS07 CHARACTER** (also used for transmission after ENQ for block verification)
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
0	.
PAUSE	,
RESERVED	>
SPACE FILLER	?

A delay of at least 5ms will be present between the last character to be written into the memory and the next attempt to leave Normal mode This is to facilitate the use of slow write/erase memories.

Blocks 1-7 are defined as follows: —

Block 1	Identity Number
Block 2	Telephone Number A
Block 3	Telephone Number B
Block 4	Not used
Block 5	Not used
Block 6	Telephone Number E
Block 7	Telephone Number F

A and B are the Prestel Computer Center telephone numbers.

E and F are the third and fourth choices

Line Interface — (The following is an extract from the Prestel Terminal Specification)

Physical Termination

The Post Office will install a Jack 96A in customer's premises to access Prestel. The customer Prestel Terminal will require a suitable compatible plug (e.g Post Office Plug 505)

DC CONDITIONS

Four sets of DC conditions are specified for the line interface.

(a) The off-line condition (idle state) applies when the terminal is not using the telephone line

(b) The line holding condition applies when the terminal goes on-line, is sending tones to or receiving tones from the line and during inter-digit pauses

(c) The pulsing make condition applies during the make part of a dialed digit pulse.

(d) The pulsing break condition applies during the breakpart of a dialed digit pulse.

	Plug Points	Resistance	Capacitance
(a) Off-Line Idle Condition	2—3	>5 Mohm*	≤0.01μF
	1—5	<10 ohm	
(b) Line Holding Condition	2—3	≤300 ohm‡	
	1—5	>5 Mohm	
(c) Pulsing Make	2—3	≤50 ohm	
	1—5	>5 Mohm	
(d) Pulsing Break	2—3	>5 Mohm	
	1—5	>5 Mohm *	
All times	Any to earth	>5 Mohm*	≤0.01μF

* Measured at 250 vdc. All conditions to be independent of polarity.

‡ Measured with line curents up to 120mA.

The max dc short circuit available from line is 120mA.

AC CONDITIONS

When the terminal is on-line (i.e. line holding condition) it shall present an impedance between 400 and 900 ohms at an angle not greater than 45 degrees for all frequencies between 300Hz and 3400Hz between plug points 2 and 3.

AUTODIALING

If a loop disconnect autodialer is fitted then the following requirements must be met:

The digit signals shall appear as loop disconnect pulses between Plug Points 2 and 3 at a repetition rate of between 9 and 11 pulses per second. The break period shall be between 63% and 70% of the total pulse period (break plus make). The length of the break period condition (d) of each pulse shall be within the limits of 57.2

PIN FUNCTIONS

Pin No.	Name	Function
(A) ER1400		
1	Data	Input/Output
2	—	
3	V_{SS}	+9.1V supply
4	V_{GG}	−26V supply
5	Clock	Input
6	C1 Input	Mode control pins
7	C2 Input	
8	C3 Input	
(B) PIC1650-635		
1	V_{SS}	Ground
2	A0	Address Input/Output — connect to TELEVIEW Address Bus
3	A1	
4	A2	
5	V_{SS}	
6	A3	Address Input/Output — connect to TELEVIEW Address Bus
7	A4	
8	A5	
9	A6	
10	A7	
11	A8	
12	A9	
13	$\overline{\text{Read}}$/Write Input/Output	Control to Page Memory — connect to TELEVIEW R/W line
14	SS0	Store Select Inputs/Outputs — connect to TELEVIEW SS lines
15	SS1	
16	SS2	
17	TS1	Time Slot Inputs — connect to TELEVIEW TS lines
18	TS2	
19	Data Input/Output	Interface to ER1400 non volatile memory. Pin 20 doubles as the carrier present input
20	C3 Output	
21	C2 Output	
22	C1 Output	
23	14kHzClock Output	
24	Line Output	Output to Line Looping relay
25	Mask Output	Output to Mask relay
26	Dial Output	Output to Dialing relay
27	D0	Data Input/Output — connect to TELEVIEW Data Bus
28	D1	
29	D2	
30	D3	
31	D4	
32	D5	
33	D6	
34	D7	
35	Clock Output	Monitor point for Clock oscillator. Set frequency to 250kHz nominal
36	Oscillator Input	Connect Clock oscillator components to this point
37	$\overline{\text{Reset}}$ Input	Master reset input connect to corresponding pin on TELEVIEW control PIC1650A
38	—	No connection
39	V_{DD}	Positive supply +5V nom.
40	V_{XX}	Positive supply to output buffers +9.1V nom.

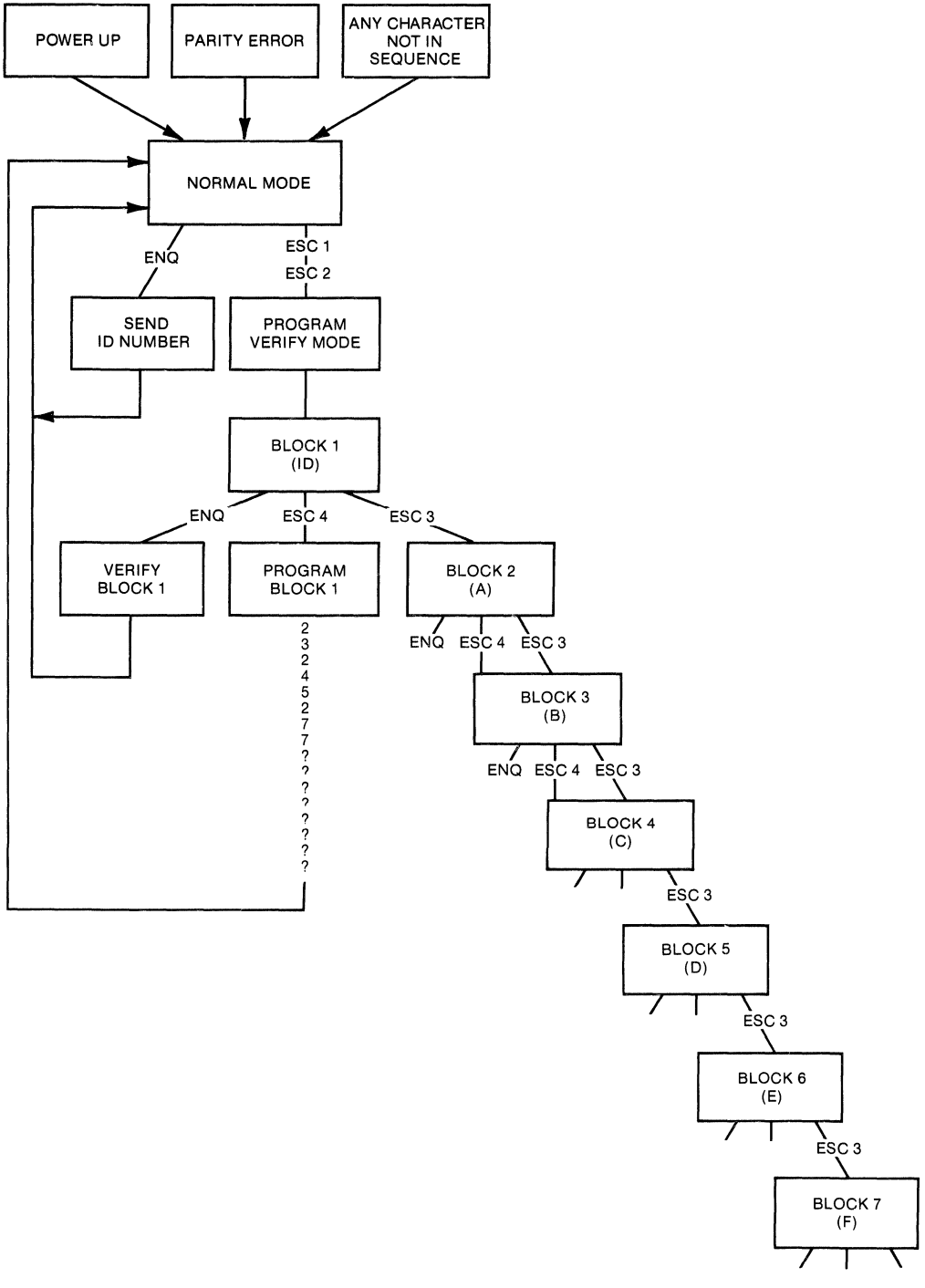


Fig. 1 FLOW DIAGRAM FOR PROGRAMING ID AND TELEPHONE NUMBERS

to 77.3 ms and the length of the make period condition (c) between any two break periods shall be within the limits 27.2 to 41.1 ms. For a period of at least 5 ms before and after pulsing condition (c) shall apply.

The digit to be dialed represents the number of break pulses to be sent except that digit 0 represents 10 pulses. Inter digit pauses shall be provided. The duration shall be between 800 and 900 ms. During the pause, condition (b) shall apply except during the first and last 5ms periods when condition (c) shall apply. (Fig. 2 explains this diagramatically).

When the terminal is transferring to the line holding state the high impedance between Plug Points 1 and 5 must not be presented more than 20 ms before the low impedance is presented between Plug Points 2 and 3.

APPLICATION

The Autodialer/Terminal Identifier has been designed for easy incorporation into the basic Teleview system. Special care has been taken to ensure that pin connections allow an easy and logical printing circuit layout.

The circuit diagram of the main electronics is shown in Fig. 3 and that of the Line Interface in Fig. 4.

The system has the following power supply requirements:

+9.1V	@	13mA	
+5V	@	140mA	(Relays)
+5V	@	55mA	(Logic)
−26V	@	8mA	

It may be acceptable to eliminate RLC and substitute two silicon diodes back to back across the modem side of the isolation transformer. This will be subject to approval by the BPO if used in Prestel equipment.

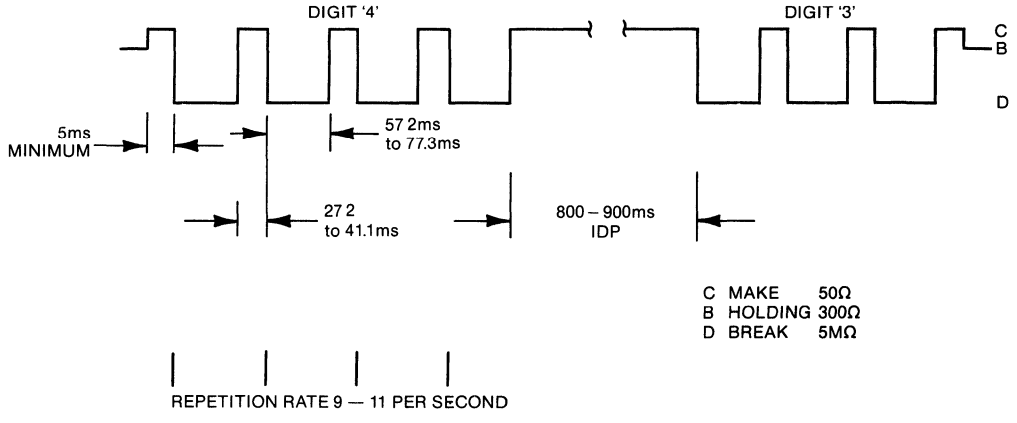


Fig. 2 AUTODIALER PULSES

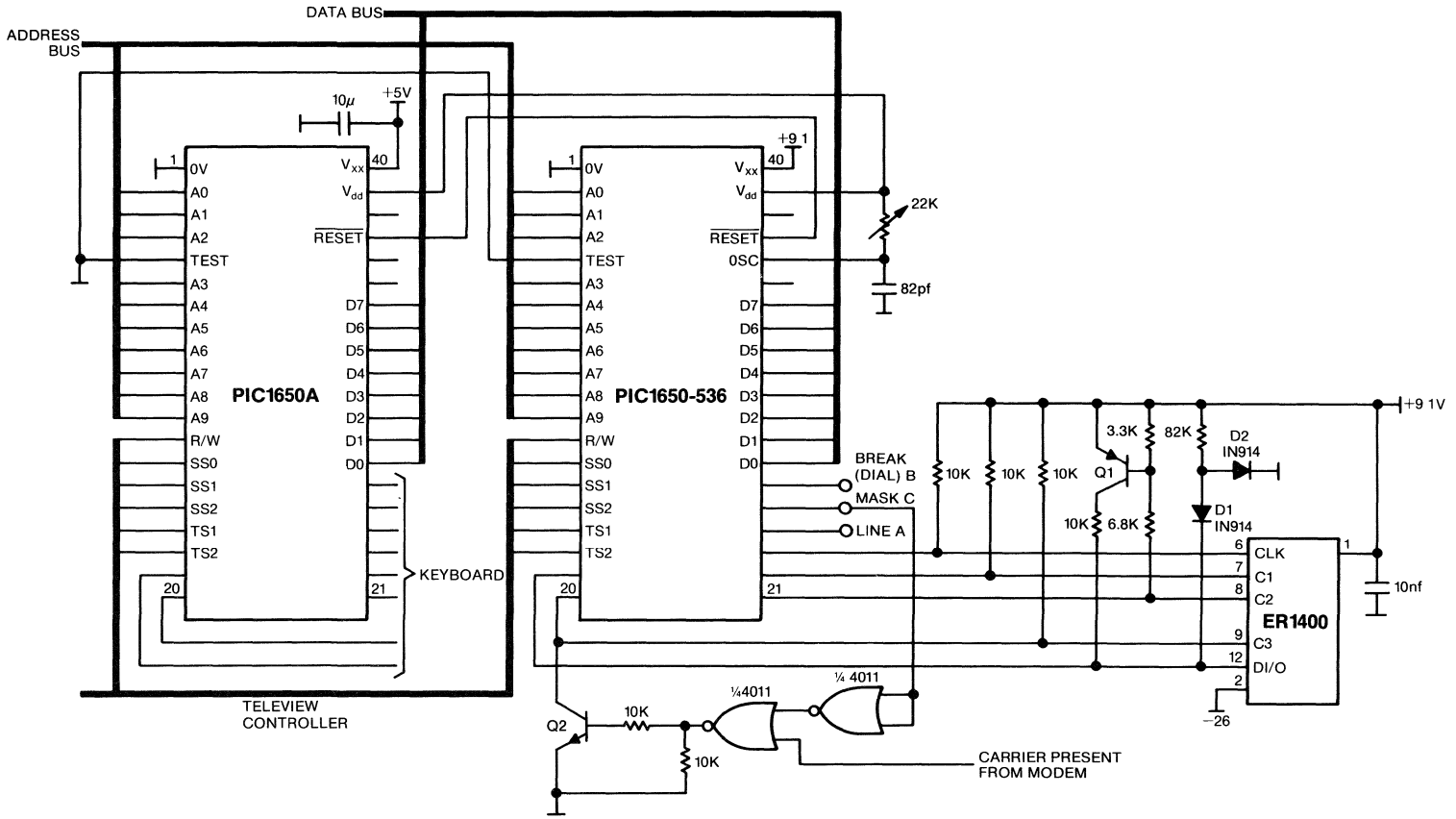
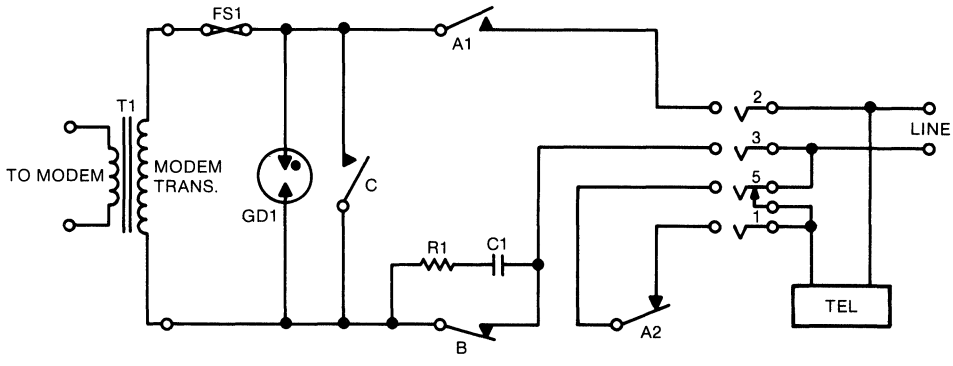
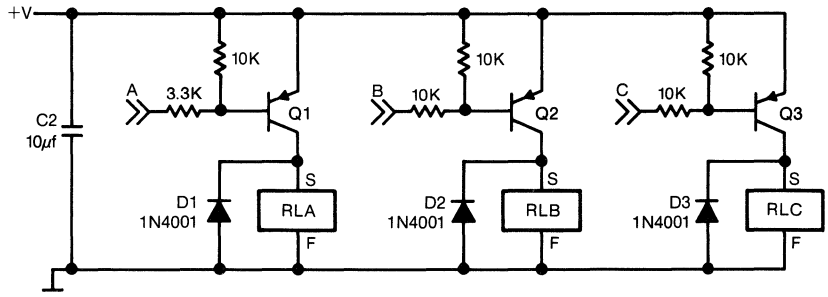


Fig. 3 AUTODIALER ADD ON CIRCUIT FOR TELEVIEW





T1	
RLA	CLARE CUP-V 10301
RLB	CLARE CUP-V 10201
RLC	CLARE CUP-V 10001
GD1	CERBERUS UC 90Q
R1	100 OHMS
FS1	250mA QUICK BLOW, ES4265
C1	2μf

Fig. 4 TELEVIEW LINE SWITCHING

VIDEO

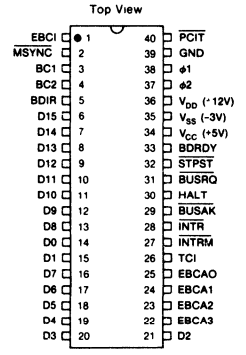
16-Bit Microprocessor

FEATURES

- 8 program accessible 16-bit general purpose registers
- 86 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit logic and 2's complement arithmetic
- Status logic and word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64K memory using single address
- TTL compatible/simple bus structure
- CP1610. 1μs cycle time, 2MHz 2-phase clock

PIN CONFIGURATION

40 LEAD DUAL IN LINE



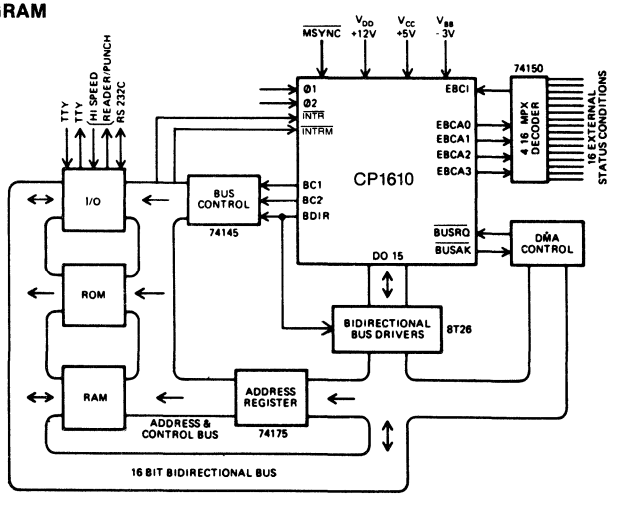
DESCRIPTION

The CP1610 is a compatible member of the Series 1600 Microprocessor products family. It is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with the General Instrument N-Channel Ion-Implant process, insuring high performance with proven reliability and production history. All members of the Series 1600 family are fully compatible with the CP1610.

The Microprocessor has been designed for high speed data processing and real time applications. Typical applications include programable TV games, home computer systems/ home information centers, programable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications.The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard, cassette tape, floppy disk, and RS-232C data communication lines.

The CP1610 utilizes third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of the program memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

CP1610 SYSTEM DIAGRAM



PROCESSOR SIGNALS

DATA BUS

D0-D15
Input/Output/High Impedance

Data 0-15: 16-bit bidirectional bus used to transfer data, addresses, and instructions between the microprocessor, memory, and peripheral devices.

PROCESSOR CONTROL

$\overline{\text{STPST}}$
Input
STop-STart: Edge-triggered by negative transition; used to control the running condition of the microprocessor.

HALT
Output
HALT: indicates that the microprocessor is in a stopped mode.

$\overline{\text{MSYNC}}$
Input
Master SYNC: Active low input synchronizes the microprocessor to the $\phi 1$, $\phi 2$ clocks during power-up initialization.

EBCA 0-3
Outputs
External Branch Condition Addresses 0-3: Address for one-of-16 external digital state tests via the BEXT (Branch on EXTernal) instruction.

EBCI
Input
External Branch Condition Input: Return signal from the one-of-16 selection made by EBCA 0-3.

BUS CONTROL

BDIR, BC1, BC2
Outputs
Bus DIRection, Bus Controls 1, 2: Bus control signals externally decoded to define the state of bus operations (see State Flow Diagram).

$\overline{\text{BUSRQ}}$
Input

$\overline{\text{BUSAK}}$
Output
BUS ReQuest, BUS AcKnowledge: BUSRQ* requests the microprocessor to relinquish control of the bus indefinitely. BUSAK* informs devices that the bus has been released.

BDRDY
Input
Bus Data ReaDY: causes the microprocessor to "wait" and resynchronize to slow memory and peripheral devices.

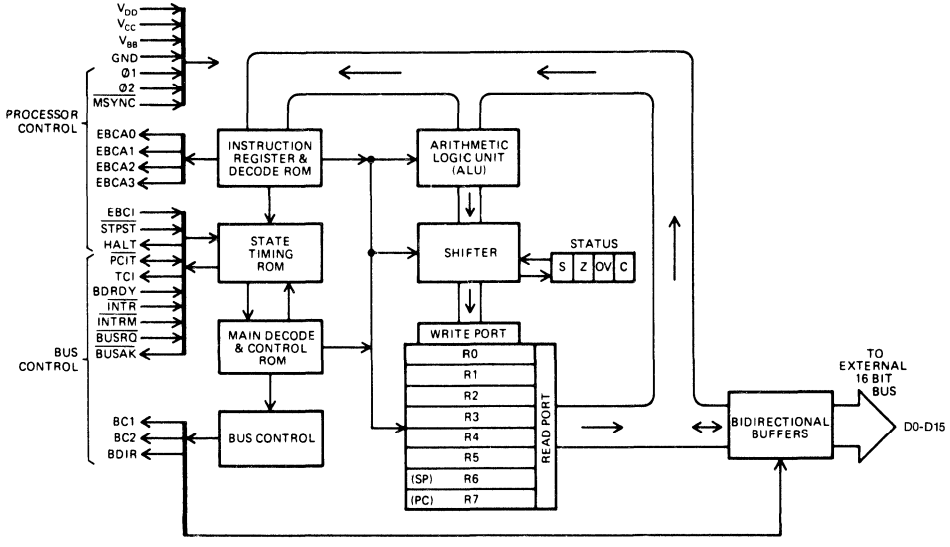
$\overline{\text{INTR}}$, $\overline{\text{INTRM}}$
INTeRupt, INTeRupt Masked: request the microprocessor to service an interrupt upon completion of current instruction.

TCI
Output
Terminate Current Interrupt: pulse outputted by the microprocessor in response to the TCI instruction.

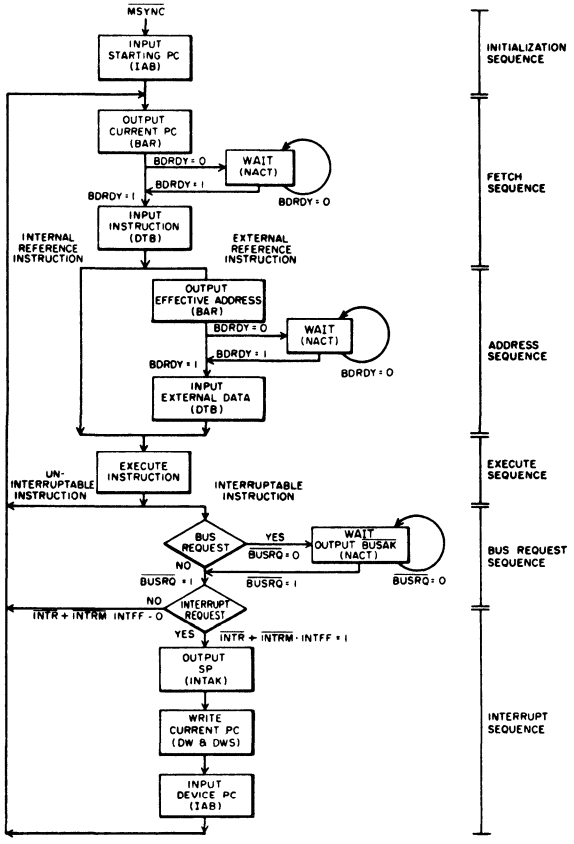
$\overline{\text{PCIT}}$
Input/output
Program Counter Inhibit/Trap: As an input, inhibits incrementation of the Program Counter during the instruction fetch sequence. As an output, generates a pulse during execution of a Software INterrupt (SIN) instruction.

VIDEO

CP1610 INTERNAL BLOCK DIAGRAM



SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

BDIR	BC2	BC1	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	0	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	1	DTB	Data To Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DW	Data Write
1	1	0	DWS	Data Write Strobe
1	1	1	INTAK	INTerrupt AcKnowledge

INSTRUCTION SET (SUMMARY LISTING)

		Mnemonics	Operation	Microcycles				Comments
				Dir.	Imm.	Indir.	Stack	
INTERNAL REFERENCE INSTRUCTIONS	Register to Register	MOVR	MOVe Register	6/7				
		TSTR	TeST Register	6/7				MOVR to itself
		JR	Jump to address in Register	7				MOVR to PC
		ADDR	ADD contents of Registers	6				
		SUBR	SUBtract contents of Registers	6				
		CMPR	CoMPare Registers by subtr	6				Results not stored
		ANDR	logical AND Registers	6				
		XORR	eXclusive OR Registers	6				
		CLRR	CLeaR Register	6				XORR with itself
	Single Register	INCR	INCrement Register	6				
		DECR	DECrement Register	6				
		COMR	COMplement Register	6				One's Complement
		NEGR	NEGate Register	6				Two's Complement
		ADCR	ADd Carry Bit to Register	6				
		GSWD	Get Status WorD	6				
		NOP	No OPeration	6				
		SIN	Software INterrupt	6				Pulse to $\overline{\text{PCIT}}$ pin
		RSWD	Return Status WorD	6				
	Register Shift	SWAP	SWAP 8-bit bytes	6				
		SLL	Shift Logical Left	6				
		RLC	Rotate Left thru Carry	6				Not interruptable
		SLLC	Shift Logical Left thru Carry	6				One or two position
		SLR	Shift Logical Right	6				shift capability Two position
		SAR	Shift Arithmetic Right	6				SWAP not supported
		RRC	Rotate Right thru Carry	6				
		SARC	Shift Arithmetic Right thru Carry	6				Add two cycles for 2-position shift
	Control Instructions	HLT	HaLT	4				
		SDBD	Set Double Byte Data	4				Must precede external reference
		EIS	Enable Interrupt System	4				to double byte data
		DIS	Disable Interrupt System	4				
		TCI	Terminate Current Interrupt	4				Not interruptable
		CLRC	CLeaR Carry to zero	4				
		SETC	SET Carry to one	4				
	Jump Instructions	J	Jump	12				
		JE	Jump, Enable, interrupt	12				
		JD	Jump, Disable interrupt	12				
		JSR	Jump, Save Return	12				Return Address
		JSRE	Jump, Save Return & Enable	12				saved in R4, 5 or 6
		JSRD	Jump, Save Return & Disable interrupt	12				
EXTERNAL REFERENCE INSTRUCTIONS	Conditional Branch Instructions	B	unconditional Branch	9*				Two words
		NOPP	No OPeration	7*				
		BC (BLGE)	Branch on Carry	7				C=1
		BNC (BLLT)	Branch on No Carry	7				C=0
		BOV	Branch on OVerflow	7				OV=1
		BNOV	Branch on No OVerflow	7				OV=0
		BPL	Branch on PLus	7				S=0
		BMI	Branch on Minus	7				S=1
		BZE (BEQ)	Branch on ZEro or EQual	7				Z=1
		BNZE (BNEQ)	Branch if Not ZEro or Not EQual	7				Z=0
		BLT	Branch if Less Than	7				S∀OV=1
		BGE	Branch if Greater than or Equal	7				S∀OV=0
		BLE	Branch if Less than or Equal	7				ZV(S∀OV)=1
		BGT	Branch if Greater Than	7				ZV(S∀OV)=0
		BUSC	Branch if Sign≠Carry	7				C∀S=1
		BESC	Branch if Sign=Carry	7				C∀S=0
		BEXT	Branch if External condition is True	7				4 LSB of instruction are decoded select 1 of 16 external conditions
								Add 2 cycles if test condition is true, except *
								Displacement in PC+1 PC←PC±Displacement
	I/O	MVO	MoVe Out	11	9	9	9	Not interruptable
		PSHR	PuSH Register to stack	—	—	—	9	PSHR=MVO@R6. Not interruptable
		MVI	MoVe In	10	8	8	11	
		PULR	PULl from stack to Register	—	—	—	11	PULR=MVI@R6.
	Arithmetic & Logic	ADD	ADD	10	8	8	11	
		SUB	SUBtract	10	8	8	11	
		CMP	CoMPare	10	8	8	11	Result not saved
		AND	logical AND	10	8	8	11	
		XOR	eXclusive OR	10	8	8	11	

1 MICROCYCLE=2 CLOCK CYCLES

VIDEO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other Input/Output Voltages with Respect to V_{BB} ..... −0.3V to +18.0V
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed

Standard Conditions: (unless otherwise noted)
V_{DD}=+11V±5%, 70mA(typ), 110mA(max.) V_{BB} = −2.2V + 5%, 0.2mA(typ), 2mA(max.)
V_{CC}=+5V±5%, 12mA(typ), 25mA(max) Operating Temperature (T_A)=0°C to +70°C

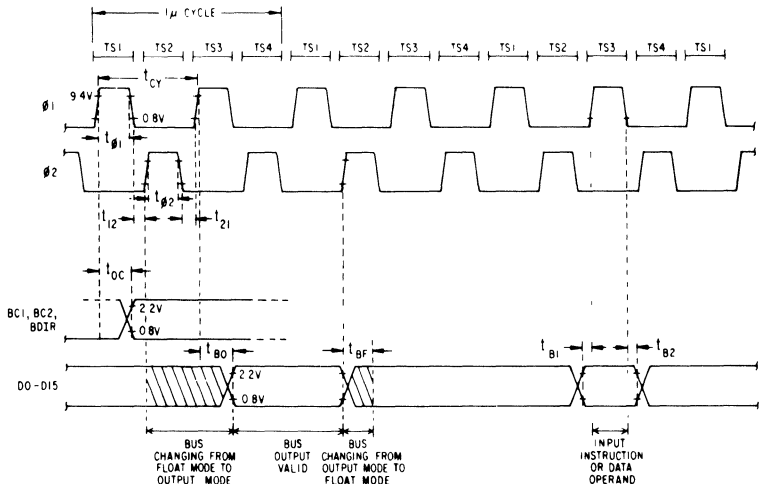
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	V_{IHC}	10	—	V_{DD}	V	
Low	V_{ILC}	0	—	0 6	V	
Input current	I_C	—	—	15	mA	$V_{IHC} = (V_{DD} - 1)V$
Logic Inputs						
Low	V_{IL}	0	—	0 65	V	
High (All Lines except BDRDY)	V_{IH}	2 4	—	V_{CC}	V	
High (Bus Data Ready Line See Note)	V_{IHB}	3	—	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2 4	V_{CC}	—	V	I_{OH} = 100μA
Low (Data Bus Lines D0-D15)	V_{OL}	—	—	0 5	V	I_{OL} = 1 6mA
Low (Bus Control Lines, BC1,BC2,BDIR)	V_{OL}	—	—	0 45	V	I_{OL} = 2 0mA
Low (All Others)	V_{OL}	—	—	0 45	V	I_{OL} = 1 6mA
AC CHARACTERISTICS						
Clock Pulse Inputs, φ1 or φ2						
Pulse Width	$t_{\phi 2}$, $t_{\phi 2}$	250		—	ns	
Skew (φ1, φ2 delay)	t_{12}, t_{21}	0	—	—	ns	
Clock Period	t_{cy}	0 5	—	2	μs	
Rise & Fall Times	tr, tf	—	—	15	ns	
Master SYNC:						
Delay from φ	tms	—	—	30	ns	
D0-D15 Bus Signals						
Output delay from φ1 (float to output)	t_{BO}	—	—	100	ns	1 TTL Load & 100pF
Output delay from φ2 (output to float)	t_{BF}	—	50	—	ns	
Input setup time before φ1	t_{B1}	0	—	—	ns	
Input hold time after φ1	t_{B2}	10	—	—	ns	
Bus Control Signals BC1,BC2,BDIR						
Output delay from φ1	t_{DC}	—	—	100	ns	
Skew	—	—	—	30	ns	
BUSAK Output delay from φ1	t_{BU}	—	150	—	ns	
TCI Output delay from φ1	t_{TO}	—	200	—	ns	
TCI Pulse Width	t_{TW}	—	300	—	ns	
EBCA output delay from BEXT input	t_{DE}	—	—	150	ns	
EBCA wait time for EBCI input	t_{AI}	—	—	400	ns	
CAPACITANCE						TA = +25°C; V_{DD} = +12V; V_{CC} = +5V; V_{BB} = −3V, tφ1 = tφ2 = 120ns
φ1, φ2 Clock Input capacitance	Cφ1, Cφ2	—	20	30	pF	
D0-D15	—	—	8	15	pF	
All Other	—	—	5	10	pF	

**Typical values are at +25°C and nominal voltages.

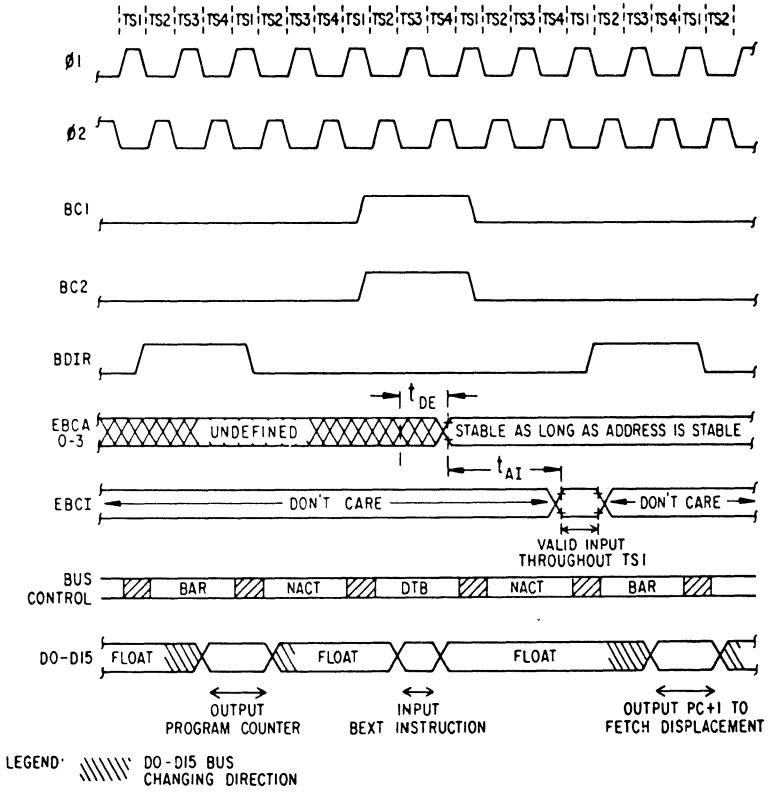
NOTE: The Bus Data ReaDY(BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration.

VIDEO

CLOCK AND BUS TIMING



TYPICAL INSTRUCTION SEQUENCE (EXTERNAL BRANCH TIMING)



VIDEO

TELEVIEW Data Acquisition Chip

FEATURES

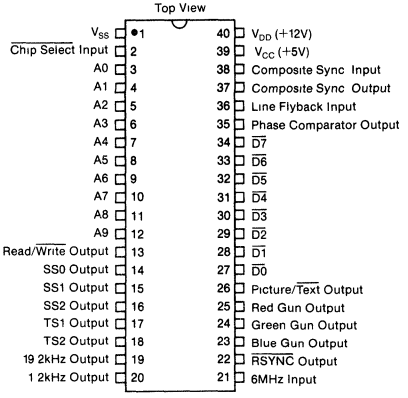
- Processes Teletext and Viewdata input data
- Direct interface with Teleview highways
- Direct interface with standard UAR/T (AY-3-1015D)
- TTL compatible serial Teletext data input
- Full checking of Teletext data including parity, Hamming and data frequency
- "Don't care" digit facility
- Non-used Viewdata control codes made available to control processor
- Addresses up to eight page Stores

DESCRIPTION

The Data Acquisition chip is one of the set of LSI devices comprising the General Instrument Teleview (Teletext/Viewdata) system. It receives data from a TV signal or Telephone Line via an appropriate interface and processes the data accordingly. Under instruction from a control device, it acquires the requested data and loads it into the correct location in the preselected page store. Control information extracted from the incoming data is provided to the Teleview system.

The device is fabricated in the General Instrument N-channel metal gate MOS process providing direct TTL interfacing, high speed, and good reliability. It is supplied in a 40 lead dual-in-line package.

PIN CONFIGURATION



PIN FUNCTIONS

Pin Number	Name	Function
1	V_{SS}	Negative supply for the device and the reference for all signals and electrical parameters.
2	TELETEXT/DS INPUT/OUTPUT	When strapped to ground (low level), will process Teletext. In Viewdata it is the data strobe output to the UAR/T (active low).
3-12	A0 to A9	10 address bits connected to the Teleview System Address Bus. As outputs, they are tri-state and active push-pull for high speed Store driving.
13	Read/Write Output	Read/Write control of the page Stores. The Stores will output data (read) when signal is high.
14-16	SS0-SS2 Outputs	Three bits of Store Select code enabling one of the eight page Stores.
17	RSYNC Input/ Output	A low going pulse indicates the start of a Teletext line. The chip will output a low going pulse within a few microseconds to re-synchronize the Data Grabber.
18	TS2 Input	The second of the two time slot bits which, when true, indicates that the chip may use the Data and address highways.
19-25	RD1—RD7 Inputs	Received Data taken directly from the UAR/T.
26	Parity Error Input	Parity error signal from the UAR/T.
27-34	D0-D7	Data I/O's for connection directly to the Teleview Data highway. As output, the active state is low and there is a passive pull-up on chip so that signals on the highway may be 'wire-ored.'
35	RDAV Output	Low active signal to the UAR/T which will reset data available output.
36	DAV Input	The Data Available signal from the UAR/T to indicate a character is available at the RD1-RD7 pins.
37	Teletext Data Input	Serial data input from Data Grabber. TTL compatible. If not used, this input should be held low.
38	Clock Input	Normally the Teletext clock running at 6.9375MHz and synchronized to the Teletext data by RSYNC. In Viewdata, a 6MHz clock (as used by the Video generator) may be input here. TTL compatible.
39	V_{CC}	Connected to +5V. This has a low current requirement and is used mainly for the output drivers.
40	V_{DD}	Connected to +12V, the main positive supply for the device.

OPERATION

The Data Acquisition (DA) chip takes data from either the TV (Teletext) or telephone line (Viewdata) via the appropriate interface, processes it accordingly to type and user requests, and loads the display data in the correct position in one of eight page Stores.

The processing of Teletext and Viewdata information is described in separate sections as is the interchange of data with the rest of Teleview system.

TELETEXT

If pin 2 is held low the DA may receive data via the serial Teletext data input.

While TS2 is true the DA will monitor $\overline{\text{RSYNC}}$ and the address highways. If a pulse appears on $\overline{\text{RSYNC}}$ it will process a Teletext data-line. At other times while TS2 is true it will respond to signals on the address highway and interchange data with a Control Device.

While TS2 is false the DA will be inactive.

TELETEXT DATA RECEPTION

Data is extracted from the TV video signal by an external circuit called the Data Grabber. This circuit provides a serial data signal and a clock to the DA input.

A 0.5μs negative pulse generated by the AY-3-9725 Video Generator will appear on the $\overline{\text{RSYNC}}$ line just before the data on a possible Teletext line. This pulse stops the clock in the low state and primes the AY-3-9710 to monitor the Teletext Data Input for clock run-in. The first negative transition restarts the clock which is used as a reference against which to compare the incoming signal. If the frequency is correct the AY-3-9710 outputs a second $\overline{\text{RSYNC}}$ pulse which allows accurate resynchronization of the clock for the rest of the Teletext line. If the frequency clock fails the AY-3-9710 goes back to the idle state waiting for a new $\overline{\text{RSYNC}}$ signal or the Data Interchange time.

After a valid clock run-in has been detected, Teletext data is clocked into a serial-to-parallel converter and Framing Code detector. A time out will cause the DA to go idle, while the detection of Framing Code will byte synchronize the S-P converter and start the DA receiving the Teletext data.

The first two words following the Framing Code have data protected by Hamming Code and the appropriate checks and corrections are performed. If the row address indicates that the data is a Page Header (Row 0) then the following 8 words are also processed by the Hamming Code circuit. If any Hamming Code fails such that it cannot be corrected, then that data line is rejected.

Requests for pages of Teletext data are input to the DA during Data Interchange periods, described later. When a new page is selected the Page and Time store in the DA is loaded with all '1's indicating "don't care" digits. As keys are pressed by the user of the Teleview system, the values are loaded into the DA in the appropriate position.

A comparator in the DA compares Magazine, Page and Time digits one at a time as they are received in the data stream with the digits stored. The comparator will give a true output if the digit compares exactly or if the stored digit is all 1 (value 15). Where an incoming digit has a range less than 4 bits, e.g. time hours tens has the range 0-3 or 2 bits, the unused bits will be made to compare.

Every line of data received is checked for comparison on Magazine number. If this does not compare and the row address indicates that the row is not a Page Header than that row is rejected.

If the magazine number does not compare and it is a Page Header then, with the exception of Rolling Headers, it is again rejected.

From the time that the DA is told that the P key has been pressed until the selected page has been captured for the first time, all Page Headers that compare on Magazine number are loaded into the Store except those with the Interrupt Sequence bit (C9) set. This mode of display is referred to as Rolling Headers and provides an indication to the user that data is being received. During this mode the Magazine Serial bit (C11) will override the Magazine comparison. A page of data may be captured when the page number has been fully entered, i.e. the 3rd digit has been received or the T key has been pressed, and a Page Header is received whose magazine, page and time digits compare with those stored in the DA. That header and all subsequent data lines with correct Magazine number will be stored up to and excluding the next Page Header of correct Magazine number. A 'Page being received' indication will be set at this time for transmission to the Control device.

Whenever a Page Header is received that fully compares the accompanying Control bits, that Header will be stored for subsequent transmission to the Control.

When the content of a data line is ready to be stored, that data is loaded into the appropriate Store as defined by the signal from the Control device. The position in the Store is defined by the Row Address of that data line, the location of the first character being 40 times the Row Address (with the exception of the Page Header which does not have the first 8 characters), with following characters being stored in the next 39 locations of Store.

Each character is checked for odd parity and if the check fails, that character is not written. The write signal is removed to avoid overwriting a possible valid character already existing in Store.

The last eight characters of every Page header contain the current clock time and are always written to Store.

VIEWDATA

With pin 2 connected to the Data Strobe input to a UAR/T and not held to ground the DA will process Viewdata.

While TS2 is true the DA is active as far as the Teleview highways are concerned and it will monitor $\overline{\text{RSYNC}}$ and the Address highway.

When an $\overline{\text{RSYNC}}$ pulse appears the DA will process any Viewdata character it has available. Whenever it is not processing characters it may receive characters asynchronously from the Telephone Line, via the exclusive connection to the UAR/T, and store them within the DA. Up to three characters may be received and stored before the next processing period when they may be loaded into the page Store. Data interchange with the Teleview system may occur when TS2 is high.

ASYNCHRONOUS DATA RECEPTION

The standard UAR/T will convert the serial data via the modem to parallel data for inputting to the DA and indicate a character is ready by the Data Available (DAV) line. At any time, except when actually processing previously received characters, the DA will read the data and acknowledge on $\overline{\text{RDAV}}$, a minimum of 3μs after the DAV signal.

VIEWDATA CHARACTER PROCESSING

The eight bit input consists of seven bits of data plus a parity fail indication. Characters intended for storage are loaded into the Store in a location determined by the Character Address counter which is always arranged to point to the position in Store into which the next character will be written. The counter is manipulated by the Control Characters appearing in Columns 0 and 1 in the character table.

- 0/ 8, Back Space, will cause the Character Address counter to be decremented by one.
- 0/ 9, Horizontal Tab, will cause the Character Address counter to be incremented by one.
- 0/10, Line Feed, will increment by 40.
- 0/11, Vertical Tab, will decrement by 40.
- 0/12, Form Feed, will reset to zero.
- 0/13, Carriage Return, will position the Character Address counter to the beginning of the current block of 40.
- 0/14, Cursor Home, will reset to zero.

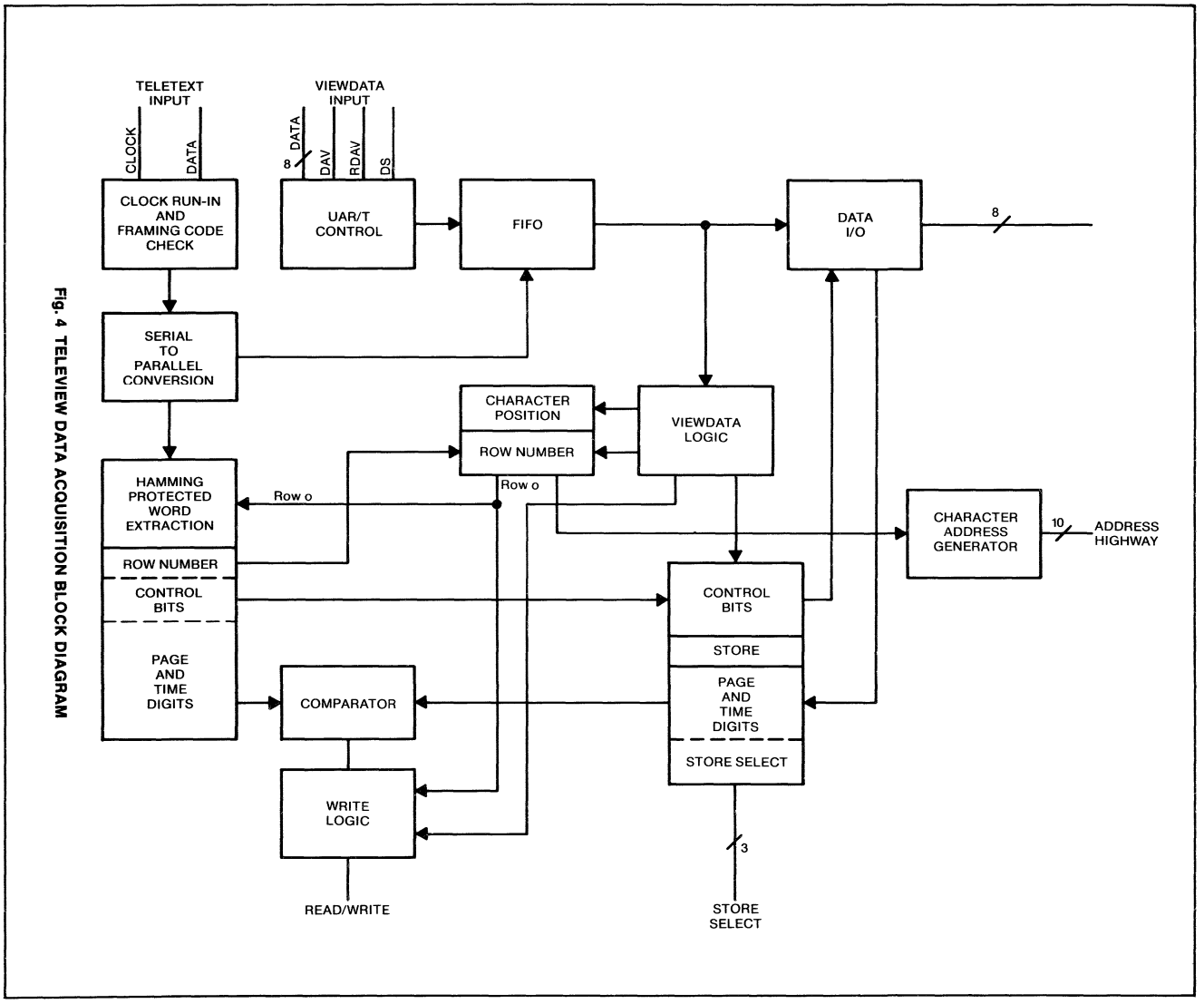


Fig. 4 TELEVIEW DATA ACQUISITION BLOCK DIAGRAM

A character in columns 2-7 will be written into the appropriate Store at the location indicated by the Character Address counter which will then be incremented by one.

The ESC character (1/11) will cause some modification of the subsequent character as follows:

If the character is in columns 4 or 5 it will be written to Store with the most significant bit changed to Zero.

If the character is in column 3 it will not be written to Store but made ready for transmitting to the Control device.

Any other characters, except NUL, will cancel the ESC sequence and be ignored.

The Form Feed character (0/12) will cause the F bit to be set in the appropriate DA to Control signalling word.

All other control characters in columns 0 and 1, except NUL, will be sent to the Control at the appropriate time.

If any character has the parity fail indication set then the character 7/15 will be written to Store. At the start of a processing period (i.e. at $\overline{RSYNC}$) if a character is available for processing then the DA will erase the Cursor bit by reading the location pointed to by the Character Address counter and re-write it. Since the DA never writes the 8th bit in the Store the cursor will be removed.

DATA INTERCHANGE

During the DA's active period, indicated by TS2, when it is not performing any data processing then it will monitor the Address highway for the following codes:

1111XXXX0X	indicates the DA should receive data from the data highway.
1111XXXXX0	indicates that the DA should send data to the data highway.
1111X0XXXX	indicates that the DA should provide control to the UAR/T.

In the Receive mode the Control device may send data according to the codes in Table 1. The most significant bit of the data acts as a strobe which will cause the other 7 bits to be received and stored in the DA. Magazine, Page and Time digits will be stored in the appropriate location in the digit store, the Store Select number will be stored for use when accessing the Store and the indications of P and T keys being processed will also be latched for use in the processing period.

The receiving of data from the Control is completely asynchronous to the DA internal clock and is controlled entirely by the Strobe bit.

The Send mode will cause the DA to apply the first code, shown in Table 2, to the data highway. When the code has been read by Control, the signal will be acknowledged by Control forcing all 1's (low levels) which will step the DA onto the second word and so on. The Strobe bit is used in this case to indicate that the data is appearing for the first time and, once read by Control, is cleared until new data is available. The exception is the first word which always has the Strobe set.

The UAR/T control is recognized by the DA since it has the UAR/T connections and in this mode a Strobe on the data highway will cause the DA to provide a data strobe $\overline{DS}$ to the UAR/T.

During the Data Interchange period the DA will monitor the Store Select lines and if they are all taken low it will output the current content of the Character Address counter to the address highway so that the Control may know where to insert the cursor.

Table 1 CONTROL TO DATA ACQUISITION SIGNALING

Active low signaling, most significant bit is a strobe.

Highway Free		0	0	0	0	0	0	0	0
Magazine Number		1	0	0	0	D	d	d	d
Page Number,	tens	1	0	0	1	D	d	d	d
	units	1	0	1	0	D	d	d	d
Store Select		1	0	1	1	0	S	s	s
Key Pressed		1	0	1	1	1	0	K	k
Spare Code		1	0	1	1	1	1	0	0
Spare Code		1	0	1	1	1	1	0	1
Spare Code		1	0	1	1	1	1	1	0
Dummy Code		1	0	1	1	1	1	1	1
Time Hours,	tens	1	1	0	0	D	d	d	d
	units	1	1	0	1	D	d	d	d
Minutes,	tens	1	1	1	0	D	d	d	d
	units	1	1	1	1	D	d	d	d

Where Kk is key identification:

P	0 0
T	0 1
Spare 1	1 0
Spare 2	1 1

Sss is store select number, 000 to 111.

Dddd, Digit key value, initially values 0-9 and 15 used although any value may be sent. For Teletext the Magazine range is 0-7, Time hours tens range 0-3, Time minutes tens range 0-7. In addition digit 15 is recognized by the DA as a 'don't care' digit causing automatic comparison.

Table 2 DATA ACQUISITION TO CONTROL SIGNALING

Active low signaling, most significant bit is a strobe. Signals acknowledged by the Control forcing all ones Control word 1 is sent first and is always sent.

Control word	1	1000 T S s s
Where	T	is the Teletext bit, 1 = Teletext.
	Ssss	is the Store Select number the DA is currently using.

Control words 2-4 depend on whether Teletext or Viewdata is being processed.

TELETEXT

Control word	2	1001	PBR	C4	C6	C5
	3	1010	C10	C9	C8	C7
	4	1011	C14	C13	C12	C11

Sent* only when Valid Header received. PBR is set while a page is being received. C4 to C14 are the Teletext Control bits.

VIEWDATA

Control word	2	1001	X	F	0	0
	3	1010	b7	0	b6	b5
	4	1011	b4	b3	b2	b1

Sent* only when a Control character received by DA. F is set when Form Feed character processed. b1-b7 are the 7 bits comprising the Viewdata Character.

NOTE:* 'Sent' means the Strobe bit is set. The other seven bits are put onto the highway at the request of the Control and may be used if appropriate (e.g. page being received).

VIDEO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} ..... −0.3V to +15V
Storage Temperature ..... −55° C to +150° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Standard Conditions (unless otherwise noted):

Supply Voltages: V_{SS} = 0V (substrate voltage)
V_{CC} = +5V ± 5%
V_{DD} = +12V ± 10%
Temperature Range: 0° C to +70° C

Data labeled "typical" is presented for design guidance only and is not guaranteed

Characteristics	Min	Typ	Max	Units	Conditions
OUTPUTS					
Address Outputs (tri-state)					
High level	+2.4	—	V_{CC}	V	I_{OH} = −320μA
Low level	—	+0.2	+0.45	V	I_{OL} = 3.2mA
Capacitance	—	—	15	pf	V = 0V
T rise, T fall	—	—	200	ns	C_{LOAD} = 100pf
Leakage, high impedance state	—	—	5	μA	V_{OUT} = 0V or +5V
Data Outputs (passive pull-up)					
High Level	+2.4	—	V_{CC}	V	I_{OH} = −1.5mA
Low Level	—	+0.2	+0.45	V	I_{OL} = 3.2mA
Capacitance	—	—	15	pf	V_{OUT} = 0V
R/W and Store Select Outputs					
High Level	+2.4	—	V_{CC}	V	I_{OH} = −320μA
Low Level	—	+0.2	+0.45	V	I_{OL} = 3.2mA
Capacitance	—	—	15	pf	V_{OUT} = 0V
Current sourced, 'off' state	1.2	—	2.6	mA	V_{OUT} = 0V
$\overline{RDAV}$ and $\overline{DS}$ Outputs					
High Level	+2.4	—	V_{CC}	V	I_{OH} = −25μA
Low Level	—	+0.2	+0.45	V	I_{OL} = 100μA
Capacitance	—	—	15	pf	V_{OUT} = 0V
$\overline{RSYNC}$ Output (Open Drain)					
Low Level	—	+0.2	+0.45	V	I_{OL} = 4mA
Leakage, output off	—	—	10	μA	V_{OUT} = +12V
INPUTS (except Clock and Teletext Data)					
High Level	2.2	—	V_{DD}	V	
Low Level	V_{SS}	—	+0.8	V	
Leakage (except I/O's)	—	—	10	μA	V = +12V
Input Capacitance	—	—	15	pf	V_{IN} = 0V
DAV Input	—	20	—	μA	V_{IN} = +5V
Clock and Teletext Data Inputs					
High Level	2.8	—	V_{DD}	V	
Low Level	V_{SS}	—	0.4	V	
Capacitance	—	—	20	pf	V_{IN} = 0V
Leakage	—	—	10	μA	V_{IN} = +12V
Frequency	1.0	—	7.5	MHz	
Power					
V_{CC} Supply Current	—	—	15	mA	V_{CC} = +5.0V
V_{DD} Supply Current	—	—	65	mA	V_{DD} = +12V (at 25° C)

VIDEO

TELEVIEW 625 Line Interlace/Non Interlace Video Generator

FEATURES

- Interlaced 625 line or non-interlaced 313 line operation
- 24 row x 40 character display
- Character Set options available
- On and Off Hours operation
- Half Page Expansion
- Boxed Clock and Header on Teletext
- Direct interfacing with the TELEVIEW busses
- Provides master timing signals for other TELEVIEW chips to indicate status of the display scan
- Address up to eight Page Stores
- Provides address information to scan allocated Page Store
- Provides composite synchronizing signals for receiver for 'Off-Hours' working
- Provides comprehensive set of display facilities
- Allows Teletext reception on lines 7-22

DESCRIPTION

The Video Generator Chip is one of a set of LSI chips used in the General Instrument TELEVIEW (Teletext/Viewdata) system. It reads the contents of a Page Store and generates outputs suitable for driving a normal 625 line Color Television receiver to display the contents of the Page Store.

The chip also monitors the composite synchronizing signals within the receiver and locks the total TELEVIEW system onto the incoming interlaced signals. When no transmission is taking place, the chip generates an interlaced or non-interlaced composite sync signal which is used to synchronize the receiver.

A full set of color display facilities as described in the Broadcast Teletext Specification (September 1976) is provided by the device.

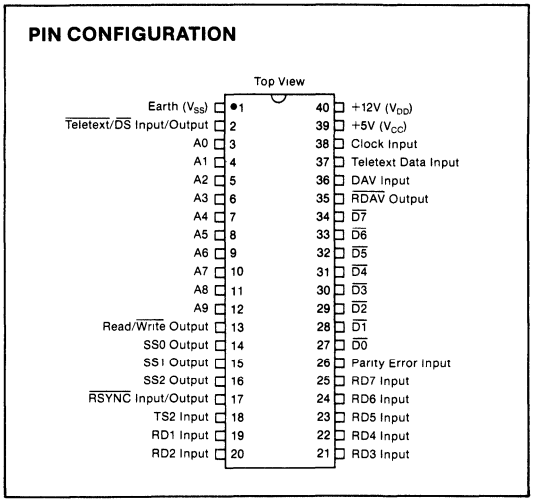
The device is fabricated in the General Instrument N-Channel, metal gate, MOS process providing direct TTL interfacing, high speed, and good reliability.

DISPLAY FACILITIES

1 Provides the following display facilities controlled by Control characters read from the store i.e. via the TELETEXT/VIEWDATA transmission.
   a. Alpha-numerics/Graphics in seven color set
   b Color or black backgrounds.
   c Selected characters may be concealed
   d Selected characters may be flashed
   e. Characters may be boxed into the normal Television Picture. This can be done manually or automatically.
   f. Characters may be either single or double height.
   g. Graphics characters may be contiguous or separated.
   h Graphics characters may be held during other control characters
   i Special graphics for high resolution applications.

2 Provides the following display facilities controlled from the user's keyboard/keypad via the control chip.
   a. Switch between normal and data video
   b Teletext or Viewdata Operation.
   c. Clock time can be boxed into a normal picture (Teletext only).
   d. Display of one half page in double height.
   e. Monochrome output of data Mix Mode.
   f. Inhibiting of character rounding and flashing.
   g. Enabling of a cursor
   h. Inhibit the display until updated.
   i. Reveal concealed characters.

PIN CONFIGURATION



CHARACTER SETS

English	AY-3-9735-002
German	AY-3-9735-003
Finnish/Swedish	AY-3-9735-004
Italian	AY-3-9735-006

VIDEO

PIN FUNCTIONS

Pin Number	Name	Function
1	V_{SS}	This is the negative supply for the chip and is used as a reference for all electrical parameters.
2	$\overline{\text{Chip Select}}$ Input	The chip can be put in its deselected state by connecting this input to V_{CC}. The input has an internal pull down to V_{SS}. If connected to V_{DD} the test mode is selected.
3-12	A0-A9	These pins are connected to the Address Bus of the TELEVIEW system. They are used for address Input/Output.
13	Read/$\overline{\text{Write}}$ Output	This output is used to drive the Random Access Memories forming the Page Memory.
14-16	SS0-SS2 Outputs	These binary coded outputs are used to select the required Page Store.
17,18	TS1, TS2 Outputs	These outputs are generated by the Video Generator from the status of the raster scan and are used to indicate this status to other chips within the TELEVIEW system.
19,20	19.2KHz and 1.2KHz Outputs	These outputs provide 19.2KHz and 1.2KHz square wave signals which are used by the UAR/T as reception and transmission clocks respectively.
21	6MHz Input	This input is fed from a 6MHz oscillator which is phase locked to the normal transmission for Teletext On Hours operation. During Off Hours working a free running crystal oscillator is normally used.
22	$\overline{\text{RSYNC}}$ Output	Open-drain output, used to indicate the presence of Teletext lines to the DA Chip and Data Grabber.
23-25	Red, Green and Blue Outputs	Push-pull outputs which go high to turn on the relevant color gun for displaying. These outputs are closely matched for propagation delay and rise and fall times.
26	Picture/$\overline{\text{Text}}$ Output	This output may be used by the TV receiver to determine whether to display the normal TV Picture or the generated Text as provided at the Red, Green and Blue outputs. In the mix mode this generates monochrome video. It will then be matched to the gun outputs for propagation delay and rise and fall times.
27-34	$\overline{\text{D0}}$-$\overline{\text{D7}}$ Inputs	The Data Inputs form the communication highway between the Video Generator and the Control Processor and Page Memory.
35	Phase Comparator Output/Interlace Select Input	In On Hours operation the display Line Flyback signal is compared for phase with an internal 64μs period signal derived from the 6MHz display clock. The output is a pulse which produces a voltage for controlling the frequency of a 6MHz display oscillator, thus locking the display to the incoming picture. In Off Hours operation this open-drain output goes high permanently, and thus can be used as an indication of On Hours/Off Hours status. When this output is high the oscillator must run fast and when this output is low the oscillator must run slow. In Off Hours operation, if the Phase Comparator output is held low a 313 line non-interlaced sync is provided at the Composite Sync output. If the Phase Comparator output is pulled high connected to V_{CC} via a 4.7K resistor, interlaced sync will be provided.
36	Line Flyback Input	The Line Flyback input is a signal from the display deflection circuitry which is used for positioning the display on the TV screen. Line Flyback pulses are positive. If no Line Flyback is provided in Off Hours mode the display will be positioned so that the start of video is approximately 16μs after the negative edge of line sync.
37	Comp Sync Output	Open-drain output. In On Hours working or in Picture mode it outputs a regenerated composite sync signal from the composite sync input. In Off Hours working it outputs an internally generated composite sync.
38	Comp Sync Input	The composite sync input monitors the composite sync/video being received and extracts synchronizing information and On Hours/Off Hours information for the Video Generator. This input must be predominantly high for Off Hours switching. Sync pulses are negative.
39	V_{CC}	This pin is connected to the +5V supply.
40	V_{DD}	This pin is connected to the +12V supply.

CHIP DESCRIPTION

The Video Generator Chip contains the logic and control functions to interrogate a selected TELEVIEW Page Store and display the contained information at the correct period within the raster scan on a normal TV receiver. The chip also generates the master timing signals TS1 and TS2 which indicate the raster status to the Control processor and Data Acquisition chips.

Comp Sync Generator and On Hours Detector — The prime function of this block is to detect negative going sync signals from the Incoming mixed sync and to synchronize the TELEVIEW system with the transmitted signal. When the incoming transmission is turned off, (i.e. goes Off Hours), this is recognized by the detector after at least 300ms of missing sync pulses. An internally generated Composite Sync is then switched to the Composite Sync out pin. Thus the receiver will continue in lock but synchronized to the Video Generator. Similarly if the normal transmission resumes, the fact that external sync pulses are being received is recognized by the Video Generator and the chip will re-synchronize itself with the incoming transmission. Because the Video Generator is aware of the status of the mixed sync at all times the chip can detect frame sync, line sync and even and odd frames. Thus with this information the chip can continuously monitor the current line number. The relevant sections of the line scan are decoded and are indicated externally by the TS1 and TS2 time slot outputs:

a. Writing to RAM. TS10
   This occurs during lines 7 to 22 under control of the DA chip.
b. Reading from RAM. TS00
   This occurs under control of the Video Generator chip between lines 48 and 288, and is when the display is active.
c. Data Interchange Period. TS11
   The interchange of information between DA, Control Processor and Video Generator occurs during this period (lines 23-47).
d. Spare TS01
   During lines 289-006 the Video Generator does not use the Data Bus.

As the chip is aware of the raster status it also starts and stops the address counter/latch combination which is used to scan the relevant Page Memory.

Character Counter and Address Logic — The address counter is a binary counter which is incremented at the Character Display Rate (1MHz). It can also be loaded from a latch which contains the start address of each character row. Since each character consists of 10 vertical lines of raster scan, the counter is incremented 40 times from a start address and then is reloaded with the same start address ready for the next raster scan of the same forty characters. This occurs nine times. On the last line the counter is incremented once and this new address is stored in the latch. This address being the start address of the next row of forty characters. The above sequence is then repeated.

If displaying only one half of a page with all characters in double height, the Video Generator scans the same forty addresses nineteen times and stores the new address on the twentieth raster scan. If it is in the bottom half of the page, the address counter is initialized to 480.

The display format of 40 characters, each 1μs wide occurs on a line of 64μs duration thus leaving a border of 12μs at each end of the character row. This address counter is actually started some 4μs before the start of the proper character display thus allowing time for address generation, RAM access time, ROM access time and display processing, these actions being pipelined. Facilities are also provided such that the output address can be reduced by 40 thus allowing accessing of the character in the row above. This is a necessary operation for a Double Height display option which will be described later. This facility is inhibited while displaying on half of a page. The address so produced is presented on the address bus and the required Page Memory is activated by the Store Select Outputs. The address drivers are tristate thus allowing easy bus interface, being active for 40μs starting 3.5-6μs after LFB.

Input Latches and Character Read Only Memory — The data being read from the required Page Memory is placed on the Data Bus and is latched into the Data Bus latches. A total of 450ns is allowed for the RAM read cycle and thus quite slow Random Access memories may be used. Having been latched by the Video Generator chip the seven bit character is used to address the character Read Only Memory. This memory is organized as 96 characters each of 45 dots (5x9 array).

Data Control Latches (Color Background Control) — Certain characters indicate to the video generator a change in display status. These characters are contained within columns 0 and 1 of the character set and may be used to change character color, background color, height, etc.

Output Logic and Drivers — The output logic reads the character ROM into a six bit parallel to serial shift register. This operation occurs at the left-hand side of the character to be displayed, the data in the register is then shifted out at 6MHz (character dot-rate) the data bits selecting between character and background information. This information is used to drive the fast Gun output drivers. These outputs are closely matched for propagation delay and rise and fall time to ensure good legibility.

DATA INTERCHANGE

During the TS11 timeslot the Video Generator can receive information from other devices attached to the TELEVIEW system busses. This is normally used by the control chip to update the control and display latches within the Video Generator. The Video Generator is enabled to receive by putting the address 111XXOXXXX on the address highway (active high).

The latches are updated by the following control words, active low signaling, most significant bit is a strobe.

Highway Free	0000	0	0	0	0	
Control Word 1	1000	T	S	s	s	
Control Word 2	1001	X	C_4	C_6	C_5	Teletext
Control Word 3	1010	C_{10}	C_9	C_8	C_7	Teletext
Control Word 4	1011	C_{14}	C_{13}	C_{12}	C_{11}	Teletext
Control Word 2	1001	X	F	0	0	Viewdata
Control Word 3	1010	b_7	0	b_6	b_5	Viewdata
Control Word 4	1011	b_4	b_3	b_2	b_1	Viewdata
Store Select for Display	1100	SP	D	d	d	
Key Data	1101	*	P	*	*	
Other Facilities	1110	X	BH	M	BC	

The Control bits are as follows: —

T	TELETEXT Mode i.e. not VIEWDATA
Sss	Identification of Store being written
Ddd	Identification of Store being displayed

(a) Teletext

C_4	Erases rows 1-23 of Store defined by Sss and resets Reveal if Sss = Ddd
C_5	Newsflash
C_6	Subtitle
C_7	Suppress Header
C_8	Update Indicator
C_9	No action
C_{10}	Inhibit display
C_{11}	No action
C_{12}-C_{14}	No action (may be programed to enable and disable the chip)

VIDEO

Character Rounding — Characters are normally rounded by adding half dots to smooth diagonals. For normal height characters the extra TV lines made available by interlace are utilized for this and so if in non-interlace mode single height characters cannot be rounded.

Character rounding can be inhibited totally by a signal from Control and in this mode, intended specifically for printers, flashing is also suppressed. Reset by P key or new Viewdata page.

Cursor — The cursor is stored as the 8th bit of the appropriate character in the Data Store. When switched on it is displayed as a bar on the bottom line of the character rectangle flashing between foreground color and black in antiphase to normal flashing characters.

Non Interlaced Operation — When interlaced composite sync is input to the chip it operates in normal Interlaced Mode and regenerates interlaced composite sync.

If there is no incoming sync the chip switches to the OFF hours mode.

If the Phase Comparator output is pulled high, e.g. 4.7K to V_{CC}, Interlaced Sync is output. If the Phase Comparator output is held low Non-Interlaced Sync is output and character rounding for single height characters is inhibited.

VIDEO

SIGNAL DETECTION CRITERIA

(For On Hours Operation)

The Video Generator detection circuitry for incoming sync signals is designed to prevent misoperation in the presence of noise. The criteria for detection is defined below.

Line Sync — The Composite Video Input must be negative for greater than 3μs.

Frame Sync — The Composite Video Input must be negative for greater than 12μs and at least 310 lines (Line Flyback pulses) must have occurred since the previous Frame Sync detection.

Odd Frame Detection — Odd Frame Detection occurs when a Line Flyback pulse falls in a window 12-39μs after frame Sync Detection. This is used to lock the line counter.

On Hours/Off Hours Detection — The incoming line flyback and line sync pulses are compared to determine whether a valid transmission is being received. Lack of coincidences/frame are accumulated and if more than 16/frame occur for a period 350-1000ms the logic deems that a valid transmission is not being received and the chip switches Off Hours. If however, less than eight occur in any two successive 1/2 frames, the logic deems that a valid Composite Sync is being received and the system goes On Hours.

For the chip to be able to look for synchronism the following phase relationship between Line Flyback and Composite Sync must be satisfied.

(a) Earliest back edge of LFB is 2μs after leading edge of line sync.

(b) Latest leading edge of LFB is 2μs after leading edge of line sync.

(c) Latest back edge of LFB is 12μs after leading edge of line sync.

The minimum length of the LFB pulse is 8μs.

6MHz Display Oscillator — The 6MHz display oscillator must run fast in the OFF Hours mode but not so fast that the On/Off Hours detection criteria cannot be satisfied. This sets a maximum offset of +1.5KHz, the minimum offset is set by lock time criteria and would typically be +0.5KHz.

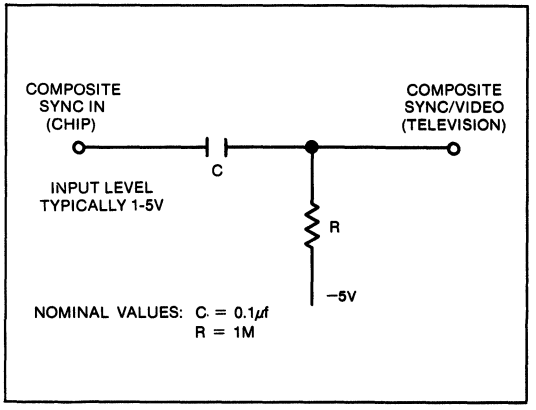
The frequency range of the oscillator must extend below the 6.0MHz nominal frequency. The minimum frequency should be at least −0.5KHz but can be as low as convenient.

COMPOSITE SYNC INPUT

On-chip dc restore is provided which allows simple interfacing to the television, either Composite Sync signals or video being acceptable.

As the Composite Sync/Video signal from the television may not be referenced to the system ground it is ac coupled to the chip.

A typical Interface Circuit is:



(b) Viewdata

b_7-b_1		
001 0001	Cursor ON	The two Control Words that make up these codes must be transmitted in numerical order in the same TS11 timeslot.
001 0001	Cursor OFF	
F	Form feed or first appearance, Erases store defined by Sss, resets Reveal if Sss = Ddd	
SP	Sets Picture/Text to picture (for initialization)	
P	P Key pressed. Resets Reveal, Half Page Expansion, Newsflash/Subtitle (Auto Box), Suppress header, Inhibit display, Update.	
M	Mix Mode	The latches are set and reset by the appropriate bit
BC	Box Clock (TELETEXT only)	
BH	Box Header (TELETEXT only)	
***	These are coded as follows:	
001	Picture/Text Key pressed	Latches toggled by the appropriate code
010	Reveal/Conceal Key Passed	
011	½ Page Key Pressed (Cycles Full, Top, Bottom, Full, etc)	
100	Update/Clear Key pressed	
101	Rounding and Flashing OFF (Reset by P Key or new VIEWDATA page)	
111	Hold (not used by AY-3-9735)	

DISPLAY OPTIONS

Logic is contained on the Video Generator chip to process the Display Modes as described in the Broadcast Teletext Specification. These facilities are outlined below.

Character Set — The chip can display 96 Alphanumeric characters and 64 Graphic shapes which may either be contiguous or separated. The alphanumeric format is determined by a 4320 bit Read Only Memory organized as:

96 (characters) x 5 (dots) x 9 (lines) = 4320

This can be programed for different character fonts

The graphic shapes are determined directly from the bits of the character code.

Display and Background Color — The characters and the background can be displayed in one of seven colors. In addition the background may be black. This information is stored in two sets of three latches representing character and background colors.

Conceal and Flash — Selected characters can be concealed and optionally revealed by the viewer. Selected characters can be flashed on command. The flashing is controlled by an on-chip flash oscillator. During the flash period or when concealed, only background information is displayed. The flash rate is 1.56Hz.

Boxing — Text or graphics characters can be boxed into a normal video picture. While in Picture mode boxing is automatic if Newsflash or Sub-title and Sss = Ddd. Other boxed characters may be manually revealed by Reveal command.

Double Height — Double height characters are characters contained between the control characters Double Height and Normal Height or end of line. When a Double Height control character is read from the RAM only the top half of the subsequent character is displayed during the 10 raster scans. During the next 10 scan lines 40 is subtracted from the addresses being output on A0-A9 so the same 40 addresses are read from another 10 times. Characters which are not double height are displayed as the background color and the bottom of the double height character is displayed.

Hold Graphics — When this latch is set, any subsequent control characters (except change Double/Normal Height or Change Alpha/Graphics) are displayed as the last graphics character.

Special Graphics — While in Graphics Mode the Special Graphics command will give a special high resolution facility. In this mode there is a one to one correspondence between data bits b1, b2, b3, b4, b5, b7 and the six dots in each horizontal line of a character. This gives a possible graphics resolution of 6 x 20 for each character in interlace mode (or 6 x 10 if not interlaced).

Box Clock — When box clock is selected in Picture mode and Teletext the last eight characters of the page header are boxed in double height. To ensure that the live clock is displayed the store address is temporarily switched to that defined by Sss. This function is cleared in text mode.

Box Header — When box header is selected in Picture mode and Teletext the page header is boxed in double height (not if bottom half of page selected).

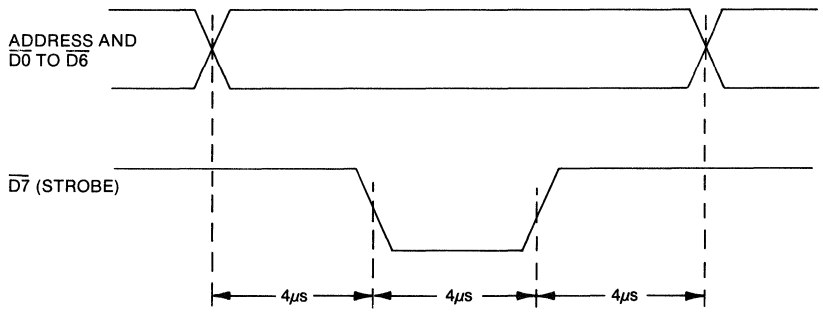
Half-page Operation — This allows either the top or bottom half of a normal Teletext/Viewdata page to be displayed over the whole screen, with each character in double height. This makes the display header easier to read from a distance. Double height characters are ignored in this mode.

Monochrome Output/Mix Mode — In normal operation the Picture/Text Output is used to blank the normal picture information for boxing or displaying a page of text.

In the mix mode this outputs Monochrome text information which is matched to the Gun Output signals in delay and drive. This can be used to superimpose text onto a picture by cutting away the picture below text data or as an output for Monochrome displays or printers. In this mode colored backgrounds are suppressed for viewing clarity. The output is at a low level to display a character.

VIDEO

TYPICAL TIMING DIAGRAM FOR INPUT DATA STROBING



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} . . . . . −0.3 to +15V
Storage Temperature Range . . . . . −55°C to +150°C

Standard Conditions (unless otherwise noted):

V_{SS} = 0V (Substrate voltage)
V_{CC} = +5V ± 5%
V_{DD} = +12V ± 10%
Operating Temperature Ranges (T_A): 0°C to +70°C
Clock Frequency 6.0MHz

*Exceeding these ratings could cause permanen damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics	Min	Typ**	Max	Units	Conditions
INPUTS					
Chip Select					
Input Logic High	2.2	—	V_{CC}	V	
Input Logic Low	V_{SS}	—	0.8	V	
Input Current	10	25	100	μA	V_{IN} = 5V
Comp Sync					
Input Logic High	1.0	—	V_{CC}	V	
Input Logic Low	−0.3	—	0.05	V	See Note 1
Input Capacitance	—	—	15	pf	V_{IN} = 0V
Source Current	—	50	—	μA	V_{IN} = 0V
6MHz					
Input Logic High	2.8	—	V_{DD}	V	
Input Logic Low	V_{SS}	—	0.4	V	
Input Capacitance	—	—	25	pf	V_{IN} = 0V
Mark to Space Ratio	40:60	—	60:40		
Frequency	1.0	—	6.5	MHz	
Input Leakage	—	—	10	μA	V_{IN} = 12V
All Other Inputs					
Input Logic High	2.2	—	V_{DD}	V	
Input Logic Low	V_{SS}	—	0.8	V	
Input Capacitance	—	—	15	pf	V_{IN} = 0V
Input Leakage	—	—	10	μA	V_{IN} = 12V
OUTPUTS					
Addresses, Read/$\overline{\text{Write}}$ Store Select (Tri-State) (Note 2)					
Logic High Output	2.4	—	V_{CC}	V	I_{OH} = −320μA
Logic Low Output	V_{SS}	0.2	0.45	V	I_{OL} = 3.2mA
Capacitance	—	—	15	pf	V_{IN} = 0V
T rise T fall	—	—	200	ns	C_{LOAD} = 200pf
Leakage (Disabled)	—	—	10	μA	V_O = 0V, 5V
Time Slots (TS1, TS2) (Push Pull)					
Logic High Output	2.4	—	V_{CC}	V	I_{OH} = −320μA
Logic Low Output	V_{SS}	0.2	0.45	V	I_{OL} = 3.2mA
T rise T fall	—	—	200	ns	C_{LOAD} = 200pf
Comp Sync (Open Drain)					
Logic Low Output	V_{SS}	—	0.45	V	I_{OL} = 1.6mA
Logic High Leakage	—	—	10	μA	V_O = 12V
Capacitance	—	—	20	pf	V_O = 0V
Delay from Comp. Sync In.	—	—	1	μs	ON Hours only
$\overline{\text{RSYNC}}$ (Open Drain)					
Logic Low Output	V_{SS}	—	0.45	V	I_{OL} = 4.0mA
Logic High Leakage	—	—	10	μA	V_O = 5V
Capacitance	—	—	15	pf	V_O = 0V
Phase Comparator (Open Drain)					
Logic Low Output	V_{SS}	—	0.45	V	I_{OL} = 4.0mA
Logic High Leakage	—	—	10	μA	V_O = 12V
Capacitance	—	—	15	pf	V_O = 0V

**Typical values are at +25°C and nominal voltages.

NOTES: 1. Voltages below −0.3 volts should be current limited to 1mA.
2. All tristated when Chip $\overline{\text{Select}}$ = V_{CC} R.G.B. outputs also tristated when displaying picture and not mixed.
3. Picture/$\overline{\text{Text}}$ matched in mix mode only.

VIDEO

Characteristics	Min	Typ**	Max	Units	Conditions
R.G.B. Outputs Picture/Text Output (Tri-state) (Note 2)					
Logic High Output	$V_{CC}-1$	—	V_{CC}	V	$I_{SOURCE} = 2mA$
Logic Low Output	V_{SS}	—	1	V	$I_{SINK} = 5mA$
Capacitance	—	—	20	pf	$V_{IN} = 0V$
T rise T fall (10%-90%)	—	—	30	ns	$C_L = 30pf$
Differential T rise T fall	—	—	30	ns	$C_L = 30pf$ (Note 3)
Leakage (Disabled)	—	—	10	μA	$V_O = 0.5V$
19.2kHz, 1.2kHz Outputs					
Logic High Output	2.4	—	V_{CC}	V	$I_{OH} = -32\mu A$
Logic Low Output	V_{SS}	0 2	0.45	V	$I_{OL} = 320\mu A$
T rise T fall	—	—	1	μs	$C_{LOAD} = 100pf$
POWER					
V_{CC} Supply	—	25	40	mA	$V_{CC} = 5V$
V_{DD} Supply	—	50	80	mA	$V_{DD} = 12V$

**Typical values are at +25°C and nominal voltages.

NOTES:

1. Voltages below −0.3 volts should be current limited to 1mA.
2. All tristated when $\overline{\text{Chip Select}} = V_{CC}$ R.G.B. outputs also tristated when displaying picture and not mixed.
3. Picture/$\overline{\text{Text}}$ matched in mix mode only.

VIDEO

GENERAL INSTRUMENT

Video Graphics

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
PERSONAL TERMINAL	The 8900 system is a programable video display system, capable of detailed graphics definition and manipulation.	General Information	9-42
		CP1610	9-22
		AY-3-8900	9-43
		AY-3-8900-1	9-43
		RO-3-9502	9-46
		RO-3-9503	9-49
		RO-3-9600	9-51
		RO-3-9504	9-54
		AY-3-8910	9-56
		AY-3-8912	9-56
		AY-3-8913	9-56
		AY-3-8915	9-57

8900 Programable Game System

FEATURES

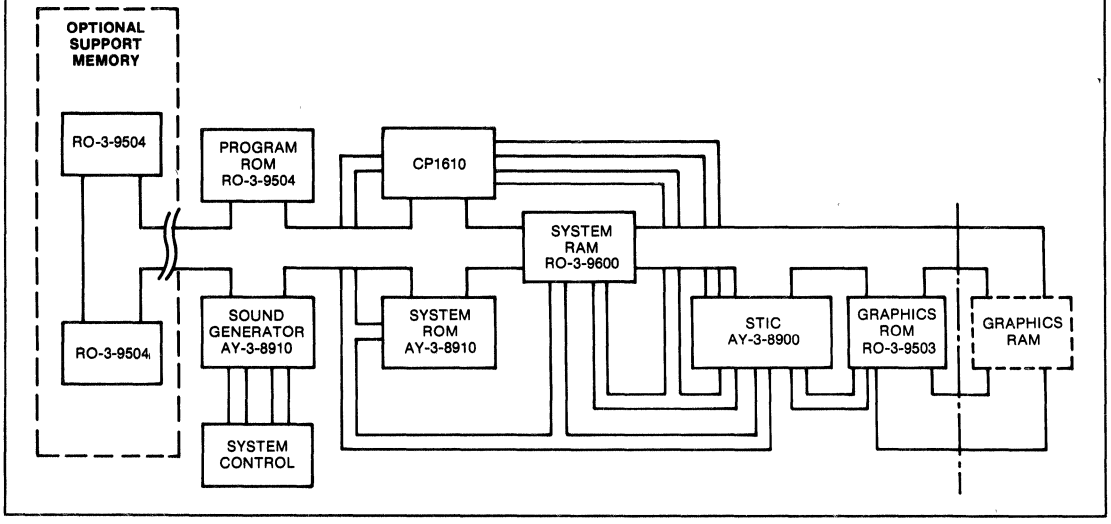
- Infinite game selection
- Lowest cost expandable system
- Uses programable Read Only Memories with 16K and 20K Storage (RO-3-9502, RO-3-9503, and RO-3-9504)
- Eight color selectable, coordinate addressable game objects
- Resident library of 256 complex game objects, including full 64 character alpha numerics
- Shape library extendable by a further 256 objects using graphics RAM.
- Full multicolor background capability
- Sixteen selectable color tones
- Program controllable moving background
- Two hundred and forty independently programable background locations

DESCRIPTION

The 8900 system is based on two processors; one computes the game action against the stored program rules; and the second interprets a condensed memory area and uses this to generate the T.V. raster display. The second processor fetches moving and background pictures from the graphic picture storage and presents the data as a video output.

The set consists of five General Instrument supplied N-Channel circuits. The AY-3-8900 Standard Television Interface Circuit (STIC); the CP1610 GIMINI Microprocessor; an RO-3-9502 20K program ROM; a similar RO-3-9503 graphics picture ROM and an RA-3-9600 RAM. To complete the system the user supplies clocking and modulation circuitry plus any other peripheral control requirements. Other circuits may be optionally added to expand the system capabilities. They are the AY-3-8910 Sound Generator, the RO-3-9504 ROMs, and Standard RAM devices.

8900 SYSTEM DIAGRAM

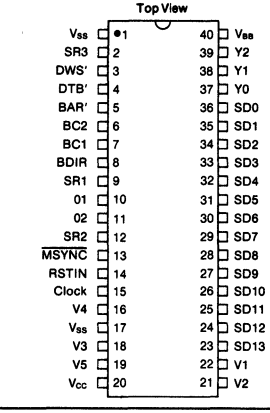


Standard Television Interface Chip

FEATURES

- Outputs include coded signal timings for CCIR or NTSC compatible video signal generation AY-3-8900 for CCIR, AY-3-8900-1 for NTSC
- Operation from a 4.000MHz clock for AY-3-8900 and from a 3.579545MHz clock for AY-3-8900-1
- 8 coordinate addressable foreground objects on a grid of 168H by 104V for AY-3-8900 or 167H by 105V for AY-3-8900-1 of which 159 x 96 are visible positions
- Foreground objects independently programable for half height, y zoom, x zoom and 8 or 16 character lines high
- Selectable background display on a matrix of 20H x 12V using 8 x 8 picture elements
- Capable of accepting data, address and graphics information on common multiplexed bus
- 16 digitally selectable colors

PIN CONFIGURATION
40 LEAD DUAL IN LINE
AY-3-8900/AY-3-8900-1



DESCRIPTION

The AY-3-8900/8900-1 STIC is designed for use within a computer system having an external CPU and an area of ROM and RAM memory. Some of the memory must be dedicated to the support of the graphic character descriptors and patterns.

The display facilities of the circuit are separated into two simultaneously operating modes. The main chip function provides eight coordinate positioned "foreground" objects, which have a number of display options including selection from a choice of sixteen colors. The second mode provides a background display facility, which is composed of a matrix of twelve rows by twenty columns of which 19 are composed of 8 x 8 picture elements and the 20th 7 x 8 picture elements. The "background" mode utilizes a dedicated area of external memory (240 by 14 bit words) to store the character control codes for each display position and both modes require some external memory assigned to the storage of the character patterns. The graphic pattern memory is eight bits wide.

The AY-3-8900/8900-1 operates within the computer system by time sharing a bidirectional 14 bit bus. The demultiplexing and the system synchronization are defined by three sets of control signals.

The main synchronization which operates at the T.V. frame rate uses SR1, SR2 and SR3. The SR1 signal occurs once per frame and it is used to synchronize the CPU algorithms to the intended display sequences. SR1 indicates that STIC time is complete and that the AY-3-8900-1 has switched to the CPU controlled mode. SR2 is issued thirteen or fourteen times per picture frame depending on picture offset. The AY-3-8900/8900-1 takes this signal low to request the first line access for a new row of twenty characters.

The SR3 signal operates in conjunction with SR2 to read the "background" character descriptors out of external memory. The AY-3-8900/8900-1 pulses SR3 positive for each character position. Once the first line has been accessed by the SR2, SR3 combination, the following fifteen lines to complete the 8 x 8 array are fetched by SR3 alone.

The SR3 signal is also issued during the CPU controlled mode in response to BAR, ADAR or DW to enable an external device onto the 14 bit BUS.

The second control bus is used to specify address, read and write sequences for the area of external memory used to store the graphic character "dot" patterns. The three signals on this BUS are BAR', DTB' and DWS'. The BAR" is output by the AY-3-8900/8900-1 when a valid graphics character address is on the 14 bit BUS. The external memory must latch this address for future read or write operations. The DTB' signal indicates that a "read" is requested and the external memory must place the eight bits of character pattern onto the 14 bit BUS. The DWS' signal indicates that a "write" is requested.

The graphics control BUS is used during "STIC" time in the fetch of "foreground" object patterns and "background" object patterns. During the non "STIC" time when in the CPU controlled mode, the graphics control BUS can be used to link the memory area containing the graphics patterns to the main memory area of the external microprocessor.

The third control BUS communicates with the external CPU. This BUS comprises signals BC1, BC2 and BDIR. They are coded to signify address, read and write sequences. The CPU control BUS is only validated if the AY-3-8900/8900-1 is in the CPU controlled mode, otherwise it is ignored.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0° C to +40° C
Storage Temperature ..... −55° C to +150° C
All Input or Output Voltages with Respect to V_{BB} ..... −0.2V to +9.0V
V_{CC}, V_{DD} & V_{SS} with Respect to V_{BB} ..... −0.2V to +9.0V

Standard Conditions (unless otherwise noted)

T_A = 0° C to +40° C, V_{BB} = −3.3V,
V_{CC} = ±4.85V—±5.15V, V_{SS} = 0 0V

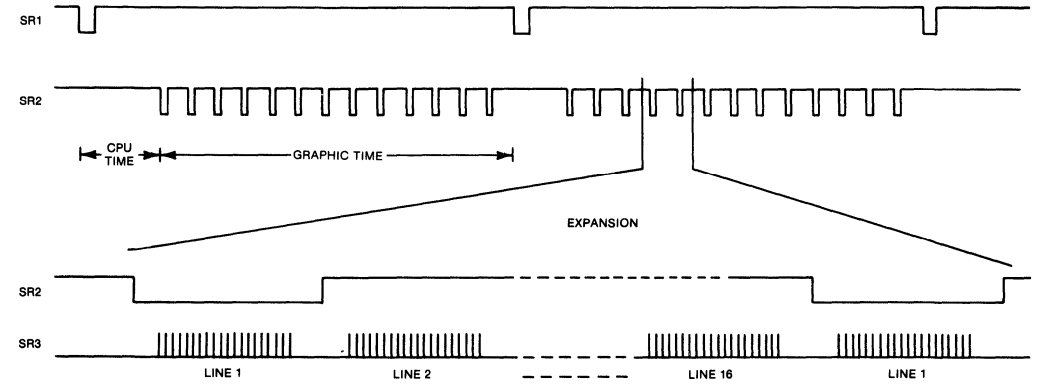
*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Data labeled "typical" is presented for design guidance only and is not guaranteed.

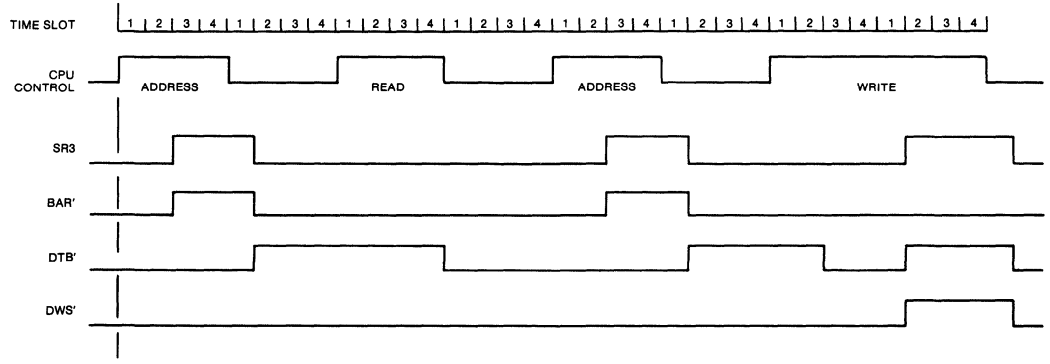
Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Bus Inputs						
Input Logic Low	V_{IL}	0	—	0 7	V	
Input Logic High	V_{IH}	2.4	—	—	V	
Input Current	I_{IL}	—	—	10	μA	$V_{in} = V_{CC}$
Bus Outputs						
Output Logic Low	V_{OL}	0	—	0 5	V	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	V	+100pF
Supply Current						
V_{CC} Supply	I_{CC}	—	—	200	mA	V_{CC} = +5.25V @40° C
AC CHARACTERISTICS						
Clock Input Frequency	f_{cl}	—	—	—	MHz	4.000 for AY-3-8900 3.579545 for AY-3-8900-1 both externally adjusted
Bus Inputs						
Address Set Up	t_{as}	200	—	—	ns	
Address Overlap	t_{ao}	30	—	—	ns	
Write Set Up	t_{ws}	100	—	—	ns	
Write Overlap	t_{wo}	30	—	—	ns	
Bus Outputs						
Turn ON Delay	t_{da}	—	—	140	ns	1 TTL Load
Turn OFF Delay	t_{do}	0	—	—	ns	+100pF

VIDEO

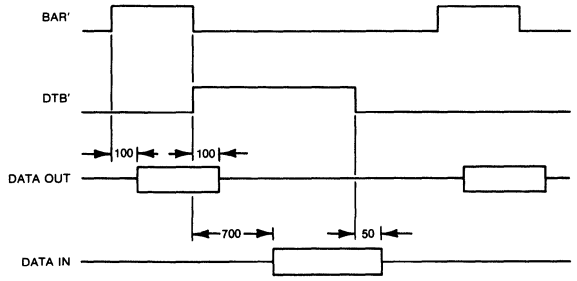
SYSTEM SYNCHRONIZATION TIMING



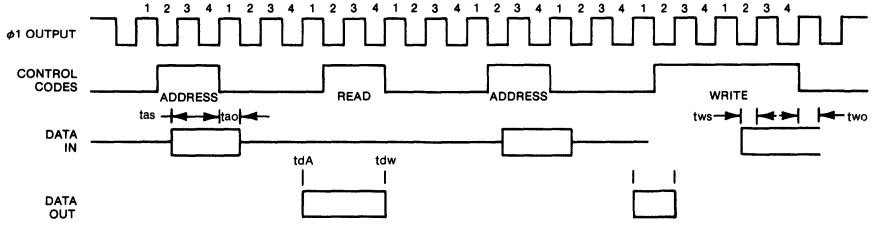
CONTROL SIGNAL OPERATION DURING CPU TIME



OBJECT FETCH TIMING



AY-3-8900-1 CPU CONTROL TIMING



VIDEO

Program ROM

FEATURES

- Mask programable storage providing 2048 x 10 bit words
- 16 bit on-chip address latch
- Control decoder
- Programable memory map circuitry to place 2K ROM page within 65K word memory space located on 2K page boundaries
- Master logic with programable 16 bit vectored start address
- Interrupt logic with programable 16 bit vectored interrupt address
- 16 bit static address outputs for external memory
- Control signals for external memory:
  ENABLE = (DTB + DWS) Address External = R/$\bar{E}$
  WRITE = DWS. Address External = R/$\bar{W}$
- Programable memory map selection for external memory area
- Bus drive capability, 1 TTL load and 100pF plus tri-state

CIRCUIT REQUIREMENTS

The RO-3-9502 operates as the program memory for systems using a CP1610 series microprocessor.

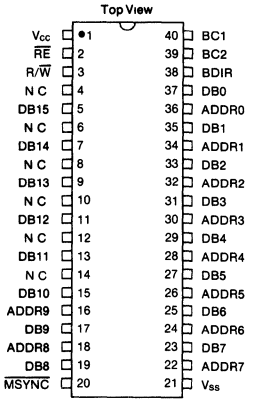
It is configured as 2048 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

OPERATING DESCRIPTION

The RO-3-9502 is initialized by the MSYNC Input and from the positive edge of this signal, it remains in a tri-state output condition, awaiting the IAB response. During the IAB, the 9502 transmits a 16 bit code onto the external bus thus providing the system start address vector. The completion of the MCLR sequence is recorded on chip such that any further IAB Codes output the second interrupt vector. From initialization, the 9502 waits for the first address code. For this address code and all subsequent address sequences, the 9502 reads the 16 bit external bus and latches the value into its address register. The contents of this address register are made available for connection to external memory and are supplied on 16 latched outputs with a drive capability of 1 TTL load and 100pF.

The 9502 contains a programable memory map location for its own 2K page and if a valid address is detected, the particular addressed location will transfer its contents to the chip output buffers. If the control code following the address cycle was a Read, the 9502 will output the 10 bits of addressed data and also drive a logic zero on the top six bits of the bus.

PIN CONFIGURATION
40 LEAD DUAL IN LINE



INPUT CONTROL SIGNALS

BDIR	BC1	BC2	EQUIVALENT SIGNAL	RESPONSE
0	0	0	NACT	NACT
0	0	1	IAB	IAB
0	1	0	ADAR	ADAR
0	1	1	DTB	DTB
1	0	0	BAR	BAR
1	0	1	DWS	—
1	1	0	DW	—
1	1	1	INTAK	—

OPERATION WITH EXTERNAL MEMORY

The 16 bits from the address register are provided as static outputs for connection to external ROM or RAM devices. Two other signals are provided to control the external memory area. An enable signal is provided for any read or write operation, and a write signal, for any move out operation. The two external memory control signals are gated by a min-max memory map comparator. The minimum and maximum values are programable on boundaries within the 65K word memory area. The memory map comparator for external memory is a simple single compare and the operation is such that when a 2K area is chosen, a five bit compare is used and for a 4K area a four bit compare, etc. The effect of this is that 2K pages may start on 2K boundaries, i.e., 0, 2, 4, 6, 8 etc., but 4K pages must be on 4K boundaries, i.e., 0, 4, 8, 12, etc. The same is true for 8K and 16K pages.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with Respect to V_{SS} ..... −0.2V to +9.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

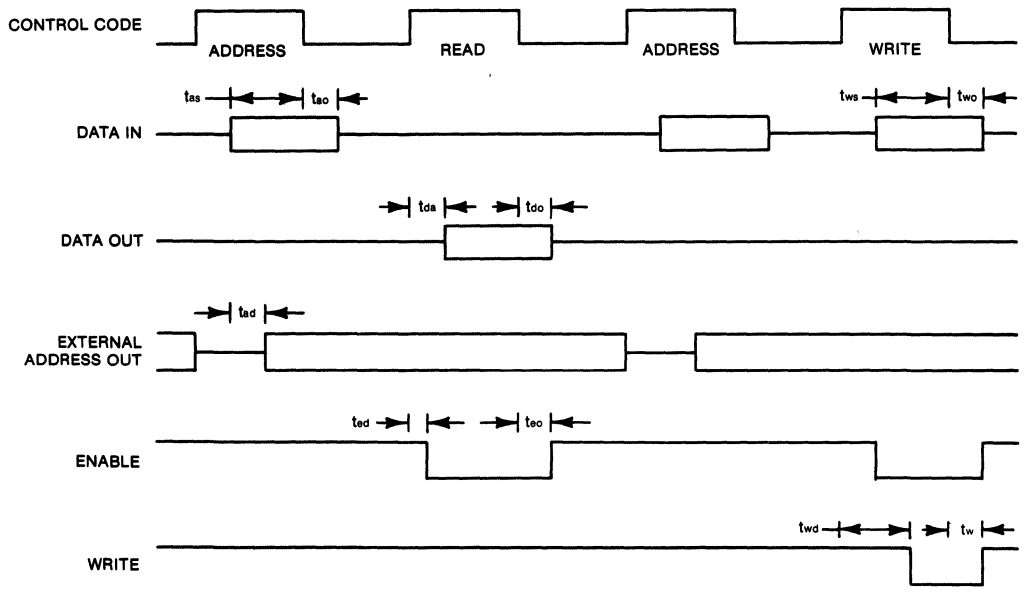
Standard Conditions (unless otherwise noted)

T_A = 0°C to +40°C V_{SS} = 0.0V
V_{CC} = +4.85V − +5.15V

Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Inputs						
Input Logic Low	V_{IL}	0	—	0.7	volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	volts	
Input Leakage	V_{IL}	—	—	10	μA	V_{IN} = V_{CC}
CPU BUS Outputs						
Output Logic Low	V_{OL}	0	—	0.5	volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	volts	+100pF
Address and Enable Outputs						
Output Logic Low	V_{OL}	0	—	0.5	volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	volts	+100pF
Supply Current						
V_{CC} Supply	I_{CC}	—	—	120	mA	V_{CC} = 5.25V @ 40°C
AC CHARACTERISTICS						
Inputs						
Address Set Up	t_{as}	300	—	—	ns	
Address Overlap	t_{ao}	—	50	—	ns	
Write Set Up	t_{ws}	300	—	—	ns	
Write Overlap	t_{wo}	—	50	—	ns	
CPU BUS Outputs						
Turn ON Delay	t_{da}	—	—	300	ns	1 TTL Load
Turn OFF Delay	t_{do}	—	—	200	ns	+100pF
Address and Enable Outputs						
Turn ON Delay	t_{ad},t_{ed}	—	—	200	ns	
Turn OFF Delay	t_{eo}	—	—	150	ns	
Turn ON Delay	t_{wd}	—	—	300	ns	
Turn OFF Delay	t_{wo}	—	—	150	ns	

VIDEO

MEMORY TIMING RO-3-9502



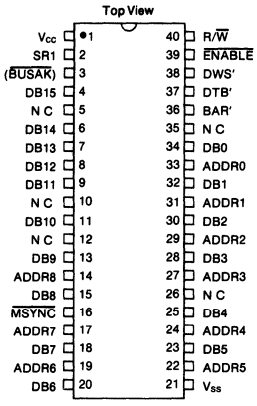
Graphics ROM

FEATURES

- Mask programable storage providing 2048 x 8 bit words
- 16 bit on-chip address latch
- Memory map circuitry to place the 2K ROM page within a 65K memory area
- 8 bit tri-state bus with higher 8 bits driven to zero during read operations
- 11 bit, static address outputs for external memory
- Control signals for external memory:
  $\overline{\text{ENABLE}}$
  R/$\overline{\text{W}}$
- Bus drive capability, 1 TTL load and 100pf plus tri-state

PIN CONFIGURATION

40 LEAD DUAL IN LINE



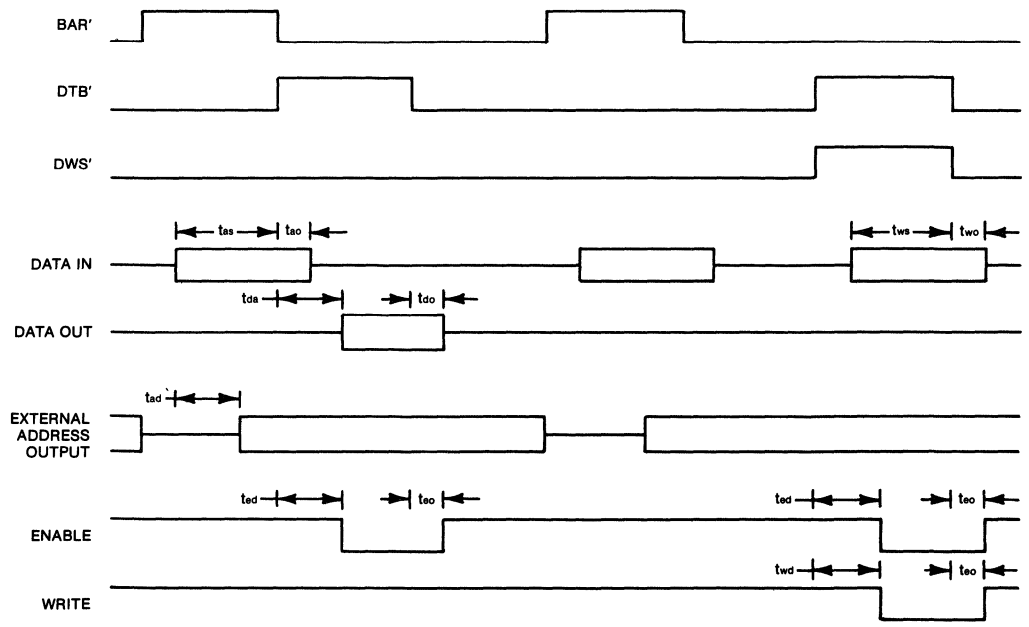
OPERATING DESCRIPTION

The device operates in three memory configurations. These configurations are selected via the input control signals.

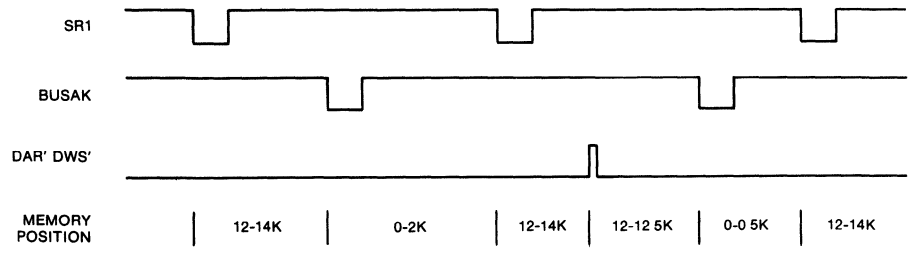
1. When SR1 has been pulsed negative, the memory is located at 12288 to 14335. The external memory is addressed at 14336 to 16383.
2. When $\overline{\text{BUSAK}}$ has been pulsed negative, the memory is located at 0 to 2047. The external memory is addressed at 2048 to 4095.
3. When BAR' and DWS' are pulsed positive, the memory will not respond to address bit 9 and address bit 10, which restricts the memory to 512 locations. The memory is now located from 0 to 511 relative to the current memory origin. The external memory is also addressable from 0 to 511 relative to its current origin. Configuration three may be released by applying a negative pulse on the SR1 input.

VIDEO

MEMORY TIMING



MEMORY POSITION RELATIVE TO CONTROL OPERATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0° C to +40° C
Storage Temperature ..... −55° C to +150° C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with Respect to V_{SS} ..... −0.2V to +9.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

T_A = 0° C to +40° C
V_{CC} = +4.85V − + 5.15V
V_{SS} = 0.0V

VIDEO

Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Bus Inputs						
Input Logic Low	V_{IL}	0	—	0 7	Volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	Volts	
Input Leakage	I_{IL}	—	—	10	μA	$V_{IN} = V_{CC}$
CPU BUS Outputs						
Output Logic Low	V_{OL}	0	—	0 5	Volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	Volts	+100pF
Address and Enable Outputs						
Output Logic Low	V_{OL}	0	—	0 5	Volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	Volts	+100pF
Supply Current						
V_{CC} Current	I_{CC}	—	—	150	mA	V_{CC} = +5.25V @ 40° C
AC CHARACTERISTICS						
Bus Inputs						
Address Set Up	tas	300	—	—	ns	
Address Overlap	tao	—	50	—	ns	
Write Set Up	tws	300	—	—	ns	
Write Overlap	two	—	50	—	ns	
CPU BUS Outputs						
Turn ON Delay	tda	—	—	300	ns	1 TTL Load
Turn OFF Delay	tdo	—	—	200	ns	+100pF
Address and Enable Outputs						
Turn ON Delay	tad,ted,twd	—	—	200	ns	1TTL Load
Turn OFF Delay	teo	—	—	100	ns	+100pF

All delays measured between 2.2 Volts and 0.7 Volts test points

System RAM

FEATURES

- Memory area 352 words of 16 bits
- Address counter and control logic for D M.A operation
- Control decoder for CPU data control signals
- Memory map comparator and control logic for additional memory on 14 bit bus
- Current line buffer — 20 words of 14 bits
- Drive capability on 16 bit and 14 bit bus for 1 TTL load and 100pf

FUNCTIONAL DESCRIPTION

The RA-3-9600 is a dual port interface and 16 bit wide RAM storage area The RA-3-9600 contains twenty 14 bit serial data buffer registers with separate bus control signals

The RA-3-9600 memory is 352 x 16 bit contiguous words from address 512-863 with the graphics descriptors using the first 240 words The graphics use only the lower 14 bits of each word leaving the two most significant bits available for user storage

OPERATION DESCRIPTION

The RA-3-9600 RAM accepts data from the CPU via a 16 bit bi-directional bus which is time multiplexed with address and data A 3 bit control bus from the CPU is used to provide strobe signals for the on-chip address latch and main memory area

The RAM has two operating modes.

Mode 1 — On decoding an interrupt the RAM is enabled into a bus copy mode In this mode the RAM copies the lower fourteen bits of the CPU bus onto the graphics bus The direction of copy is always from the CPU and towards the graphics except during a bus reversal condition The reversal condition is indicated when the CPU requests a read from an external graphics address on the 14 bit bus Under this condition the 9600 will turn its 14 bit bus outputs into tri-state and gate the 14 bit bus through to the 16 bit CPU bus

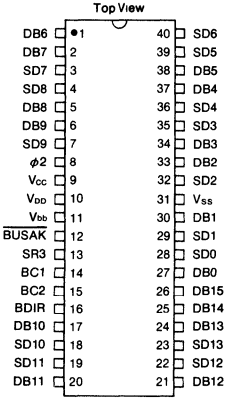
Mode 2 — Is selected when the CPU issues $\overline{\text{BUSAK}}$ command (DMA request) The effect of $\overline{\text{BUSAK}}$ inside the 9600 is to reset the interrupt synchronizing logic and to switch the address decoder from the CPU address register to the graphics address counter This counter, which sequences through the 240 words of graphics data, will have been previously set to zero when the interrupt signal was decoded. When the CPU is in the DMA state, the graphics system will prepare to display a new row of twenty characters and to load the 20 buffer registers within the 9600 For the first cycle of DMA after interrupt the graphics address counter will be at zero and the data at that address is passed to the 14 bit output The action of SR3 will enable the output buffers and drive the 14 bit bus The twenty shift registers are also loaded at this time The negative edge of SR3 tri-states the 14 bit output and increments the graphics address counter The shift registers are also clocked at this time The SR3 input provides twenty positive pulses to the 9600 and loads the shift register buffers while giving the graphics the first row of characters At the end of the first DMA cycle, after the CPU interrupt, the graphics address counter will be at value 20 The 9600 operation for the next fifteen lines will be to clock the 20 shift registers and gate the contents onto the 14 bit bus under control of the SR3 input. When the CPU is running and $\overline{\text{BUSAK}}$ is a logic 1, the graphics address counter is not incremented and it stays at the value 20. At the end of the first row of characters, the complete DMA operation is repeated and the address counter will be left at 40 This sequence occurs for the 12 rows of characters until all 240 have been successfully accessed

The operation of SR3, INCREMENT/TRI-STATE signal, is to step the shift register sequentially through each of the twenty characters If the $\overline{\text{BUSAK}}$ signal is low, i.e., in DMA, it also increments the graphics ADDRESS COUNTER SR3 disables the 14 bit graphics bus during the low period.

At the end of active picture the STIC issues an interrupt request to the CPU The RA-3-9600 tests for the INTAK* response from the CPU and uses this signal as an entry control for a copy mode between the two buses The end of the copy mode is controlled by the first $\overline{\text{BUSAK}}$ negative edge.

*INTAK, equivalent BC1, BC2, BDIR = '1'

PIN CONFIGURATION
40 LEAD DUAL IN LINE



VIDEO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{BB} ..... −0.2V to +18.0V
V_{CC}, V_{DD} and V_{SS} with Respect to V_{BB} ..... −0.2V to +18.0V

Standard Conditions (unless otherwise noted)

T_A = 0°C to +40°C V_{CC} = +4.85V—+5.15V
V_{DD} = +11.6V—+12.4V V_{BB} = −3.3V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
Clock Input Freq. $\phi 2$	—	—	—	—	MHz	1.79545MHz
Input Logic Low	V_{ILC}	0	—	0.7	Volts	
Input Logic High	V_{IHC}	2.4	—	V_{DD}	Volts	
Input Current	I_{ILC}	—	—	10	μA	$V_{in} = V_{CC}$
Bus Inputs and Control Inputs						
Input Logic Low	V_{IL}	0	—	0.7	Volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	Volts	
Input Currents	I_{IL}	—	—	10	μA	$V_{in} = V_{CC}$
Bus Outputs						
Output Logic Low	V_{IL}	0	—	0.5	Volts	1 TTL Load
Output Logic High	V_{OL}	2.4	—	V_{CC}	Volts	+100pF
AC CHARACTERISTICS						
Clock Input					ns	
Rise & Fall Time	t_r, t_f	—	—	50	ns	
CPU Bus Timing						
Address Set Up Time	t_{as}	300	—	—	ns	
Address Hold Time	t_{ao}	—	—	50	ns	
Data Access Time	t_{da}	—	—	500	ns	1 TTL Load
Data Hold Time	t_{do}	—	100	—	ns	+100pF
Write Data Setup	t_{ws}	100	—	—	ns	
Write Data Hold	t_{as}	0	—	—	ns	
Graphics Bus Timing						
Data Access Time	t_{ga}	—	—	150	ns	1 TTL Load
Data Hold Time	t_{go}	—	100	—	ns	+100pF

VIDEO

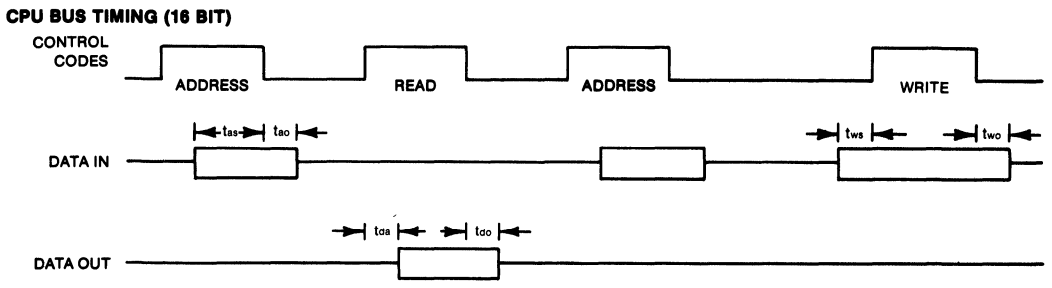


Fig. 1 BUS TIMING

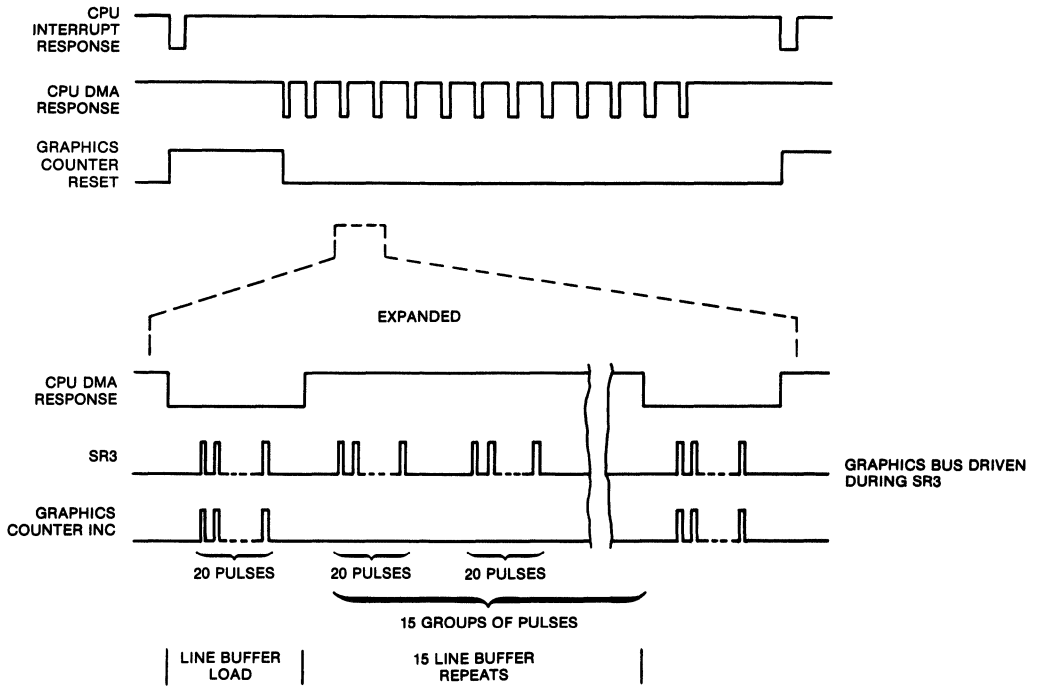


Fig. 2 RAM GRAPHICS OPERATION

Cartridge ROM

FEATURES

- Mask programable storage providing 2048 x 8 bit words
- 16 bit on-chip address latch
- Memory map circuitry to place the 2K ROM page within a 65K Memory area
- 16 bit tri-state bus with higher 6 bits driven to zero during read operations

CIRCUIT REQUIREMENTS

The RO-3-9504 operates as the program memory for systems using a CP1610 microprocessor. It is configured as 2048 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

DESCRIPTION

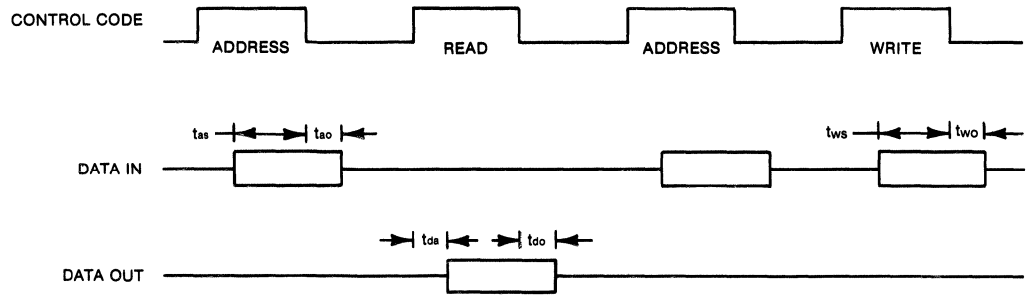
From initialization, the RO-3-9504 waits for the first address code, i.e., BAR. For this address code and all subsequent address sequences, the 9504 reads the 16-bit external bus and latches the value into its address register.

The 9504 contains a programable memory map location for its own 2K page, and if a valid address is detected, the particular address location will transfer its contents to the chip output buffers. If the control code following the address cycle was a READ, the 9504 will output the 10 bits of addressed data and drive a logic zero on the top six bits of the bus:

INPUT CONTROL SIGNALS

BDIR	BC1	BC2	EQUIVALENT SIGNAL	RESPONSE
0	0	0	NACT	NACT
0	0	1	IAB	NACT
0	1	0	ADAR	ADAR
0	1	1	DTB	DTB (READ)
1	0	0	BAR	BAR
1	0	1	DWS	—
1	1	0	DW	—
1	1	1	INTAK	—

MEMORY TIMING RO-3-9504



VIDEO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with Respect to V_{SS} ..... −0.2V to +9.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

T_A = 0°C to +40°C
V_{CC} = +4.85V − + 5.15V
V_{SS} = 0.0V

Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Inputs						
Input Logic Low	V_{IL}	0	—	0.7	volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	volts	
Input Leakage	V_{IL}	—	—	10	μA	$V_{IN} = V_{CC}$
CPU BUS Outputs						
Output Logic Low	V_{OL}	0	—	0.5	volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	volts	+100pf
Supply Current						
V_{CC} Supply	I_{CC}	—	—	120	mA	V_{CC} = 5.25V @ 40°C
AC CHARACTERISTICS						
Inputs						
Address Set Up	t_{as}	300	—	—	ns	
Address Overlap	t_{ao}	—	50	—	ns	
Write Set Up	t_{ws}	300	—	—	ns	
Write Overlap	t_{wo}	—	50	—	ns	
CPU BUS Outputs						
Turn ON Delay	t_{da}	—	—	300	ns	1 TTL Load
Turn OFF Delay	t_{do}	—	—	200	ns	+100pf

Programable Sound Generator

FEATURES

- Full software control of sound generation
- Interfaces to most 8-bit and 16-bit microprocessors
- Three independently programed analog outputs
- Two 8-bit general purpose I/O ports (AY-3-8910)
- One 8-bit general purpose I/O port (AY-3-8912)
- Single +5V Supply

DESCRIPTION

The AY-3-8910/8912/8913 Programable Sound Generator (PSG) is a Large Scale Integrated Circuit which can produce a wide variety of complex sounds under software control. The AY-3-8910/8912/8913 is manufactured in the General Instrument N-Channel Ion Implant Process. Operation requires a single 5V power supply, a TTL compatible clock, and a microprocessor controller such as the General Instrument 16-bit CP1600/1610 or one of the General Instrument PIC1650 series of 8-bit microcomputers.

The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling and FSK modems. The analog sound outputs can each provide 4 bits of logarithmic digital to analog conversion greatly enhancing the dynamic range of the sounds produced

In order to perform sound effects while allowing the processor to continue its other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable channels available in the PSG.

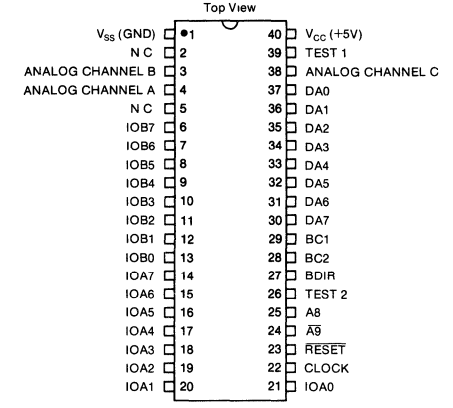
All of the circuit control signals are digital in nature and intended to be provided directly by a microprocessor/microcomputer. This means that one PSG can produce the full range of required sounds with no change in external circuitry Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections.

Since most applications of a microprocessor/PSG system would also require interfacing between the outside world and the microprocessor, this facility has been designed into the PSG. The AY-3-8910 has two general purpose 8-bit I/O ports and is supplied in a 40 lead package; the AY-3-8912 has one port and 28 leads: the AY-3-8913 has no I/O ports and 24 leads.

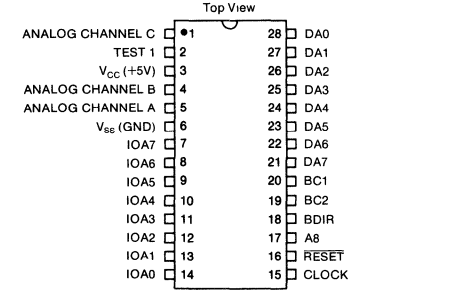
See complete data sheets of AY-3-8910/8912/8913 in Audio Section.

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-3-8910



28 LEAD DUAL IN LINE
AY-3-8912



VIDEO

Color Processor Chip

FEATURES

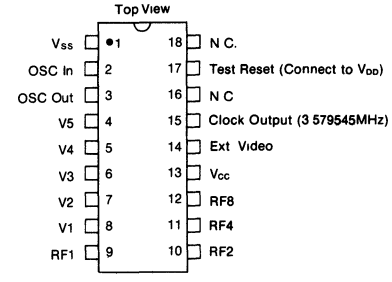
- Operation from 7 15909MHz crystal
- Five-line digital selection for 1 of 16 colors, blanking, sync and color burst
- 3 579545MHz buffered output

DESCRIPTION

The required color to be displayed for each 280ns PIXEL is decoded on a four line binary coded input. This selects one of sixteen possible colors. An external resistor network completes the D to A function as shown in the schematic of Fig. 1. The waveform plus table illustrates the use of the five inputs to produce composite sync, color burst, line blanking, frame blanking and video.

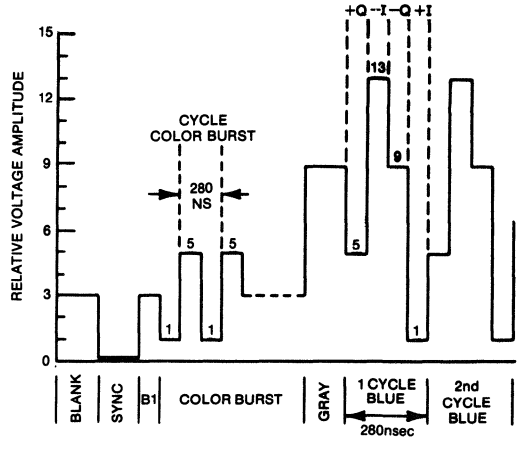
The external video input pin provides the ability to superimpose white high resolution (140ns wide) video information over the picture (color image).

PIN CONFIGURATION
18 LEAD DUAL IN LINE



INPUT CODE ASSIGNMENT					TIME SLOT RELATIVE VOLTAGE AMPLITUDES				COLOR OUTPUT DESCRIPTION	
V5	V4	V3	V2	V1	+Q	−I	−Q	+I		
0	0	0	0	0	3	3	3	3	Black	
0	0	0	0	1	5	13	9	1	Blue	Group A
0	0	0	1	0	8	0	4	12	Red	Group A
0	0	0	1	1	4	4	12	12	Tan	Group A
0	0	1	0	0	3	8	11	6	Grass Green	Group A
0	0	1	0	1	3	11	13	5	Green	Group A
0	0	1	1	0	9	11	15	13	Yellow	Group A
0	0	1	1	1	13	13	13	13	White	Group A
0	1	0	0	0	9	9	9	9	Gray	
0	1	0	0	1	8	13	12	7	Cyan	Group B
0	1	0	1	0	9	4	9	14	Orange	Group B
0	1	0	1	1	4	4	8	8	Brown	Group B
0	1	1	0	0	13	5	3	11	Magenta	Group B
0	1	1	0	1	12	12	6	6	Light Blue	Group B
0	1	1	1	0	5	9	13	9	Yellow-Green	Group B
0	1	1	1	1	10	5	2	7	Purple	Group B
1	X	X	0	0	3	3	3	3	Blanking	
1	X	X	1	0	1	1	5	5	Color Burst	
1	X	X	0	1	0	0	0	0	Sync	
1	1	1	1	1	0	15	0	15	Test	

X = Don't Care



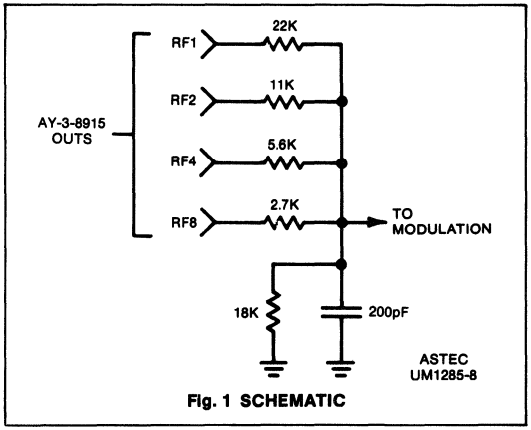


Fig. 1 SCHEMATIC

VIDEO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with Respect to V_{SS} ..... −0.2V to +9.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

T_A = 0°C to +40°C
V_{CC} = +4.85V − + 5.15V
V_{SS} = 0.0V

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Oscillator Freq. In.	—	—	—	—	MHz	7.15909MHz crystal Trimmed by external capacitor
3.579545MHz Clock Output						
Output Logic Low	V_{OL}	0	—	0.5	volts	
Output Logic High	V_{OH}	2.4	—	V_{CC}	volts	
Logic Inputs V1, V2, V3, V4, V5, EXT. VIDEO						
Input Logic Low	V_{IL}	0	—	0.7	volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	volts	
Outputs RF1, RF2, RF4, RF8						
Output ON	I	5	—	—	mA	V_{out} = +0.5V
Output OFF	I	—	—	10	μA	V_{out} = +2.4V
Supply Current						
V_{DD}	I_{CC}	—	—	80	mA	V_{CC} = 5.25V @ 40°C

VIDEO

Video Games

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
BALL & PADDLE	Six selectable games for one or two players, with vertical paddle motion.	AY-3-8500	9-60
		AY-3-8500-1	9-60
8600 SERIES	The 8600 series games consist of a set of single chip TV game integrated circuits.	General Information	9-63
ROADRACE	One or two player games where racing skill in "traffic" generates the highest score.	AY-3-8603	9-64
WARFARE	One or two player games featuring subs, destroyers, cargo ships, and spaceships.	AY-3-8605	9-65
WIPEOUT	One or two player games where players "wipe out" objects by controlling a ball in the play area.	AY-3-8606	9-66
SHOOTING GALLERY	Twelve games for one or two players using external photocell rifles for shooting.	AY-3-8607	9-68
SUPERSPORT	Ten selectable games for one or two players, with vertical and horizontal paddle motion.	AY-3-8610	9-70
MOTOR CYCLE	One player cycle game with variable skill selection.	AY-3-8765	9-72

Ball & Paddle

FEATURES

- 6 Selectable Games—Tennis, soccer, squash, practice and two rifle shooting games
- 625 Line (AY-3-8500) and 525 Line (AY-3-8500-1) versions
- Automatic Scoring
- Score display on T.V. Screen, 0 to 15
- Selectable Bat Size
- Selectable Rebound Angles
- Selectable Ball Speed
- Automatic or Manual Ball Service
- Action Sounds
- Shooting Forwards in Soccer Game
- Visually defined area for all Ball Games.

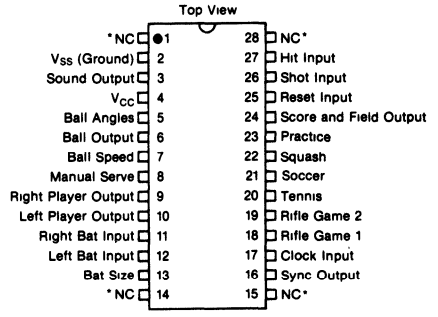
DESCRIPTION

The AY-3-8500 and AY-3-8500-1 circuits have been designed to provide a TV games function which gives active entertainment using a standard domestic television receiver.

The circuit is intended to be battery powered and a minimum number of external components are required to complete the system.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



*Do not use as tie point.

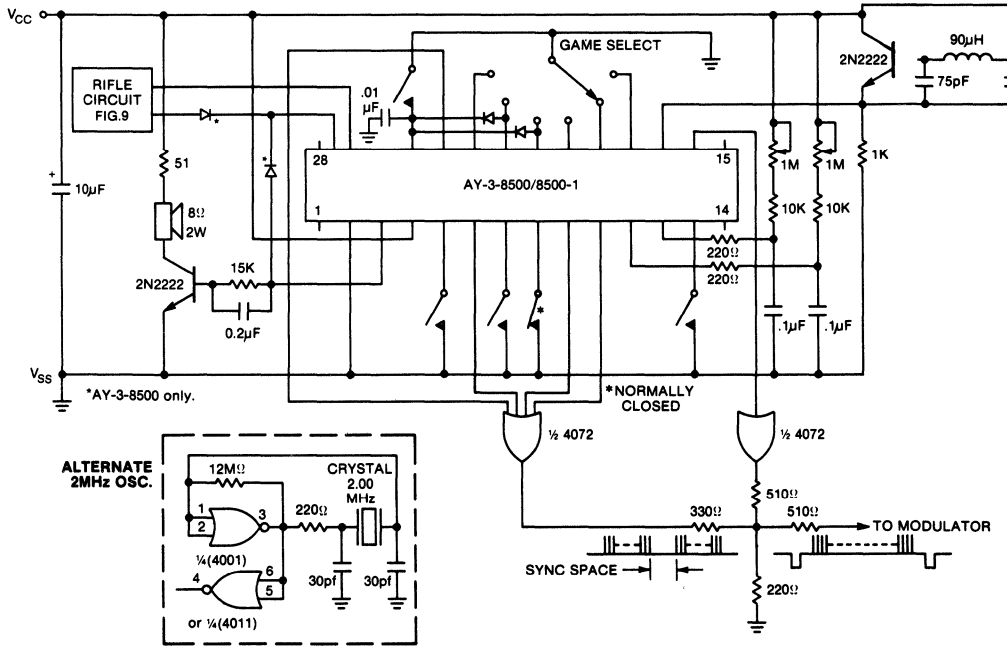


Fig. 1 BLACK AND WHITE IMPLEMENTATION

PIN FUNCTIONS (Pin numbers in parentheses)

Vss (2)
Negative supply input, nominally 0V(GND).

Sound Output (3)
The hit (32ms pulse/976Hz tone), boundary reflection (32ms pulse/488Hz tone) and score (32ms pulse/1.95KHz tone) sounds are output on this pin.

Vcc (4)
Positive supply input.

Ball Angles (5)
This input is left open circuit (Logic '1') to select two rebound angles and connected to Vss (Logic '0') to select four rebound angles. When two angles are selected they are ± 20°, when four are selected they are ±20° and ±40°.

Ball Output (6)
The ball video signal is output on this pin.

Ball Speed (7)
When this input is left open-circuit, low speed is selected (1.3 seconds for ball to traverse the screen). When connected to Vss (Logic '0'), the high speed option is selected (0.65 seconds for ball to traverse the screen).

Manual Serve (8)
This input is connected to V_{SS} (Logic '0') for automatic serving. When left open circuit (Logic '1') the game stops after each score. The serve is indicated by momentarily connecting this input to V_{SS}.

Right Player Output/Left Player Output (9,10)
The video signals for the right and left players are output on separate pins.

Right Bat Input/Left Bat Input (11,12)
An R-C network connected to each of these inputs controls the vertical position of the bats. Use a 10K resistor in series with each pot.

Bat Size (13)
This input is left open circuit (Logic '1') to select large bats and connected to V_{SS} (Logic '0') to select small bats. For a 19" T.V. screen, large bats are 1.9" and small bats are 0.95" high.

Sync Output (16)
The T.V. vertical and horizontal sync signals are output on this pin. See Fig. 2

Clock Input (17)
The 2MHz master timing clock is input to this pin. The exact frequency is 2.012160 ± 1%.

Rifle Game 1, Rifle Game 2, Tennis, Soccer, Squash, Practice (18 thru 23)
These inputs are normally left open circuit (Logic '1') and are connected to V_{SS} (Logic '0') to select the desired game.

Score and Field Output (24)
The score and field video signal is output on this pin.

Reset (25)
This input is connected momentarily to Vss (Logic '0') to reset the score counters and start a new game. Normally left open circuit.

Shot Input (26)
This input is driven by a positive pulse output of a monostable to indicate a "shot".

Hit Input (27)
This input is driven by a positive pulse output of a monostable which is triggered by the shot input if the target is on the sights of the rifle.

NOTE: The "Shot" and "Hit" inputs have on-chip pull-down resistors to Vss. All other inputs (except the "Bat" inputs) have on-chip pull-up resistors to Vcc.

VIDEO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} Pin ..... −0.3 to +12V
Storage Temperature Range ..... −20° C to +70° C
Ambient Operating Temperature Range ..... 0° C to +40° C

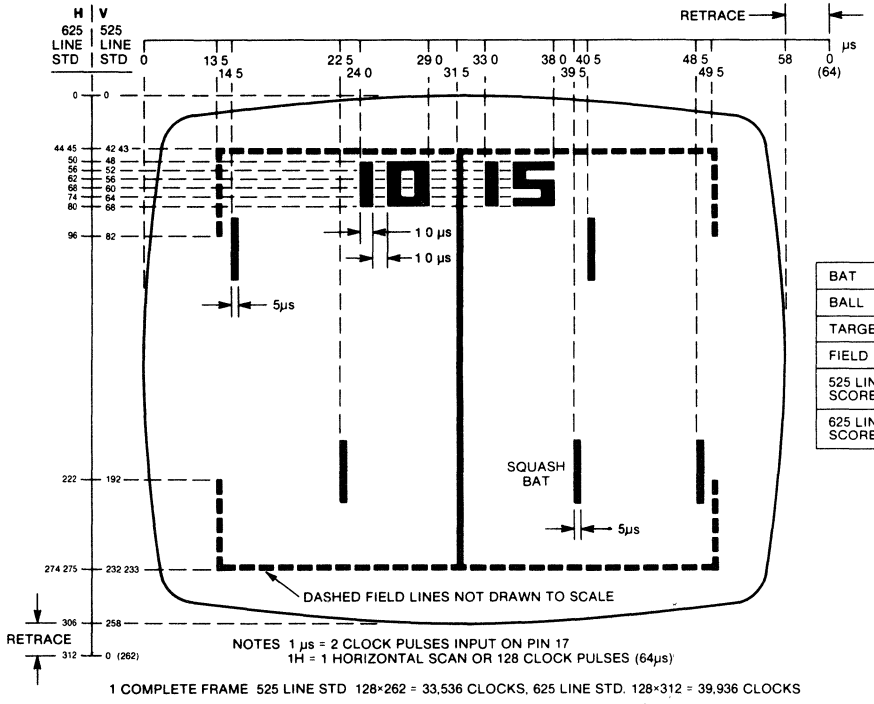
Standard Conditions (unless otherwise noted)

V_{CC} = +6 to +7V
V_{SS} = 0V
Operating Temperature (T_A) = 0° C to +40° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied — operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics at 25° C and Vcc = +6 Volts	Min	Typ	Max	Units	Conditions
Clock Input					Maximum clock source impedance
Frequency	1.99	2.01	2.03	MHz	of 1K to V_{CC} or V_{SS}.
Logic '0'	0	—	0.5	V	
Logic '1'	V_{CC}-2	—	V_{CC}	V	
Pulse Width — Pos.	—	200	—	ns	
Pulse Width — Neg.	—	300	—	ns	
Capacitance	—	10	—	pF	V_{IN} = 0V, F = 1MHz
Leakage	—	100	—	μA	
Control Inputs					Max contact resistance of 1K to V_{SS}
Logic '0'	0	—	0.5	V	
Logic '1'	V_{CC}-2	—	V_{CC}	V	
Input Impedance	—	1	—	MΩ	Pull up to V_{CC}
Rifle Input	—	1	—	MΩ	Pull down to V_{SS}
Outputs					
Logic '0'	—	—	1	V	Iout = 0.5mA
Logic '1'	V_{CC}-2	—	—	V	Iout = 0.1mA
Power Supply Current	—	40	60	mA	at V_{CC} = +7V



	H	V
BAT	0 5μs	14/28 lines
BALL	1 0μs	5 lines
TARGET	2 5μs	14 lines
FIELD	0 5μs	2 lines
525 LINE SCORE	5 0μs	20 lines
625 LINE SCORE	5 0μs	30 lines

Fig. 2 LOCATION OF DATA OUTPUT PULSES

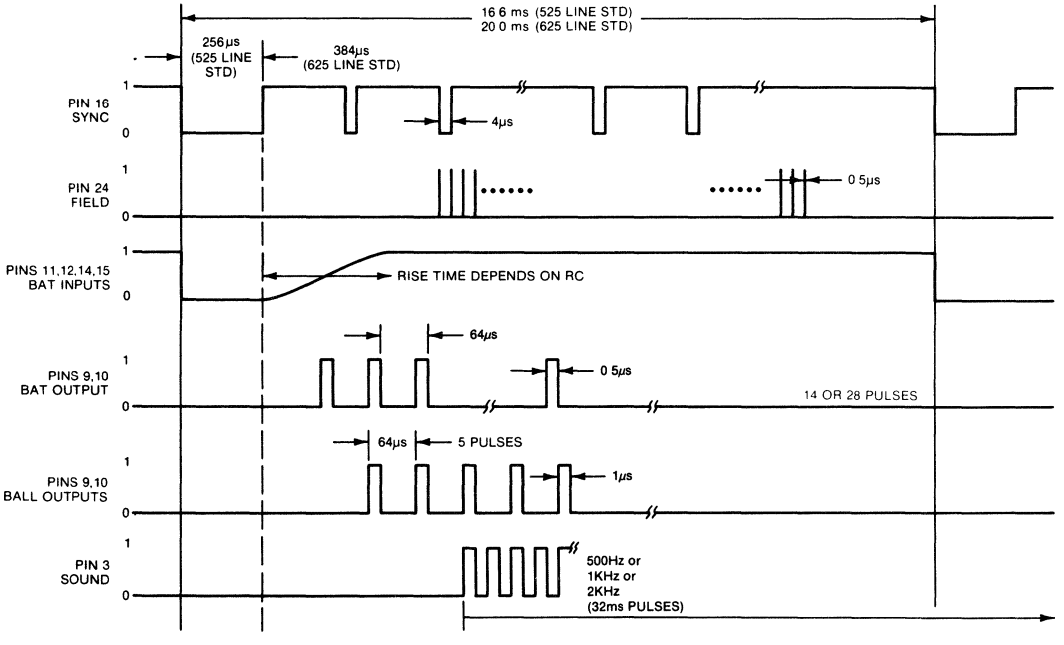


Fig. 3 TIMING DIAGRAM

VIDEO

TV Games

The Gimini 8600 Series games consist of a set of single chip TV game integrated circuits. This series consists of AY-3-8603 Roadrace, AY-3-8605 Warfare, AY-3-8606 Wipeout, AY-3-8607 Rifle, AY3-8610 Supersport, and AY-3-8765 Motorcycle chips. Circuit descriptions giving detailed information on each game chip are in the following pages of this section.

The TV games may be configured as dedicated games when packaged with a color processor and peripheral circuitry. When packaged as individual cartridges, able to be connected to a main console containing the color processor and peripheral circuitry, the game becomes programable by its user.

The following block diagram shows a programable game configuration which can be combined to provide a dedicated game if desired.

DESCRIPTION

The console consists of a resident game/color processor, an R.F. video modulator, a calculator type keyboard for game selection, a set of three skill select switches, and a game reset switch. Attached to the console are the player controllers which can consist of joysticks or a variety of controls suited to the game.

The console need never be opened once in operation; all changes to the system are plugged in externally. The cartridges and controls are the only items that are altered to give the 8600 system new game characteristics.

The block diagram shows the basic system with its expandability.

SECTION A

There are three switches that will allow skill selections. These skills will be determined by the specific game cartridge and will control speeds, sizes and shapes of objects in any particular game cartridge. A fourth switch acts as game reset.

SECTION B

The game selections will be made by a maximum of ten momentary switches similar to the calculator keyboard. Again the number of games is determined by the cartridge.

SECTION C

The controls are always in pairs to allow for two players. Depending on the game cartridge, a variety of controls may be used.

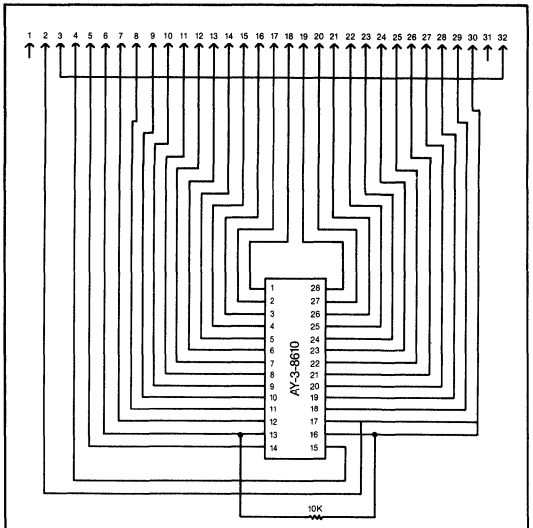


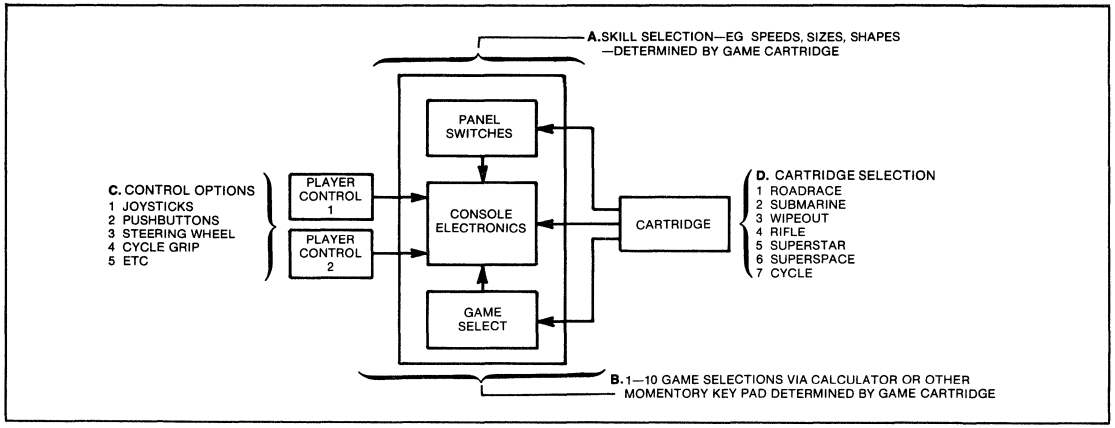
Fig. 1 AY-3-8610 CARTRIDGE

Basically most games can be controlled by resistance joysticks. If controls are remote, the connectors used should be a minimum of six pins each to allow for game flexibility.

SECTION D

The cartridges will all be compatible with the console and a variety will be offered. Each cartridge will give the game a completely new objective. The cartridge should have a minimum of 34 pins to allow for special connections such as sound effects, etc., and remain compatible with the system.

Fig. 1 illustrates as an example the straightforward layout for the AY-3-8610 Supersport game cartridge.



Roadrace

FEATURES

- Two game selections—one and two player games
- T.V. raster generator
- All timing signals for color or black and white application
- Direct compatibility with Economy "8600" game console
- Automatic on-screen scoring
- Score color-keyed for each player
- Skill selection for difficult or easy driving conditions
- Realistic motor and crash sound generation with a minimum of external components

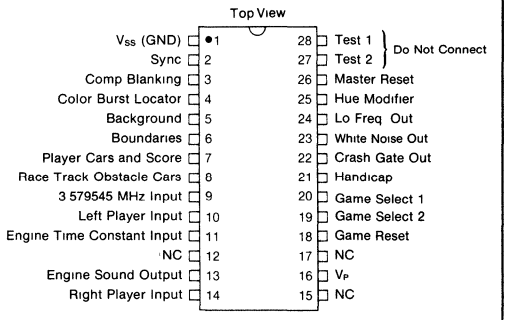
DESCRIPTION

The AY-3-8603 game circuit has been designed to provide a realistic roadrace game using a standard television receiver. The circuit is intended for color or black and white usage with a 625 (AY-3-8603) line receiver. The circuit is designed to be either a stand-alone game or an add-on for the Gimini Economy "8600" game series

OPERATION

The AY-3-8603 utilizes two potentiometers to produce control voltage for the horizontal positioning of the race cars Each player controls his own car. The circuit displays a score for each driver, processes the game logic and produces composite sync, color burst location and blanking signals for a 625 line T.V. receiver. Sound outputs are also included to produce simulated engine and crash sounds with a minimum of external components.

PIN CONFIGURATION
28 LEAD DUAL IN LINE



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} ..... −0.3 to +12V
Storage Temperature Range ..... −20° C to +70° C
Ambient Operating Temperature Range ..... 0° C to +40° C
Operating Voltage Supply Range ..... +7 5 to +9V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied — operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise noted)

Parameter values at $T_A = 25°C$

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristic	Min	Typ	Max	Units	Conditions
Clock Input					
Frequency	—	3.579545	—	MHz	
Logic '0'	0	—	0.5	V	45-55% duty cycle
Logic '1'	V_p-2	—	V_p	V	
Leakage	—	—	—	—	
Control Input					
Logic '0'	0	—	0 2	V	Max. contact resistance of 1K to V_{SS}
Logic '1'	V_p-2	—	V_p	V	
Input Impedance	—	100	—	KΩ	Pull up to VP
Output pins	—	—	1	V	I_{out} = 2mA
On Off	—	1000	—	μA	$V_{out} = V_p$
Power Supply Current	—	—	60	mA	at V_p = 7 5V

Warfare

FEATURES

- Outputs include CCIR (AY-3-8605) compatible composite sync, color burst location and blanking
- Operation from a 3.579545 clock
- One or two player game
- Digital on-screen scoring
- Sound generation for engine, sonar, firing and explosions
- Outputs and power requirements compatible with the Gimini Economy "8600" game series

DESCRIPTION

The AY-3-8605 game circuit has been designed to provide realistic sea and space battle games using a standard television receiver. The circuit is intended for use with a 625 (AY-3-8605) line receiver.

OPERATION

The AY-3-8605 utilizes two potentiometers (one for each player) or one axis of two joysticks to produce control voltages for internal Schmitt triggers. These position the submarine, destroyer, and spaceships, via rate controllers in the horizontal axis only The circuit displays an on-screen score for each player, processes the game logic and produces a composite sync, color burst location and blanking signals for a 625 line T.V. receiver. Sound outputs are also included to produce simulated engine, sonar, firing, and explosion sounds with a minimum of external components.

The outputs are designed for compatibility within the Gimini Economy Game series. Game selection is made via a 2 strobe/3 select switch matrix with momentary contacts. Two momentary switches that ground the "fire" input pins are used to activate the torpedoes, depth charges, and missiles.

SOUND OUTPUTS

Space background noise—7 Bit Polynomial Counter clocked at 2kHz rate

Torpedo or Depth Charge fired—1kHz signal for 2 frames then off for 4 frames.

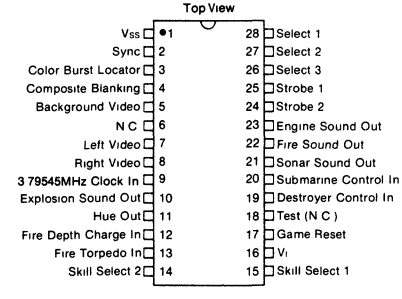
Explosion— ∿ 8kHz signal for∿ 3½ seconds.

Destroyer engine—Fast sound is a 240Hz clock into a 4 bit poly counter—Slow sound is a 120Hz clock rate.

Sonar for Submarine—Decaying 480Hz signal for ∿ 2.9 seconds followed by a 2kHz signal burst for∿ 200ms. This sound repeats every 3½ seconds.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



MOVEMENT

The cargo ship will traverse the screen in 16 seconds.

The destroyer ship will traverse the screen in 5.3 seconds.

The submarine moves across the screen in 8 seconds.

The torpedo rises at a rate of 1 line per frame. To move the 100 lines to hit the destroyer will take 1.67 seconds.

The depth charge falls at a rate of 1 line every 2 frames. To hit the submarine will take 3.34 seconds.

Wipeout

FEATURES

- Outputs include CCIR for AY-3-8606
- Operation from a 3.579545MHz clock
- One or two player games
- Digital on-screen scoring
- Sound generation for tones to indicate hits of ball to bat, ball to objects, and ball to border
- Outputs and power requirements compatible with Gimini Economy "8600" Game Series to allow plug-in operation

DESCRIPTION

The AY-3-8606 game circuit has been designed to provide an active paddle/squares game using a standard television receiver. The circuit is intended for use with a 625 (AY-3-8606) line receiver.

OPERATION

The AY-3-8606 utilizes two potentiometers (one for each player) one axis only of each joystick to produce control voltages for internal Schmitt triggers. These position the player's bats in the vertical axis only to allow play of the game. The circuit displays an on-screen score color coded to each player, processes the game logic and produces a composite sync, color burst location and blanking signals for a standard line TV receiver. Sound output is also included to produce tonal sounds for ball hits to bats, ball hits to borders and ball hits on objects with a minimum number of external components.

The outputs are designed for compatibility within the Gemini Economy "8600" Game Series. Game selection is made via a 4 strobe, 3 select switch matrix with either fixed or momentary contact closures.

Two momentary switches that ground the input serve control pins are used to start the ball into motion after reset or when a reserve is necessary according to game rules. Three skill selection switches are used to determine game difficulty.

GAME OPERATION

Select 1 Strobe 1 (Game #1)

A single-player game in which the player manipulates the paddle in the vertical axis after manually serving the ball The objective is to wipe out as many boxes as possible in the seven serves that are allowed during a single game.

Select 1 Strobe 2 (Game #2)

A single-player game in which the player manipulates two paddles at each end of the playing area in the vertical axis after manually serving the ball. The objective is to wipe out as many boxes as possible in the seven serves that are allowed during a single game

Select 1 Strobe 3 (Game #3)

A two-player game in which each player manipulates his paddle at the ends of the playing area in the vertical axis The ball is served by the last player to score after game is in play. The objective is to wipe out all boxes in the playing area. The winner ends with the highest score

Select 1 Strobe 4 (Game #4)

A two-player game in which each player manipulates his paddle at the ends of the playing area in the vertical axis. The ball is served by the last player to score after the game is in play. The objective is to wipe out all the boxes in the playing area The winner ends with the highest score The ball will rebound off the center barrier.

Select 2 Strobe 1 (Game #5)

A single-player game in which the player manipulates two different colored paddles at each end of the playing area in the vertical axis after manually serving the ball The objective is for the player to wipe out as many correct colored objects depending on which color paddle hits the ball into the playing area as possible The game ends when all of one color objects are wiped out

Select 2 Strobe 2 (Game #6)

A two-player game in which each player manipulates his paddle at the ends of the playing area in the vertical axis The ball is served by the last player to score after the game is in play. The objective is to wipe out as many boxes color coordinated with the player's paddle The first color completely wiped out wins

Select 2 Strobe 3 (Game #7)

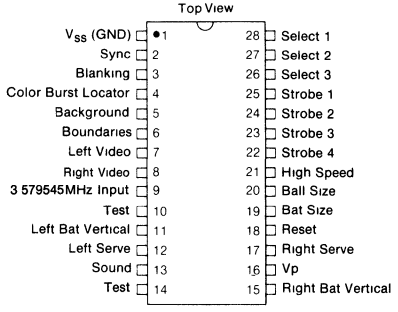
A two-player game in which each player manipulates his paddle at the ends of the playing area in the vertical axis The ball is served by the last player to score after the game is in play The objective is to wipe out as many boxes color coordinated with the player's paddle The first color completely wiped out wins

Select 2 Strobe 4 (Game #8)

A single-player game in which the player manipulates the paddle in the vertical axis after manually serving the ball The object is to wipe out as many color coordinated boxes with the player's paddle as possible in the seven serves that are allowed during a single

PIN CONFIGURATION

28 LEAD DUAL IN LINE.



VIDEO

game. The ball alternates colors on each rebound, thus it can only hit one color square to wipe out and is transparent to the other color at any one time. After a hit and rebound, the ball can wipe out the opposite color square.

Select 3 Strobe 1 (Game #9)

A single-player game in which the player manipulates the paddle in the vertical axis after manually serving the ball. The objective is to break through the end wall and score on as many blocks as possible. The game ends after either seven serves or the first breakthrough.

Select 3 Strobe 2 (Game #10)

A two-player game in which each player manipulates his paddle in the center of the playing area in the vertical axis. The ball is kept in motion by each player trying to protect the wall behind his paddle. If a player misses a hit with the paddle, the ball will hit the wall and one block will disappear and the score will increment for the opposite player. The objective of this game is to knock out as many blocks to get a high score before breaking through the wall. The first player to hit the ball through an open section of a wall ends the game.

NOTE: If the ball hits the left wall at a point where three blocks connect from the lower edge, the block in the same direction as the trajectory will disappear.

SKILL SELECTION

The games mentioned can be made more difficult by selecting one or more of the following skills:

1. Bat Size (left player only)
2. Ball Size (in large ball size, bat must hit center of ball)
3. Ball Speed

A ground on any of these function pins shall:

1. Halve the bat size
2. Halve the ball size
3. Double the ball speed

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_n Pin ..... −0.2V to 12V
Storage Temperature Range ..... −20° C to +70° C

Standard Conditions (unless otherwise noted)

V_p = +7.5 to +9.0 volts
Ambient Operating Temperature Range 0° C to +40° C
Characteristics at +25° C and V_p = 7.5V

* Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied — operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics	Min	Max	Units	Conditions
CLOCK INPUT				
Frequency	—	—	MHz	
Logic '0'	0	0.5	V	45-55% duty cycle
Logic '1'	V_p-2	V_p	V	
Leakage	—	100	μA	
CONTROL INPUT				
Logic '0'	0	0.5	V	May contact resistance of 1K to V_n
Logic "1"	V_p-2	V_p	V	
Input Impedance	—	—	KΩ	
OUTPUT PINS 2-8, 13				
ON	—	1	V	I_{out} = 2mA
OFF	—	100	μA	V_{out} = V_p at 7.5V
OUTPUT PINS 22-25				
ON	—	1.0	V	I_{out} = .5mA
OFF	—	100 μA	μA	V_{out} = V_p (open drain)
Power Supply Current	—	75	mA	

Shooting Gallery

FEATURES

- Outputs include CCIR (AY-3-8607) compatible composite sync, color burst location and blanking
- Operation from a 3.579545MHz clock
- One or two player game
- Digital on-screen scoring
- Sound generation for flight, fall, hit and impact
- Outputs and power requirements compatible with Gimini Economy "8600" Game Series to allow plug-in operation

DESCRIPTION

The AY-3-8607 game circuit has been designed to provide an active series of target games using a standard television receiver. The circuit is intended for use with a 625 (AY-3-8607) line receiver.

OPERATION

The AY-3-8607 utilizes an external photo cell mounted in a gun or rifle for recording hits. The logic requires the gun to input a shot pulse when the trigger is pulled and if the photo cell in the gun records the hit (if on target) a pulse will be transmitted to the chip. (No pulse if off target).

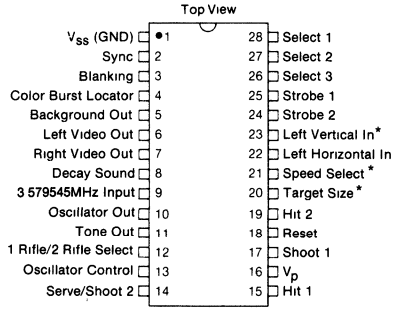
Some of the two-player games require two guns.

With the two-player game where one player controls the target and the other shoots, the joystick in the console will be used for target control.

Skill select switches on the console are used for (1) target size large or small (2) target speed, fast or slow. In two-player/two-rifle games, the left joystick is used for additional handicapping/skill selection.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



*Pin functions are for one-player games.
For two-player games, the functions of pins 20 thru 23 are:

20—Player 1 Target Size
21—Player 1 Speed Select
22—Player 2 Target Size
23—Player 2 Speed Select

VIDEO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_n Pin ..... −0.3 to +12.0V
Storage Temperature ..... −20° C to +70° C
Ambient Operating Temperature Range ..... 0° C to 40° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied — operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Standard Conditions (unless otherwise noted)

V_{dd} = 7 5 to 9.0 Volts
V_{SS} = 0 Volts
All characteristics specified at 25° C and V_{dd} = 7.5 volts

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics	Min	Max	Units	Conditions
Clock Input	—	—	—	Crystal controlled @ 3 579545MHz with 45% to 55% positive duty cycle.
	0	0.5	V	Logic "0" level
	V_{dd}-2	V_{dd}	V	Logic "1" level
	—	100	μA	Leakage, $V_{in} = V_{dd}$
Outputs				
Pins 2, 3, 4, 5, 6, 7	—	1 0	V	Logic "0" level $I_{out} = -2mA$
	—	100μA	μA	Off volt = V_{dd} = 7.5 Volts
Output Pin #8	—	1	V	$I_{out} = -0.5mA$
	V_{dd}-2	—	V	$I_{out} = +0.5mA$
Output Pins 11, 13	—	1	V	$I_{out} = -0.2mA$
	V_{dd}-2	—	V	$I_{out} = +0$ 2mA
Output Pin #22, 23	—	1	V	$I_{out} = -0$ 5mA
	—	35	μA	Volt = V_{dd} = 7 5 Volts
Inputs				
Pin #26, 27, 28	150	375	K	V_{dd} = 7 5 Volts
Pin #12, 14, 17, 18, 20	75	150	K	V_{dd} = 7 5 Volts
Power supply current I_{dd}	—	65	mA	V_{dd} = 7 5 Volts

VIDEO

Supersport

FEATURES

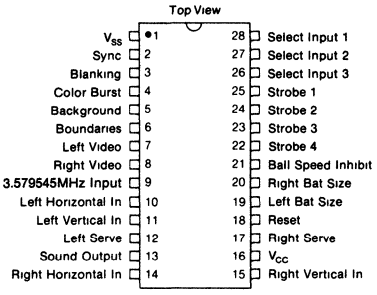
- Ten selectable games — tennis, hockey, soccer, squash, practice, gridball, basketball, basketball practice, one and two player target
- 625 Line (AY-3-8610) versions
- T.V. raster generator
- Two axis player motion
- Automatic on-screen scoring, 0-15
- Automatic ball speed-up after 7 hits or may be disabled by ball speed inhibit input
- Realistic ball service and scoring
- Score color keyed to player
- Independent player selectable bat size for handicapping
- Fast ball speed inhibit
- Five segment bats giving high, low, and horizontal ball angles
- Sound outputs for hit, rebound and score
- Shooting forwards in hockey and soccer

DESCRIPTION

The AY-3-8610 circuit has been designed to provide a TV 'game' function which gives active entertainment using a standard color or black and white domestic television receiver.

The circuit is intended to be battery powered and a minimum number of external components are required to complete the system.

PIN CONFIGURATION
28 LEAD DUAL IN LINE



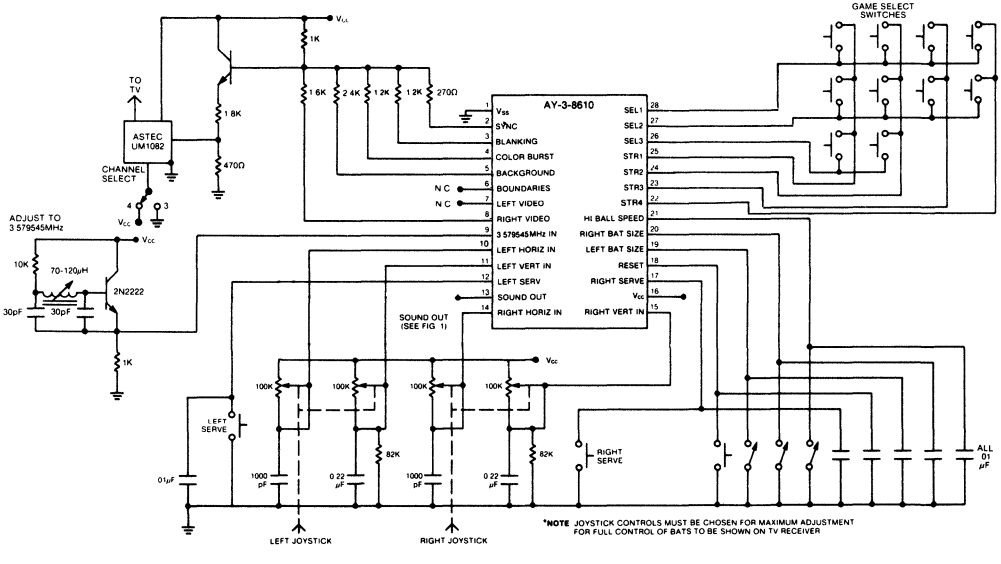


Fig. 1 BLACK AND WHITE IMPLEMENTATION

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} Pin ..... −0.2 to +12V
Storage Temperature Range ..... −20° C to +70° C
Ambient Operating Temperature Range ..... 0° C to +40° C

Standard Conditions (unless otherwise noted)

V_{CC} = +7.5 to +9.0V
V_{SS} = 0V

*Exceeding these ratings could cause permanent damage to these devices. This is a stress rating only and functional operation of these devices at these conditions is not implied — operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics**	Min	Typ	Max	Units	Conditions
Clock Input					
Frequency	—	3.579545	—	MHz	
Logic '0'	0	—	0.5	V	50% duty cycle ±5%
Logic '1'	V_{CC} −2	—	V_{CC}	V	
Leakage	—	—	100	μA	
Control Inputs 12, 17, 18, 19, 20, 21, 26, 27, 28					Max. contact resistance of 1K to V_{SS}
Logic '0'	0	—	0.5	V	
Logic '1'	V_{CC}−2	—	V_{CC}	V	
Input Impedance	—	100	—	KΩ	Pull up to V_{CC}
Outputs Pins 2-8, & 13					
On	—	—	1	V	I_{out} = 2mA
Off	—	—	100	μA	V_{out} = V_{CC} (open drain)
Outputs Pins 22-25					
On	—	—	1	V	I_{out} = 0.5mA
Off	—	—	100	μA	V_{out} = V_{CC} (open drain)
Power supply current	—	—	60	mA	At V_{CC} = +7.0V

**At 25°C & V_{CC} = 6V

Motor Cycle

FEATURES

- Full color operation with AY-3-8615 color processor
- 4 game selections—Time Out, Obstacle Race, Moto Jump and Rally Run
- 2 skill selections—PRO/AM
- 625 line (CCIR) and 525 line (NTSC) pin selectable
- Internal TV (raster) generator
- Automatic on-screen scoring
- Realistic sound effects

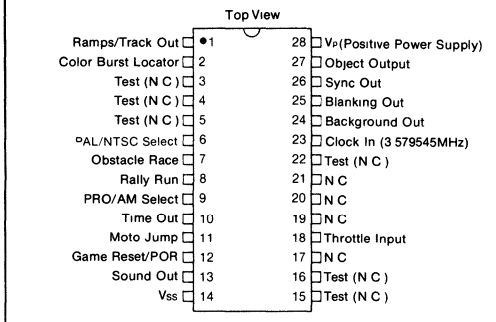
DESCRIPTION

Motor Cycle is a game for one player who controls the speed of a motorbike and rider. At the start of each game the motorbike and rider are stationary at the upper left-hand side of the TV screen As the player moves the joystick, the motorbike and rider move across the screen on track 1. The motorbike sound starts with the bike movement and as the bike and rider accelerate, the motorbike sound reflects these speed changes. The motorbike wheels have an appearance of rotating at a speed also related to the throttle setting

At the end of track 1 the bike and rider reappear on track 2 at the left-hand side, and likewise at the end of track 2 the bike appears on track 3 at the left-hand side of the screen The movement of the bike and rider on track 3 to the right edge of the screen will cause a reinitialization of the bike and rider at the left of the screen on track 1. There will be no movement until the throttle is reset to a slow speed and then increased. Figure 1 shows the playing field for each game.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



GAME OPERATIONS

Time Out

The object of this game is to reach the end of track 3 in the shortest time The three-digit score is automatically reset as the rider first begins to move on track 1 and the score is incremented until the game is over The score appears centered on the screen above track 1, and the score remains until the start of the next game.

Time Out requires a speed shifting to achieve the lowest time scores. As the throttle speed is increased and the rider begins to move, the bike object is in speed one and moves at a set rate across the screen. The only way to accelerate the bike object motion is to return the throttle to a "slow" position and then turn to a "fast" position. This shifting procedure will move the bike into speed 2 and the object will go across the screen at a faster rate. Another "shift" will allow speed 3

A PRO/AM option switch is provided to select a difficulty factor. In the hard mode, a crash occurs if the player tries to increase the throttle speed too rapidly. A crash will flip the bike and rider upside down and the sound will be a high-pitch screech. At the end of the crash the bike and rider are reinitialized on track 1 and the score reset. In the easy mode no crash is allowed.

Obstacle Race

As the throttle speed is increased, the bike and rider move across track 1 at a rate determined by the throttle controller setting Obstacle Race has no speed shifting Located on each of the three tracks are obstacles. The easy/hard option switch selects the number of obstacles per track. The easy mode has one obstacle per track and the hard mode has two obstacles per track.

The object of this game is to traverse the three tracks in the shortest time, doing a wheelie over each obstacle. The score counters record the run time in the same manner as the Time Out Game

In Obstacle Race the crash is not caused by accelerating too rapidly. The crash is caused by not doing a wheelie over an obstacle. In the wheelie position, the bike will have the front wheel lifted off the track. A crash into an obstacle will flip the bike upside down and produce the screech sound The score is reset at the end of the crash.

Moto Jump

The object of this game is to control the throttle speed to properly jump the ramp and buses located on track 3 The game begins with 8 buses and with each successful jump over the ramp and buses an additional bus appears The game is over when the maximum number of errors has been reached, which is 3 or 7 errors, depending on the position of the PRO/AM switch. The game is then started by reselecting the Moto Jump game input.

Errors are caused by accelerating too rapidly, insufficient speed to clear the buses, or landing too far past the back ramp after the jump. The bike and rider flip upside down and a screeching sound indicates an error. The score records the number of errors in the first digit and the number of displayed buses in the next two digits.

Rally Run

This game is similar to Moto Jump with the addition of obstacles on track 1 and track 2 The object of Rally Run is to do a wheelie over each obstacle and then adjust the throttle for the correct speed to jump the buses on track 3 The PRO/AM option switch selects two obstacles per track and allows three errors per game in the hard mode, and one obstacle per track and seven errors per game in the easy mode. Errors are caused by accelerating too rapidly, not in wheelie position over the obstacles, insufficient speed to clear the buses, or landing too far past the back ramp after the jump. The score records the number of errors and the number of buses displayed the same as in the game of Moto Jump.

PIN FUNCTIONS

Pin No.	Name	Function
1	Ramps and Tracks	The output of this pin is the video signal of ramps and tracks.
2	Color Burst Locator	The output of this pin is the color time slot which occurs after the sync signal during horizontal blanking.
3	Test	Not Connected
4	Test	Not Connected
5	Test	Not Connected
6	PAL/NTSC	This input is provided with an internal resistor pull-up to V_P. If this input is tied to V_{SS} NTSC (262 vertical lines) is selected. If this input is tied to V_P or allowed to float, PAL (312 vertical lines) is selected.
7	Obstacle Race	This pin is provided with an internal resistor pull-up to V_P. If this input is momentarily connected to V_{SS}, this game will be selected. Otherwise, this pin is normally open.
8	Rally Run	This pin is provided with an internal resistor pull-up to V_P. If this input is momentarily connected to V_{SS}, this game will be selected. Otherwise, this pin is normally open.
9	PRO/AM Option	This pin is provided with an internal resistor pull-up to V_P. If this input is switched to V_{SS}, the PRO (hard) mode is selected. Switching this pin to V_P or allowing it to float selects the AM (easy) mode.
10	Time Out	This pin is provided with an internal resistor pull-up to V_P. If this input is momentarily connected to V_{SS}, this game is selected. This pin is normally open
11	Moto Jump	This pin is provided with an internal resistor pull-up to V_P. If this input is momentarily connected to V_{SS}, this game is selected. This pin is normally open.
12	Game Reset and POR	The input to this pin is provided by an external RC network, which generates a reset signal. This network consists of a 100KΩ resistor from this pin to V_P and a 0.1 μF capacitor from this pin to V_{SS}.
13	Sound	The output of this pin is the sound for the bike engine, bus hit, crash, screech and a good jump. This output is designed to drive a PNP transistor, which in turn drives the game speaker.
14	V_{SS}	This input is the negative power supply.
15	Test	Not Connected
16	Test	Not Connected
17	N.C.	Not Connected
18	Throttle	The input to this pin is an oscillator signal for controlling the motion of the bike and rider.
19	N.C.	Not Connected
20	N.C.	Not Connected
21	N.C.	Not Connected
22	Test	Not Connected
23	Clock In	The input to this pin is the 3.58MHz oscillator.
24	Background	This output provides the background video signal.
25	Blanking	This output provides the horizontal composite blanking between each line of video information.
26	Sync	This pin provides the combined output of horizontal sync or vertical flybacks.
27	Object Output	The output of this pin is the video output signal for the bike, buses, score and obstacles.
28	V_P	This input is the positive power supply.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} ..... −0.3 to +12V
Storage Temperature Range ..... −20° to +70° C
Ambient Operating Temperature Range ..... 0° C to +40° C
Operating Voltage Supply Range ..... +7.5 to +9 Volts

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied — operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise noted)

Parameter values at $T_a = 25°C$

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics	Min	Max	Units	Conditions
Clock In (Pin 23)				
Frequency	—	—	MHz	Nominal 3.579545
Input low voltage	V_{SS} −0.3	V_{SS} +0.3	V	
Input high voltage	V_{SS} +6.5	V_P	V	
Duty Cycle	35	65	%	Clock swing from 0 to V_P
Throttle (Pin 18)				
Frequency	50	250	KHz	
Pulse width—positive	1.5	—	μs	
Input low voltage	V_{SS} −0.3	V_{SS} +0.2	V	
Input high voltage	V_{SS} +6.5	V_P	V	
Inputs (Pins 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 16, 22)				
Input high voltage	V_{SS} +6.5	V_P	V	
Input low voltage	V_{SS} −0.3	V_{SS} +0.2	V	
Sound Output (Pin 13)				
Voltage output low vol.	—	V_{SS} +0.5	V	Force 0.75mA at $V_P = 7.5V$
FTC Out (Pin 19)				
Voltage output low (V_{ol})	—	V_{SS} +0.5	V	Force 0.5mA at $V_P = 7.5V$
Other Outputs (Pins 1, 2, 24, 25, 26, 27)	—	V_{SS} +0.5	V	Force 1.0mA at $V_P = 7.5V$
Voltage output low (V_{ol})	—	—	—	
Power Supply Current	—	75	mA	At $V_P = 7.5V$

VIDEO

TUNING 10

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			Television
ECONOMEGA IIA DIGITAL TUNING SYSTEM	Provides electronic control of a varactor tuned TV from keyboard entry.	AY-3-8211	10-4
FREQUENCY LOCKED LOOP TUNING SYSTEMS	Provides frequency locked loop tuning in radio, TV applications.	Economega III	10-8
PHASED LOCKED LOOP TUNING SYSTEM SYNTHESIZER	Provides PLL frequency synthesis for color TV tuning.	Economega IV	10-19
		AY-3-2012	10-22
		CT2010	10-27
		CT2017	10-29
PHASED LOCKED LOOP TV TUNING SYSTEM CONTROL	Provides control and interface for PLL television tuning.	PIC1650-020	10-33
		ER1400	10-33
			Synthesizer/Counter
FREQUENCY SYNTHESIZER/ COUNTER	Provides a time base for frequency synthesizer counting.	AY-5-8105	10-44
			EAROM
512 BIT EAROM	512 bits organized 32 x 16.	ER2051	10-48
		ER2051 IR	10-48
		ER2051 HR	10-48

TUNING

GENERAL INSTRUMENT

Television

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
ECONOMEGA IIA DIGITAL TUNING SYSTEM	Provides electronic control of a varactor tuned TV from keyboard entry.	AY-3-8211	10-4
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		AY-3-2012	10-22
		CT2010	10-27
		CT2017	10-29
PHASED LOCKED LOOP TV TUNING SYSTEM CONTROL	Provides control and interface for PLL television tuning.	PIC1650-020	10-33
		ER1400	10-33

ECONOMEGA IIA Digital Tuning System

FEATURES

- 16/32 Program Options
- 4 Bands
- 14 Bit Tuning Resolution on B3
- Program Copying
- Non-Volatile Memory without Battery
- Manual Up/Down Tuning
- Manual Band Switching
- Mute Output at Program Selection
- Search Active Output
- Local Program Up/Down Control
- Validate Circuitry
- Referenced Tuning Waveform Output
- Band Step Option 3/4 Select

DESCRIPTION

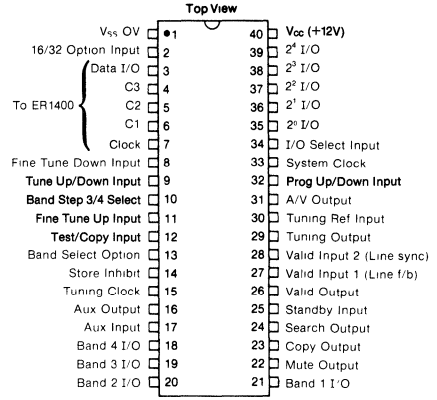
The Economega IIA Digital Tuning system is a voltage synthesizer for both Radio and TV manual tuning applications.

The AY-3-8211 N-Channel control chip interfaces directly with an ER1400 non-volatile memory enabling storage of up to 32 programs.

Variable mark space ratio tuning information from the AY-3-8211 is amplified and filtered, and the resulting DC level used to control the TV or Radio tuner

PIN CONFIGURATION

40 LEAD DUAL IN LINE



OPERATION

Tuning—Resolutions are as follows:

	Option 1	Option 2
B1 (Band 1)	11 bits (16mV)	12 bits (8mV)
B2 (Band III), B4	12 bits (8mV)	13 bits (4mV)
B3 (UHF)	14 bits (2mV)	14 bits (2mV)

These are the tuning information incrementing resolutions controlled by the Tune Up/Down, Band Inputs, and Fine Tune inputs. Voltages relate to approximately 30 volt tuning range.

Fine Tune—The Fine Tune steps approximately 8 times per second (related to system clock). The Fine Tune input is disabled when searching (Band inputs pressed or Tune Up/Down active) and when Mute is active Tuning resolutions as above.

Scanning—The actual tuning rates, fixed by the Tuning Clock, may be adjusted over a wide limit, typical figures are quoted below

Operation of a Band Input or Tune Up/Down initiates scanning on the selected band, and the Search O/P goes low.

Typical Scan rates are as follows:

Band	Scan Time Option 1	Option 2
1	1.25 sec	2 5 sec
2, 4	2.5 sec	5 sec
3	10 sec	10 sec

This corresponds to a Tuning Clock of approximately 1.6KHz.

When the Tuning Output overflows, scanning pauses for 256ms to allow time for the tuning voltage, and if in Band Step Mode, the Band outputs to settle.

This pause occurs at the bottom of the tuning range when tuning up and at the top of the tuning range when tuning down.

Muting—When a program change is made, at Power ON, and Standby to OFF, the mute output is activated for 256 msecs and disables the Fine Tune inputs for this time, Mute O/P is also active while scanning; i.e. when a Band I/P or Tune Up/Down I/P is active.

Tuning Procedure—Three tuning procedures are available:

(a) 1 Select required program number (1 to 16 or 32).
2. Press required band button, scanning commences from the station currently tuned, scanning stops immediately upon release of button.
3. Fine tune if required.
4. Tuning information is stored automatically upon release of band button or release of Fine Tune button.
5. Tuning information may be copied by pressing Copy and selecting a new program number.

(b) With Tuning Option selected:
1. Select Band—this is latched on.
2 Tune Up or Down using Tune Up/Down Input
3 Fine Tune if required.
4. Tuning information is stored automatically upon release of Tune Up/Down or release of Fine Tune Up/Down.
5. A program location is selected by first pressing Copy and then selecting the required Program number.

(c) With Band Step 3 or 4 selected and Tuning Option Selected:
1. Select band—this is latched on.
2. Tune Up or Down (Tuning will now follow from band to band).
3. Once a station is tuned, release Tune Up/Down and Fine Tune, if required.
4. Tuning information is stored automatically upon release of Tune Up/Down or release of Fine tune Up/Down.
5. A Program location is selected by first pressing copy and then selecting required program number.

Output Signals—Tuning voltage and Band outputs are not disturbed by internal sequences, for example; STORE and COPY. Only program change will disturb these outputs—program change being either a change of band and/or tuning information.

TUNING

Memory Recall—The memory recall sequence is triggered by a program change and, after the 256 millisecond Power On reset. The sequence is as follows:

a) 20 millisecond antibounce delay on the I/O Select or Program inputs.

b) Mute and Fine Tune input inhibit triggered for 256 milliseconds and memory read initiated.

c) Approximately 12 milliseconds after initiation of memory read, new tuning and band information will be output.

d) Remainder of the 256 milliseconds period allows time for the band drives and tuning voltage to settle.

Power On—At power on (V_{CC} on), a 256 millisecond reset allows the power supplies to settle. Mute is active for this period and all inputs are inhibited. At the end of this 256 millisecond period a memory recall sequence is triggered.

Three recall modes are possible:

a) I/O select low (input) mode—in this case band and tuning voltage information will be output for the program number input.

b) I/O select high (output) mode—program 1 together with associated band and tuning voltage information will be output.

c) I/O select open circuit—program 1 band and tuning information will be output. If I/O Select goes high, program 1 will be output on the Program I/O lines.

Standby—When leaving standby, Mute is activated for 256 milliseconds, and all inputs are inhibited. A memory recall sequence now follows this delay period. Memory recall occurs regardless of program change status. Three Standby off modes are possible:

a) I/O Select in either output mode or open circuit. Program information will be as it was prior to Standby.

b) I/O Select in input mode, program remains unchanged. Program information will be as it was prior to Standby.

c) I/O Select in input mode and program changed. The new program information will be output during the memory recall sequence.

Tuning Output Waveform—The tuning output is a rectangular waveform of variable mark space ratio. This output is filtered to produce the tuning voltage. The mark space ratio and tuning voltage can be varied, up to a maximum resolution on Band 3, of 14 bits. See Tuning for the resolutions on other bands.

Seven fundamental frequency components can be present in the output waveform, depending upon tuning position. The following table lists these frequencies together with their maximum effective mark space ratios. The condition for which all 7 components make up the output waveform would result in a condition of maximum ripple at the output of the tuning filter. The worse case tuning voltage ripple can, therefore, be determined.

TABLE 1 FUNDAMENTAL TUNING WAVEFORM COMPONENTS

Frequency	Mark/Space Ratio
4kHz	1:1
2kHz	1:511
1kHz	1:1023
500Hz	1:2047
250Hz	1:4095
125Hz	1:8191
62.5Hz	1:16383

Program change timing with I/O Select in input mode (low)

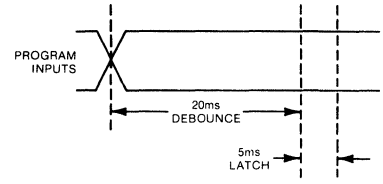


Fig. 1 PROGRAM STROBE TIMING

Any program input change is detected and, after a 20 millisecond antibounce period, the program lines are latched in and the corresponding tuning information output. The program lines must be stable for the 5 millisecond 'latch' time shown above.

Latched Program information using I/O Select feature

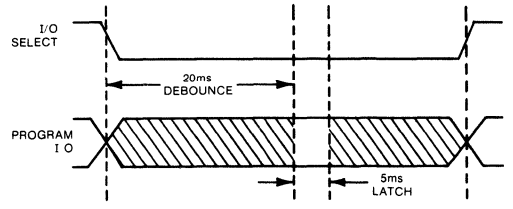


Fig. 2 LATCHED PROGRAM TIMING

I/O Select to low converts the program lines to input mode and triggers a 20ms antibounce period. The program lines are then latched into the chip and the corresponding tuning information output. The program data must be stable for the 5ms latch period. I/O Select to high converts the program lines back to the output mode.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} pin ..... −0.3V to +20V
Ambient Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied — operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

Temperature 0°C to +70°C
V_{SS} = 0V
V_{CC} = +12V = ±10%
System Clock = 1.44 to 2.15MHz (2.048MHz) Nominal (10.8 to 13.2 Volts)

Characteristic	Min	Typ	Max	Units	Conditions
Option (2, 13), Fine Tune Up (11), Fine Tune Down (8) Inputs					
Low Level	V_{SS}	—	3	V	
High Level	V_{CC}-3	—	V_{CC}	V	
Pull Up to V_{CC}					
Low Level Source	—	—	0 5	mA	V_{IN} = V_{SS}
High Level	V_{CC}-3	—	—	V	I_{SOURCE} = 10μA
Standby (25) Auxiliary (17) Inputs					
Low Level	V_{SS}	—	3	V	
High Level	V_{CC}-3	—	13.2	V	
Input Leakage to V_{SS}	—	—	10	μA	V_{IN} = 13.2 Volts
Store Inhibit (14), Test/Copy (12) Tune Up/Down(9),Band Step 3/4 Select (10), Program Up/Down (32), I/O Select (34) Inputs					
Low Level	V_{SS}	—	1	V	
'Open Circuit' Level	3	—	0.5V_{CC}	V	
High Level	V_{CC}-3	—	V_{CC}	V	
Pull Up to V_{CC} (Note 3)					
Low Level Source	—	—	0.5	mA	V_{IN} = V_{SS}
'Open Circuit' Level	3	—	—	V	I_{SOURCE} 10μA
Pull Down to V_{SS} (Note 3)					
High Level Sink	—	—	0.5	mA	V_{IN} = V_{CC}
'Open Circuit' Level	—	—	0.5V_{CC}	V	I_{SINK} 10μA
Band Input/Output (18 to 21)					
Output Low Level	3	—	5	V	I_{SINK} 5mA
Off Leakage to V_{SS}	—	—	10	μA	V_{OUT} = V_{CC}
Input Low Level	V_{SS}	—	1	V	
Input High Level	3	—	V_{CC}	V	
Copy (23), Mute (22), Search (24), Auxiliary (16), A/V (31) Outputs					Open Drain
Low Level	—	—	1	V	I_{SINK} (max) = 10mA
Off Leakage to V_{SS}	—	—	10	μA	V_{OUT} = V_{CC}
Program I/O (35 to 39)					
Input Low Level	V_{SS}	—	3	V	
Input High Level	V_{CC}-3	—	V_{CC}	V	
Input Pull Up to V_{CC}					
Low Level Source	—	—	0.5	mA	V_{IN} = V_{SS}
High Level	V_{CC}-3	—	—	V	I_{SOURCE} =10μA
Output Low Level	—	—	0.4	V	I_{SINK} = 1.0mA
Output High Level	As above Pull Up High Level				
Control, Data + Clock Outputs to ER1400 (4, 5, 6, 3 +7)					
Low Level	—	—	1	V	I_{SINK} = 20μA
High Level	V_{CC}-0.5	—	—	V	I_{SOURCE} = 20μA
Rise Time, Fall Time (Note 2)	—	—	1	μs	C = 30pf
Clock to ER1400 (7)	11.25	16 0	16.79	KHz	System Clock ÷ 128
(50% Duty Cycle)					
Data Input from ER1400 (3)					
Low Level	*	—	3	V	*Note 4
High Level	V_{CC}-3	—	V_{CC}	V	
Input Leakage to V_{SS}	—	—	10	μA	V_{IN}= V_{CC}
Input Leakage from V_{CC}	—	—	8	μA	V_{IN} = 3 Volts

TUNING

Characteristic	Min	Typ	Max	Units	Conditions
Tuning Clock (15)					
External Resistor to V_{CC}	47	—	1000	KΩ	
External Capacitor to V_{SS}	1.0	—	220	nf	
Leakage to V_{SS} (Tuning Clock OFF)	—	—	1	μA	$V_{IN} = V_{CC}$
System Clock (33)					
External Resistor to V_{CC}	2	—	330	KΩ	
External Capacitor to V_{SS}	10	—	100	pf	Normally adjusted for 16.0KHz at Pin 7.
Valid 1 (27) Valid 2 (28) Inputs	*				
Low Level		—	3	V	*Note 4
High Level	V_{CC}-3	—	V_{CC}	V	
Input Leakage to V_{SS}	—	—	10	μA	$V_{IN} = V_{CC}$
Valid Output (26)					Push Pull
Low Level	—	—	1	V	I_{SINK} = 0.4mA
High Level	V_{CC}-1.0	—	—	V	I_{SOURCE} = 1mA
Tuning Output (29)					V_{REF} = 5 to 7.1 Volts
Low Level	—	—	0.4	V	I_{SINK} = 500μA
High Level	V_{REF}-0.4	—	—	V	I_{SOURCE} = 100μA
Rise Time, Fall Time 10-90%	—	—	50	ns	C = 10pf
Tuning Reference (30)	5	—	7	V	
Supply Current Vcc (40)	—	—	50	mA	T = 70°C

NOTES: 1. All Pull Ups, unless otherwise stated, are configured with depletion FET's with gate connected to source. They have non-linear VI characteristics.
2. Rise time and fall times measured V_{CC}-1 to V_{CC}-8 Volts.
3. Tristate 'Pull Ups' and 'Pull Downs' are configured with enhancement FET's. They have non-linear VI characteristics.
4. Guard ring to clamp any input more negative than V_{SS}. Maximum clamp current = −100μA.

PIN FUNCTIONS

Pin No.	Name	Function
1	Vss	Connect to zero volts.
2	16/32 Program/Resolution Option	Selects program number and tuning resolution. Low 32 mode, high 16 mode.
3	Data I/O	To ER1400
4	C3	
5	C2	
6	C1	
7	16KHz Clock	System Clock ÷ 128
8	Fine Tune Down	When connected, a low causes Fine Tune to decrement automatically at approximately 8 steps/second. There is a pause of approximately ⅛ second before the first step is executed. The input is disabled if either a Band Input is selected, Tune Up or Tune Down is selected, or if MUTE is active. Tuning information is stored when Fine Tune Down is released. There is a 20 millisecond debounce on the store function.
9	Tune Up/Down Input	Tristate input which determines Tuning direction. Tune down for low, tune up if open circuit or connected high. When using the Band Select Option this input is used for tuning, low tune down, high tune up, and open circuit OFF. The Fine Tune Up/Down input is inhibited while tuning and tuning information is stored automatically upon release of either tune up or down. There is a 20ms antibounce delay on the store function. Note: Tuning will occur if this input is active, independent of the Band Inputs.
10	Band Step 3/4 Select	Tristate input. When connected low the 3 band step search mode is selected. When connected high the 4 band step search mode is selected. Tuning is now carried out using the Tune Up/Tune Down input.

	Resolution		
	B1	B2, 4	B3
Open 16 Prog.	11	12	14
Low 32 Prog.	12	13	14

In the 16 program mode, program numbers up to 32 are accepted on the 2^0, 2^1, 2^2, 2^3 and 2^4 inputs. The number of programs is limited to 16 only when the Program Up/Down input is used.

TUNING

Frequency Locked Loop Tuning Systems

INTRODUCTION

Economega III is a powerful Frequency Locked Loop (FLL) tuning system with applications in Radio, TV and wherever the control of frequency or speed is required. It is based on the General Instrument PIC series of single chip microcomputers.

The FLL principle can be used for many applications with many varied implementations. Some examples are shown later but it should be emphasized that the system is specifically designed to be flexible and that variants having other features and cost/performance trade-offs can be provided.

Depending upon the requirements, the system will use any of the General Instrument PIC's (1650A, 1655A, 16C55, 1656, 1670, etc.) with or without an EAROM (ER1400, ER2055, etc.).

Low cost and simplicity are the key features of Economega III.

TUNING SYSTEMS

The Superheterodyne Receiver

Practically all Radio and TV receivers currently manufactured are of the Superheterodyne variety. These receivers mix the incoming signal with local oscillator to translate the signal to a third, fixed lower frequency called the Intermediate Frequency (IF). Most of the amplification and selectivity is provided at the IF, the signal is then demodulated to recover the Audio or Video. The receiver is tuned by varying the local oscillator frequency. The frequencies are related by the following equation:

$F_S = F_{LO} - F_{IF}$

(in the typical case where the oscillator frequency is higher than the signal frequency).

To take a specific example in the FM Band,

if $F_S = 87.7MHz$, $F_{IF} = 10.7MHz$

then F_{LO} must be set to 98.4MHz.

A simplified block diagram of an FM receiver is shown in Fig. 1

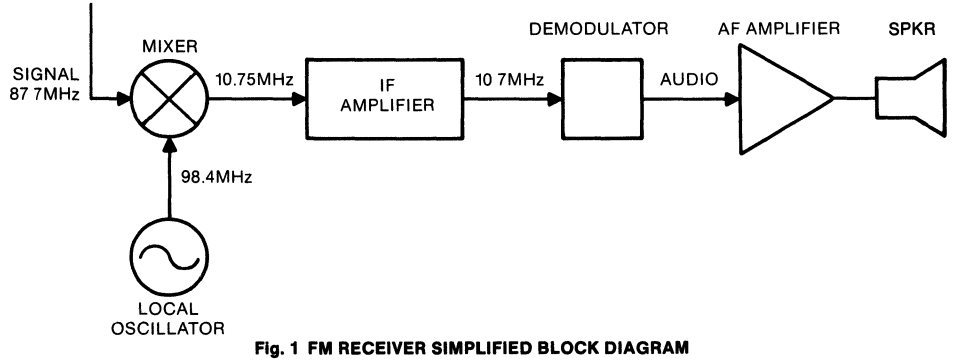


Fig. 1 FM RECEIVER SIMPLIFIED BLOCK DIAGRAM

Mechanical Tuning

The classical way to tune a receiver is to use a mechanical variable capacitor with a knob, slow motion drive, scale and pointer. This method is used in virtually all portable radios and in many low end TV sets (Figure 2).

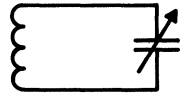


Fig. 2 MECHANICAL TUNING

Varactor Tuning

Here the bulky and inconvenient mechanical variable capacitors are replaced by Varactor Tuning Diodes which are voltage variable. They thus open up the way to electronic tuning. In the simplest implementation the tuning voltage is provided from a voltage reference by a potentiometer or bank of potentiometers (Figure 3).

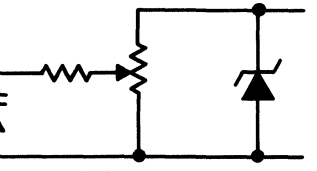


Fig. 3 VARACTOR TUNING

TUNING

Voltage Synthesis

The first mass production electronic tuning systems replaced the potentiometers with a digital store and a D/A convertor (Figure 4).

The digital words are stored in a non-volatile memory such as an ER1400. Since the tuning is fully electronic, it becomes relatively simple to add features that were previously difficult or uneconomic, such as favorite program storage, automatic tuning, remote control.

The systems so far described are all open loop and demand a high order of stability in all components to achieve long-term accuracy of tuning. Furthermore, there is no inherent readout of frequency availability, and expensive mechanical or electronic arrangements are necessary if readout is desired. Finally, if any component is changed, the receiver will have to be completely retuned. These disadvantages encouraged the adoption of closed loop systems where a highly stable quartz crystal is used as control reference.

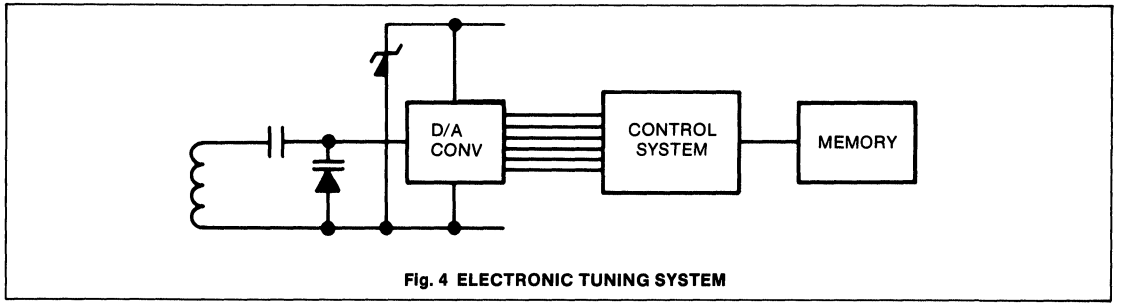


Fig. 4 ELECTRONIC TUNING SYSTEM

Phase Locked Loop (PLL) Frequency Synthesis

This was the first closed loop system to be adopted and was initially used in professional radio communications equipment which demand high stability and accuracy in extreme environments, using components that make it difficult or impossible to achieve the requirements using simpler techniques.

The basic system operates by phase locking a sub-multiple of the local oscillator frequency to a crystal controlled reference (for example a 1KHz reference and a 1MHz oscillator divided by 1000). By altering the division ratio, the oscillator frequency can be altered in steps (e.g. to 1.001MHz by using a divide by 1001). The local oscillator is varactor tuned and the tuning voltage is set by the output of a phase comparator which compares the reference and the divided local oscillator signal. As the oscillator tries to drift off frequency, the phase comparator output changes and the tuning voltage is readjusted to compensate. The rate at which corrections can be made is high, commonly more than 1000 per second. This is fast enough to improve the noise spectrum of a noisy oscillator or to reduce frequency modulation caused by mechanical vibration.

A basic PLL Synthesizer is shown in Figure 5.

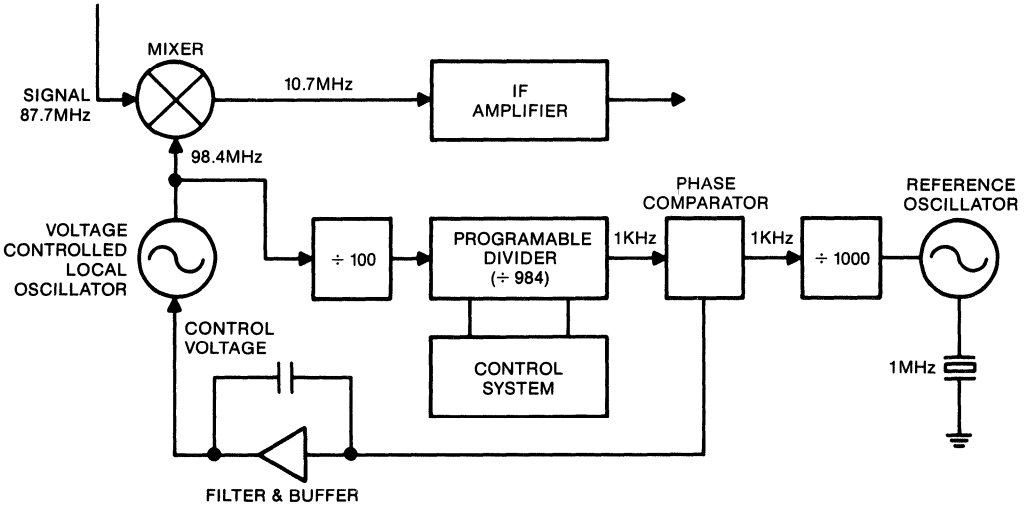


Fig. 5 BASIC PLL SYNTHESIZER

Practical systems are often more complicated, especially where small frequency steps are required.

A typical system would contain a high frequency dual modulus divider (in ECL technology), a synthesizer (consisting of programable divider, reference divider and phase comparator), a buffer amplifier/filter, and a control block (usually a microcomputer). For certain well defined applications, some or all of the blocks may be contained in one integrated circuit.

Frequency Locked Loop (FLL) Frequency Synthesis

The FLL synthesizer approaches the problem from a different direction. It assumes that it is fairly easy to make a low noise oscillator with good short-term stability (every conventional Radio and TV has one) and aims to add long-term stability and a means to accurately set the frequency.

At the heart of the system is a varactor tuner, the frequency of which is determined by the voltage stored on a capacitor. The basic stability of the tuner and the discharge rate of the capacitor are ideally specified so that uncorrected, the frequency would stay within acceptable limits for several seconds.

Longer-term stability is achieved by counting the frequency and comparing it with the desired frequency. If the error exceeds acceptable limits a current pulse is fed to the capacitor to readjust the tuning voltage and bring the oscillator onto frequency. The amplitude and length of the pulse may be made proportional to the error to speed the initial tuning procedure.

To tune the system initially, it is desirable to repeat the frequency measurement fairly rapidly to minimize the tuning time. Once on tune, however, the measurements need only be made intermittently and measurement cycles may be omitted as desired. The system because of this, lends itself to implementation in software and the system control microcomputer can do the tuning as well. Compared to a PLL, the synthesizer block has been eliminated. Another simplification is in the prescaler which can be a simple divider.

Frequency synthesizer systems inherently give a frequency readout and, since microcomputers are used as controllers, it is very easy to provide features to simplify operations and differentiate products (Figure 6).

There is only one application for which FLL is not entirely suitable; single sideband reception. For this class of transmission, a very high order of short-term stability is required, a simple FLL system does not control the frequency closely enough.

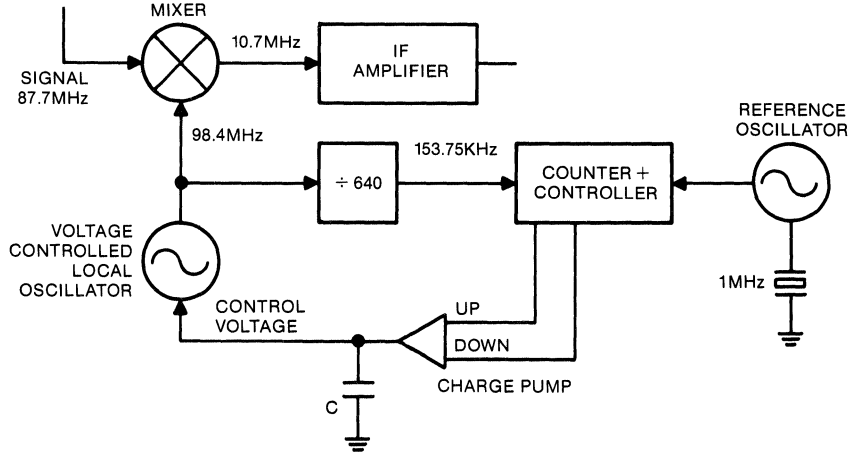


Fig. 6 BASIC FLL SYNTHESIZER

ECONOMEGA III

Introduction

Economega III is a family of Tuning Systems with a wide variety of applications . All the variants have in common the FLL principle and the General Instrument PIC microcomputer. The implementation, however, varies considerably as each has a different trade-off between cost, performance and features.

Each member of the family is designated by a letter suffix (e.g. Economega III E) and an optional numerical suffix where there is a minor variant (e.g. Economega III E-1). The individual PIC used is identified by its type and pattern number (e.g PIC1650A-031). Full PIC data sheets are in the Microcomputer section of this catalog

Six existing Economega III systems are briefly described and compared in the following sections.

Economega IIIA

This system is programed for European TV applications and tunes 61 channels in 3 bands. Favorite program storage is provided in EAROM for 16 stations (Figure 7).

The control loop has been optimized to give high stability and low noise together with fast locking.

A PIC1650A microcomputer is used as the control element and an ER1400 as the favorite program store together with a ÷4096 prescaler (÷256, ÷16).

FEATURES

- Tunes CCIR Channels 2-4, 5-12 and 21-71
- Three Bands
- Non-Volatile Storage of 16 Favorite Programs
- Fine Tune ± 4MHz in 50KHz steps
- 2 + 2 Digit Display of Program and Channel Number
- Lock Time 200ms (max)
- 38 9MHz IF
- Local Commands for Channel 10's, Channel 1's, Fine Tune Up, Fine Tune Down
- Parallel Remote Control Input for Program Number
- Customizing Service Available

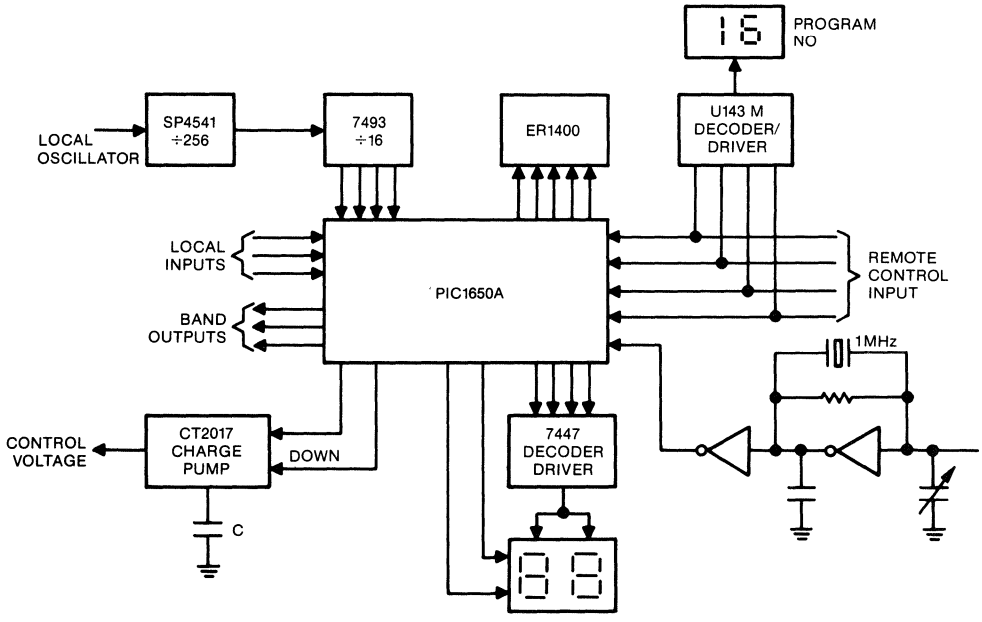


Fig. 7 ECONOMEGA III A BLOCK DIAGRAM

TUNING

Economega IIIB

This system is programed for USA TV applications and tunes 82 channels in 3 bands. Favorite channel storage is provided in EAROM. A remote control receiver function is incorporated. This, in addition to controlling the tuning, provides a main ON/OFF output and a 16 step volume control (Figure 8).

A PIC1650A microcomputer is used as the controller and an ER2055 as the favorite channel store together with a ÷ 2048/4096 prescaler (÷128, ÷16/32).

FEATURES

- Tunes 82 Channels
- Three Bands
- Favorite Channels Stored in EAROM
- Built in Remote Control Receiver
- Main ON/OFF Output
- 16 Step Volume Control
- Local Control of Volume and Channel
- Output for On Screen Display
- Lock Time 200 ms (typ)
- Customizing Service Available

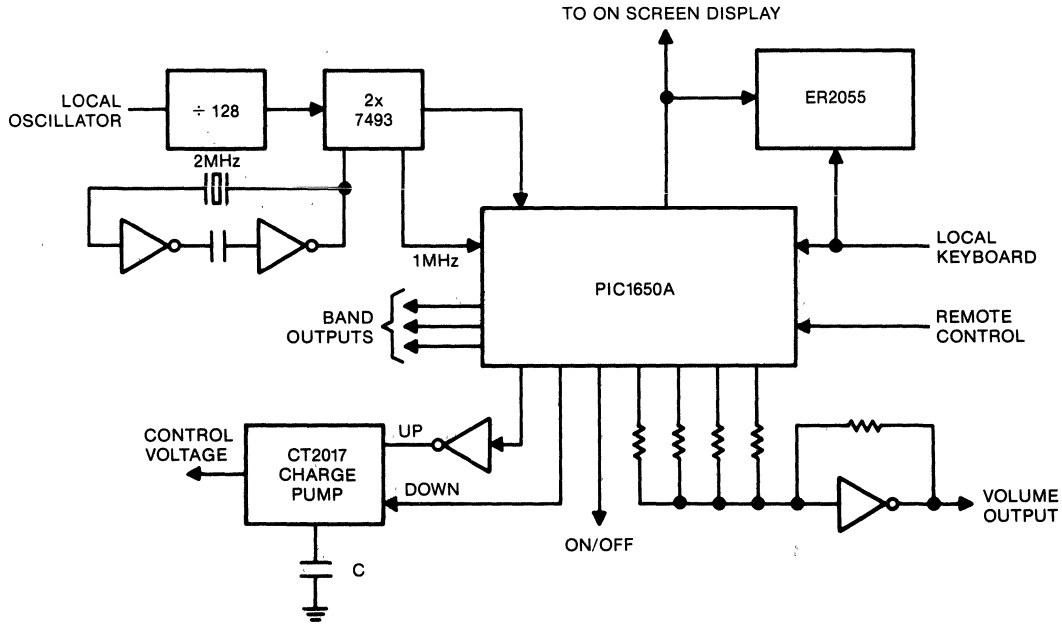


Fig. 8 ECONOMEGA IIIB BLOCK DIAGRAM

Economega IIIC

This system is programed for USA TV applications and tunes 82 channels in 3 bands. Favorite channel storage is provided in RAM. A remote control receiver function is incorporated. This, in addition to controlling the tuning, provides a main ON/OFF output and a 16 step volume control (Figure 9).

A PIC1650A microcomputer is used as the controller together with a ÷2048/4096 (÷256; ÷8/19) prescaler and a 2102 RAM for favorite channel storage.

FEATURES

- 82 Channels
- Three Bands
- Favorite Channel Storage in RAM
- Two Digit LED Display
- Local Keyboard
- Built in Remote Control Receiver
- 16 Step Volume Control
- Main ON/OFF Output
- Lock Time 200 ms (typ)

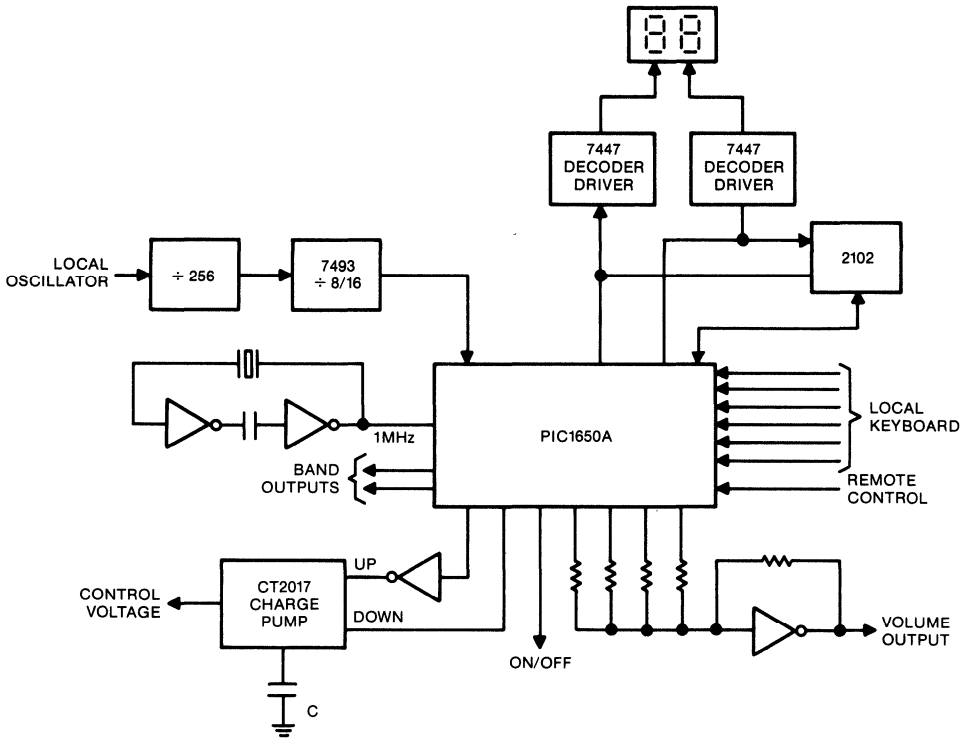


Fig. 9 ECONOMEGA IIIC BLOCK DIAGRAM

TUNING

Economega IIID

This system is programed for USA Radio applications and tunes MW and FM bands. It has direct frequency entry, manual tuning and a seek function (Figure 10).

A PIC1656 microcomputer is used as the controller together with a ÷16/640 prescaler (÷80; ÷8/16).

FEATURES

- AM Band 530KHz to 1610KHz, 10KHz Channels, 455KHz/260KHz IF
- Direct Frequency Entry
- Manual Tune Up/Down
- Seek
- Fine Tune Up/Down
- 4 Digit LED Display
- Customizing Service Available

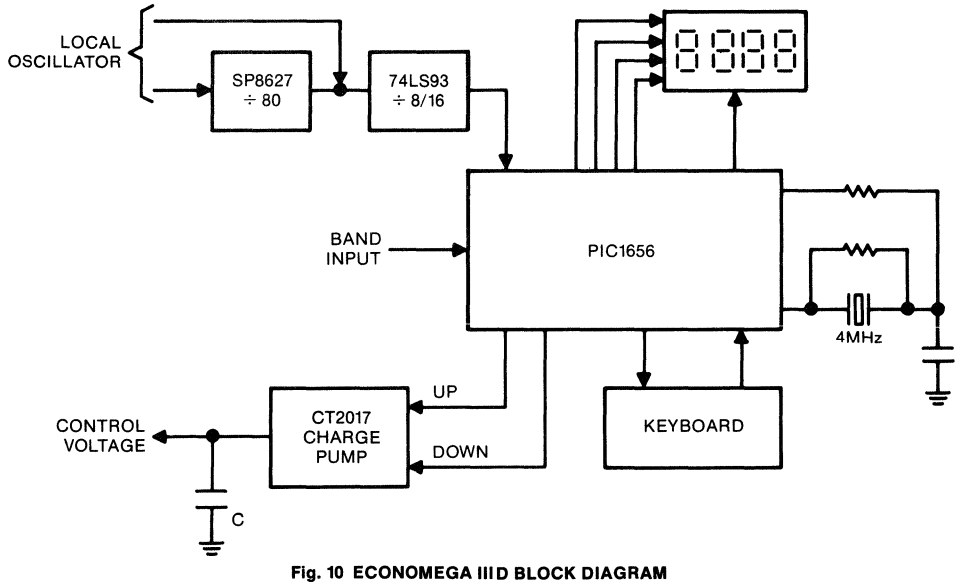


Fig. 10 ECONOMEGA IIID BLOCK DIAGRAM

Economega IIIE

This system is a high performance Radio Tuning System programed for European applications. It tunes MW and VHF bands and provides storage for 43 favorite programs, direct frequency entry, manual tuning with a knob, and search tuning (Figure 11).

Two PIC1650 microcomputers are used as the controllers, an AY-5-8105 as the FLL counter/display driver and an ER1400 as the favorite program memory together with a ÷8/÷80 prescaler.

FEATURES

- MW Band 510KHz to 1609KHz, 1KHz Steps, 455/459/460/468KHz Selectable IF
- FM Band 87.4-108. 1MHz Steps, 10.64/10.67/10.70/10.73/10.76MHz Selectable IF
- FM Channel Mode
- Storage of 43 Favorite Programs in EAROM
- Direct Frequency Entry with Automatic Range Selection
- Manual Knob Tuning
- Up/Down Search Tuning
- 2 + 5 Digit Fluorescent Display
- Lock Time 300ms (typ)
- Very Low Oscillator Noise
- Customizing Service Available

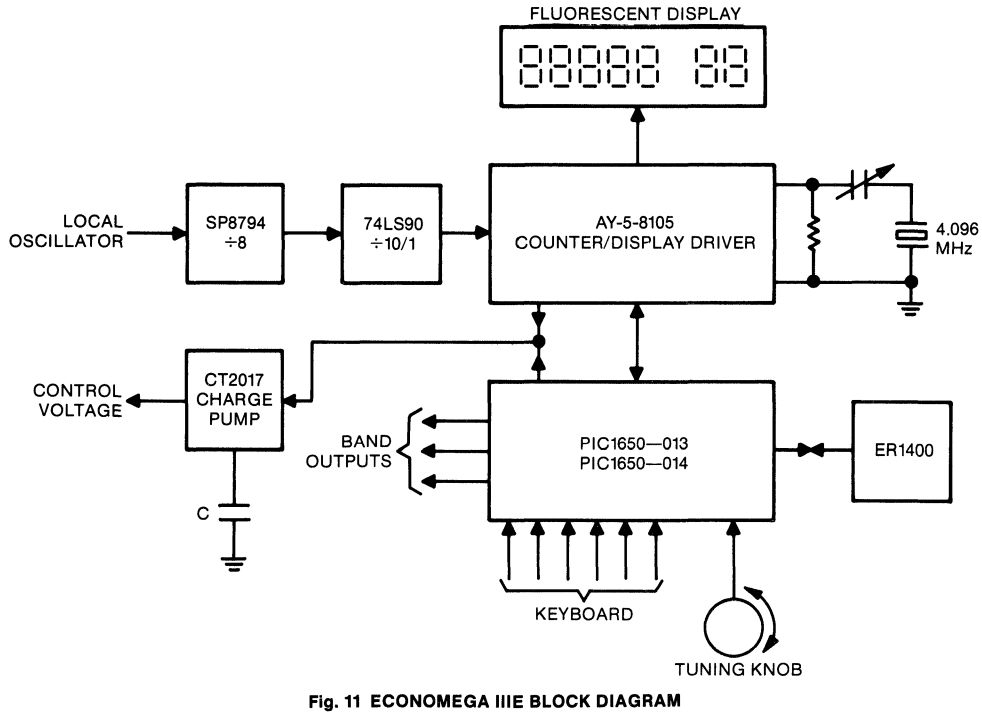


Fig. 11 ECONOMEGA IIIE BLOCK DIAGRAM

Economega III E-1

This system is a variant of Economega III E. It is a high performance Radio Tuning System programed for European applications (Figure 12).

It tunes LW, MW and VHF bands and provides storage for 38 favorite programs, direct frequency entry, push button manual tuning, and search tuning.

Two PIC1650 microcomputers are used as the controller, an AY-5-8105 as the FLL counter/display driver and an ER1400 as the favorite program memory together with a ÷8/÷80 prescaler.

FEATURES

- LW Band 150-265KHz, 1KHz Steps
- MW Band 520-1609KHz, 1KHz Steps
- FM Band 87.4-108.1MHz, 10KHz Steps
- AM IF Programable 455/459/460/468KHz
- FM If Programable 10.64/10.67/10.70/10.73/10.76MHz
- Storage of 39 Favorite Programs (Including Audio Functions)
- Direct Frequency Entry with Automatic Range Selection
- Manual Push Button Tuning
- Up/Down Search Tuning, 9KHz Channels AM, 50KHz Channels FM
- 2 + 5 Digit Fluorescent Display
- Lock Time 300ms (typ)
- Very Low Oscillator Noise
- Customizing Service Available

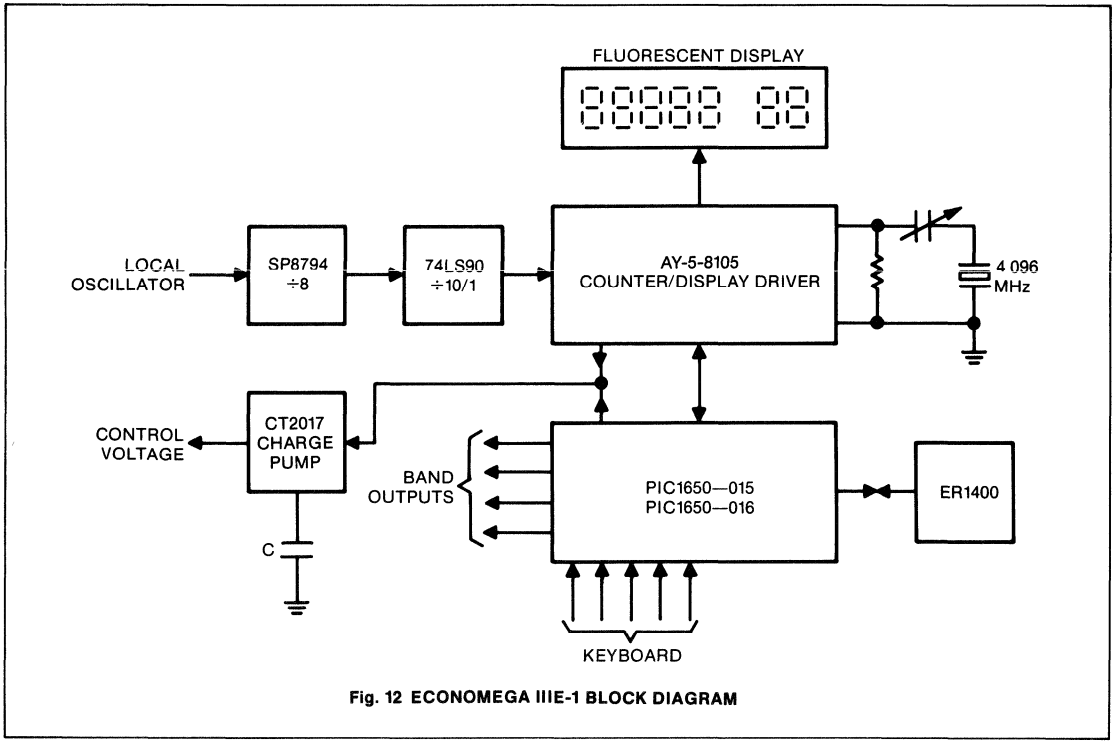


Fig. 12 ECONOMEGA IIIE-1 BLOCK DIAGRAM

TUNING

COMPARISON CHARTS

TABLE 1 TV Tuning Systems — Performance Comparison
TABLE 2 TV Tuning Systems — Components Comparison
TABLE 3 TV Tuning Systems — Performance Comparison
TABLE 4 TV Tuning Systems — Components Comparison

TABLE 1 ECONOMEGA III TV TUNING SYSTEMS — PERFORMANCE COMPARISON

System	Bands/Channels	Tuning	Storage	Display	Fine Tune	Performance	Other
III A	**CCIR** I Ch2—4 III Ch5—12 IV/V Ch21—71	**Remote** Program/ Number **Local** Channel Step Fine Tune Up/Down	EAROM (ER1400) 16 Favorite Programs	2 + 2 Digit LED Program Channel Number	±4MHz 50KHz Steps	Gate Time 10ms Lock Time 200ms (max) Stability ±25KHz Correction Rate: 8Hz absolute (max) 2Hz (typ)	Parallel Remote Control Input Power Supplies +33V +9V +5V −26V
III B	**USA** VHF LO Ch2—8 VHF HI Ch6—13 UHF Ch14—83	**Remote** Channel Number **Local** Channel Up/ Down	EAROM (ER2055) 82 Favorite Channels	On Screen	None	Gate Time 250ms Lock Time 200ms (typ) Stability ±50KHz Correction Rate 4MHz	On Chip Remote Receiver with Volume Control Power Supplies +33V +5V −30V
III C	**USA** VHF LO Ch2—6 VHF HI Ch6—13 UHF Ch14—83	**Remote** **Local**	RAM 82 Favorite Channels	2 Digit LED	None	Gate Time 250ms Lock Time 200ms (typ) Stability ±50KHz Correction Rate 4MHz	On Chip Remote Receiver with Volume Control Power Supplies +33V +5V

TABLE 2 ECONOMEGA III TV TUNING SYSTEMS — COMPONENT COMPARISON (Excluding Displays and Decoupling Components)

System	LSI		MSI/Linear		Discretes		PCB	
III A	PIC1650A	1	SP4541	1	Resistors	20	Holes	191
	ER1400	1	CT2017	1	Capacitors	5		
			7493	1	Diodes	2		
			4049	1	Transistors	7		
			7447	1	Crystal	1		
			LED Driver	1				
III B	PIC1650A	1	Prescaler	1	Resistors	33	Holes	241
	ER2055	1	CT2017	1	Capacitors	4		
			7493	2	Diodes	3		
			7404	1	Transistors	8		
			LM321	1	Crystal	1		
III C	PIC1650A	1	Prescaler	1	Resistors	49	Holes	280
	2102	1	CT2017	1	Capacitors	4		
			7493	1	Diodes	3		
			7404	1	Transistors	6		
			7447	2	Crystal	1		
			LM324	1				

TABLE 3 ECONOMEGA III RADIO TUNING SYSTEMS — PERFORMANCE COMPARISON

System	Ranges	Resolution	Tuning Methods	Storage	Display	Performance	Other
III D	530KHz—1610KHz 87.7MHz—108.1MHz	10KHz 200KHz	Direct Entry Manual Up/Down Seek	None	4 Digit LED	Gate Time 300ms Lock Time Stability Noise Correction Rate Steps	Fine Tune AM ±16KHz, 1KHz Steps FM ±160KHz, 10KHz
III E	510KHz—900KHz 850KHz—1609KHz 87.4MHz—108.1MHz CH2—Ch70+	1KHz 10KHz 100KHz	Direct Entry Seek Up/Down Knob	EAROM 43 Programs on any Range	5 + 2 Digit Fluorescent	Gate Time 8ms Lock Time 300ms Stability ±0.5KHz AM ±5KHz FM Noise 5Hz p-p AM Correction Rate 1Hz (typ)	Automatic Range Selection
III E-1	150KHz—265KHz 520KHz—1609KHz 87.4MHz—108.1MHz Audio 1, 2, 3	1KHz Manual 9KHz Seek 10KHz Manual 50KHz Seek	Direct Entry Seek Up/Down Manual Up/Down	EAROM 39 Programs on any Range	5 + 2 Digit Fluorescent	Gate Time 8ms Lock Time 300ms Stability ±0.5KHz AM ±5KHz FM Noise 5Hz p-p AM 200Hz p-p FM Correction Rate 1Hz (typ)	Automatic Range Selection 3 Audio Ranges

TABLE 4 ECONOMEGA III RADIO TUNING SYSTEMS — COMPONENT COMPARISON
(Excluding Displays and Decoupling Components)

System	LSI		LSI/Linear		Discretes		PCB	
III D	PIC1650	1	SP8627	1	Resistors	37	Holes	217
			74LS93	1	Capacitors	7		
			4016	1	Diodes	9		
					Transistors	15		
					Crystal	1		
III E	PIC1650	2	SP8794	1	Resistors	56	Holes	320
	AY-5-8105	1	74LS90	1	Capacitors	12		
	ER1400	1	LM324	1	Diodes	6		
			CA3080	1	Transistors	8		
			CA3130	1	Crystal	1		
III E-1	PIC1650	2	SP8794	1	Resistors	47	Holes	293
	AY-5-8105	1	74LS90	1	Capacitors	10		
	ER1400	1	LM324	1	Diodes	5		
			CA3080	1	Transistors	7		
			CA3130	1	Crystal	1		

PLL Tuning System

FEATURES

- 100 Channel Tuning Capability — Includes All CCIR Standard Channels, Italian and Australian Special Channels
- 32 Favorite Programs
- Automatic Sweep Tuning Option (with Automatic Fine Tune)
- Fine Tune in 50KHz Steps (Manual for Stable Transmitters, Automatic for Unstable Transmitters)
- Two Digit Channel Display
- Two Digit Program Display
- EAROM Non-Volatile Memory
- Lock Up Time 10ms (typ)

DESCRIPTION

Economega IV is a PLL Frequency Synthesizer system designed for accurate tuning of Color TV. It consists of the following five chips.

(a)	Prescaler and preamplifier — CT2010	8 pin DIL
(b)	Frequency Synthesizer — AY-3-2012	24 pin DIL
(c)	Controller — AY-3-1650	40 pin DIL
(d)	Non-Volatile Memory (optional) — ER1400	14 pin DIL
(e)	Peripheral Circuit — CT2017	18 pin DIL

The controller is microcomputer based and can be reprogramed to provide features and channels as required, with or without favorite program memory and direct channel tuning.

FEATURES PROVIDED WITH CONTROLLER AY-3-1650-20

Channel Entry

Two buttons, tens and units, allow the channel to be set. When operated the number increments every 0.5 sec (there is no carry from the units). On release of the button the channel number is stored in the memory against the selected Program Number.

Program Entry

Activation of parallel 5 bit binary input recalls the required program.

Program Display

Available as a 2 digit multiplexed BCD output.

Channel Display

Available as a 2 digit multiplexed BCD output.

Manual Fine Tune Up/Down

50KHz steps with a range of +4.0MHz and −3.95MHz around the selected channel with roll over at both ends. On depression of the button one step is made. After a delay of 0.4 sec, steps are made every 50ms. The fine tuning is automatically stored on release of the button.

Automatic Fine Tune

This mode is selected if the Auto/Manual button is pressed. The status for any program is stored in the EAROM. The Fine Tuning is then controlled by the output of the AFC discriminator and the system will track the incoming signal within ±25KHz. If there is no signal present, the system will search within a range of ±4MHz in 50KHz steps at a rate of 12ms per step.

Auto Sweep Mode

Operating the Auto Sweep button causes the system to sweep though all channels in steps of 250KHz at a rate of 100 steps per second. The channel number is incremented appropriately. When a station is found, the sweep stops and the Auto Fine tune mode is entered.

Band Output

4 outputs are provided.

Memory

An ER1400 non-volatile memory is used to store the channel, Fine Tune offset, and Fine Tune mode for each of the 32 programs.

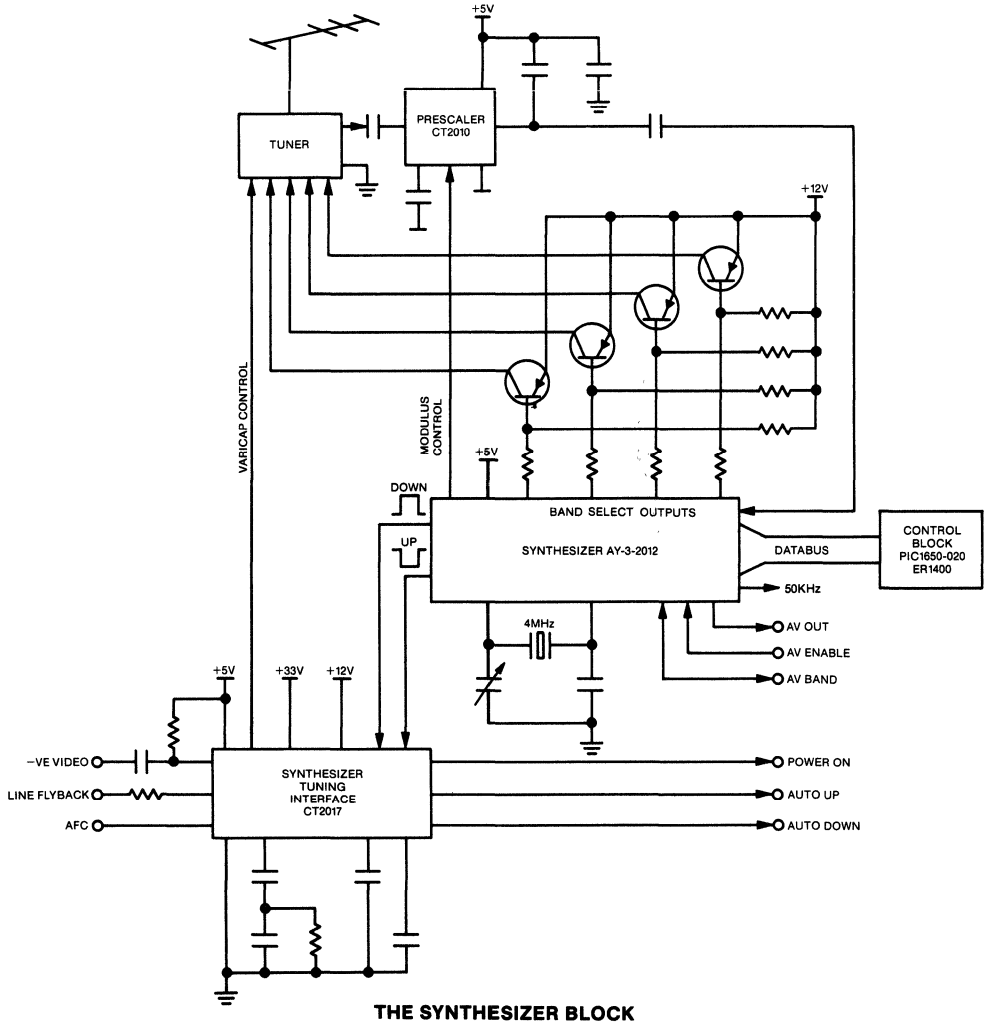
Power Up

At switch on, Program 1 is selected.

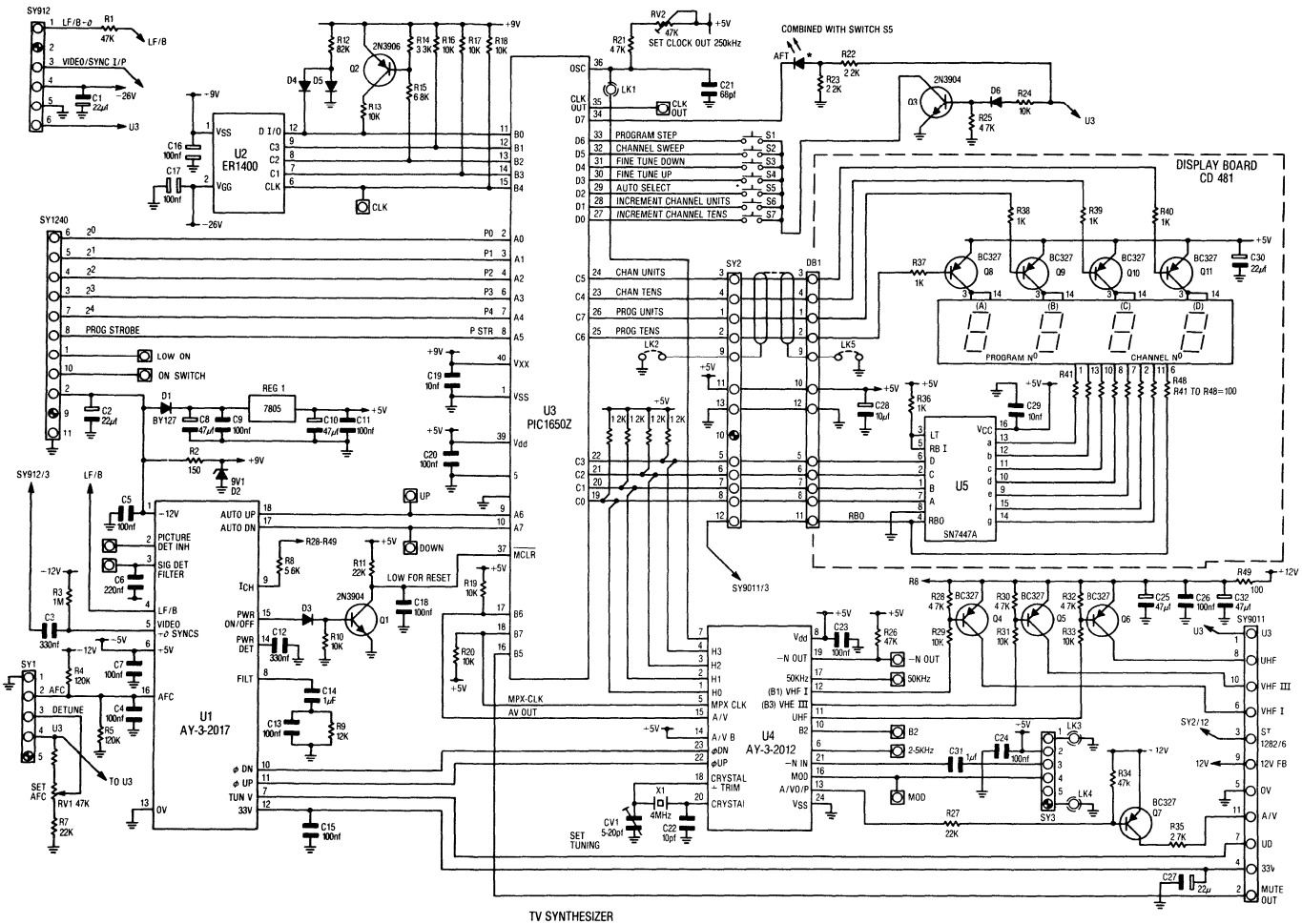
PLL Tuning System — Synthesizer Block

The three devices described form the synthesizer block of the ECONOMEGA IV system, a complete family of integrated circuits for frequency synthesis in television receivers. The Phase Locked Loop is controlled via the Data Bus by a Control Block, which consists of a PIC1650 microcomputer and an ER1400 non-volatile memory.

The CT2010 and CT2017 are manufactured by Plessey Semiconductors and data is included for information only.



THE SYNTHESIZER BLOCK



TV SYNTHESIZER

TUNING

Economega IV PLL Synthesizer Divider

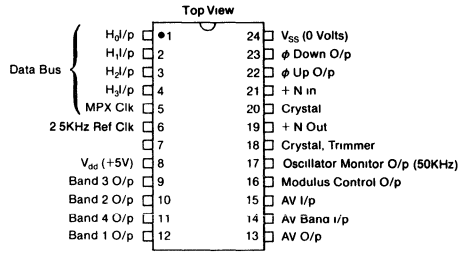
FEATURES

- 50KHz Tuning Resolution, Range Approximately 80 to 1000MHz
- Fine Tuning Range; −3.95 to +4.00MHz in 50KHz Steps
- 4MHz Crystal Oscillator Reference

DESCRIPTION

The AY-3-2012 forms part of the Economega IV phase locked loop TV tuning system. The chip is a synthesizer divider circuit fabricated in N channel MOS. Functions include a programable divider, reference oscillator and divider, phase/frequency comparator, prescaler modulus controller, and a band decoder. Tuning data is shifted into the chip under control of a PIC1650A microprocessor.

PIN CONFIGURATIONS
24 PIN DUAL IN LINE



Pin Functions

Pin Number	Name	Function
1-4	H_0-H_3 Inputs	4 Bit data highway H_0 is LSB. 4KΩ (nom) pull up to +5V
5	MPX Clock Input	Highway timing input
6	Reference Clock Output	2.5KHz output derived from 4MHz clock
7	—	
8	V_{DD}	+5V (nom) Supply
9	Band 3 Output	Open drain band output, on when Band 3 is selected. Select by Code 01
10	Band 2 Output	Open drain band output, on when Band 2 is selected. Select by Code 11
11	Band 4 Output	Open drain band output, on when Band 4 selected. Select by Code 10
12	Band 1 Output	Open drain band output, on when Band 1 is selected. Select by Code 00
13	AV Output	Open drain output, on when AV Band input and AV input are both high
14	AV Band Input	Input from band switch to allow AV mode to be selected
15	AV Input	Input from program decoder to allow AV mode to be selected
16	Modulus Control Output	Output to CT2010 prescaler to control the division ratio
17	Oscillator Monitor Output	50KHz output used to set the oscillator frequency
18	Crystal Trimmer	Oscillator input pin
19	÷N Out	Programable divider output used for test purposes
20	Crystal	Oscillator output pin
21	÷N In	Input from prescaler to programable divider
22	φ UP	Output to charge pump to raise oscillator frequency
23	φ DOWN	Output to charge pump to lower oscillator frequency
24	V_{SS} (0V)	Connect to zero volts

SYSTEM DESCRIPTION

The AY-3-2012 contains six main sections:

1. A section to recognize the Tune code (hexadecimal 1D) or Fine Tune code (hexadecimal 1E) on the data highway H_3 to H_0 and then latch the following relevant tuning information.
2. A 10 bit programable divider synchronously loaded with Tune data and counted down to part of the Fine Tune data. The amplifier on the clock input to the divider enables operation with a small swing from the output of the prescaler (CT2010). The small prescaler output keeps radiation and, hence, interference to a low level.
3. A fine tuning system which generates pulses to control the modulus of the prescaler enabling 50KHz shifts in synthesized frequency.
4. A crystal oscillator circuit (for 4MHz crystal) and fixed ÷1600 divider to give the 2.5KHz comparison or reference frequency and the fine tuning timing.
5. A phase/frequency comparator for the programable divider and fixed divider outputs. Comparison frequency 2.5KHz.
6. Logic for band decoding and for video time, constant switching for audio/visual (AV) mode.

Tune Operation Highway Information Order

		H3	H2	H1	H0	
TUNE CODE	C1	0	0	0	1	Control code
	C2	1	1	0	1	to synthesizer
DATA	D1	0	0	0	0	
	D2	0	0	0	0	Unused time slots
	D3	0	0	0	0	
	D4	B1	B0	Q9	Q8	
	D5	Q7	Q6	Q5	Q4	Band Frequency
	D6	Q3	Q2	Q1	Q0	and Offset
	D7	0	0	0	R4	
	D8	R3	R2	R1	R0	
FINISH CODE		X	X	X	X	

An '0' refers to an input low level and a '1' refers to an input High level.

Fine Tune Operation

		H3	H2	H1	H0	
FINE TUNE	C1	0	0	0	1	Control Code
CODE	C2	1	1	1	0	
DATA	D1	F7	F6	F5	F4	Fine Tune
	D2	F3	F2	F1	F0	Number
FINISH CODE		X	X	X	X	

Four binary numbers define the synthesized frequency of the loop:

1. Q; a 10 bit number (Q_{9-0}) loaded into the programable divider. This sets the synthesized frequency to the nearest 1MHz.
2. R; a 5 bit number (R_{4-0}) controlling the number of Fine Tune modulus control pulses. Zero to 19 steps of 50KHz each reduce the synthesized frequency by up to 950KHz. Combining Q and R the frequency is set to a resolution of 50KHz.
3. F; an 8 bit number (F_{7-0}) the four least significant bits of which provide 0 to 19 steps of 50KHz each, similar to Fine Tune. The three most significant bits operating on the programable divider. Combining the effect of these two provides fine tuning of −3.95MHz to +4.00MHz around the channel center.
4. B; a 2 bit number (B_{1-0}) selecting one of 4 bands.

TUNING RANGE

Combining the Fine Tune range with the programable divider range allows tuning of the local oscillator, for all television broadcast channels in Bands I, II, IV and V, to within 25KHz of channel center. In practice, all television channels are integer multiples of 50KHz and so may be received exactly apart from any crystal frequency error. This frequency error can be trimmed out.

The Fine Tuning system gives a range of −3.95 to +4.00MHz around the channel frequency.

BAND AND AV LOGIC

Four open drain band outputs are provided for driving external PNP band switch transistors.

If AV Band and AV IN are both high then AV OUT will go low: this can be used to change the time constant of the video synchronizing circuit to suit domestic video recorders. The AV Band pin would be connected to the appropriate band switch transistor.

PHASE COMPARATOR

Outputs ϕ UP and ϕ DOWN are generated by the phase comparator from the programable divider output and from the reference clock to give pulses whose length depends on the time difference between the rising edges of these signals. If Reference clock rises first the pulse will occur on ϕ DOWN. These phase comparator outputs control the loop integrator.

During the time used to demultiplex new tuning data, both outputs of the phase comparator are blocked in order to prevent erroneous ramping when changing from one channel to another. This could occur for channels close in frequency but having very different values in the more significant bits, which are latched first. As an example, consider the change from Q = 10 0000 0000 to 01 1111 1111, a shift of 1MHz, but the value will momentarily be 01 0000 0000 and 01 1111 0000 before settling to the correct value. This represents spurious shifts of 256 and 16MHz.

REFERENCE GENERATION

The crystal oscillator is based on the well known Pierce circuit providing a sine wave output of sufficient purity to avoid picture patterning from radiation.

The circuit is chosen to prevent overtone oscillation with a 4MHz series resonant crystal, and may be driven externally, if preferred.

The oscillator output drives a fixed ÷1600 to provide the 2.5KHz reference or comparison frequency. By decoding various states of the reference divider, the timing signals needed for the Fine Tuning and Fine Offset system are produced.

To aid accurate setting of the crystal trimmer capacitor, a 50KHz output is provided.

POWER ON

After power is applied to the chip, 16 Multiplex Clocks must be transferred to initialize the data decoder. Tune and Fine Tune codes may then be transferred.

SIMPLIFIED TIMING DIAGRAMS

NOTE: Control Codes C1, C2 are latched (↑) on the rising edge of Multiplex Clock, Data D0...on the following edge

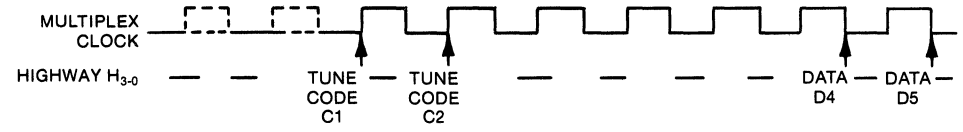


Fig. 1 HIGHWAY TIMING FOR TUNE

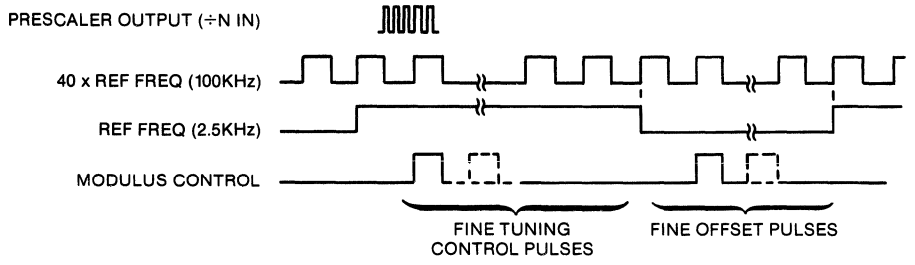


Fig. 2 FINE TUNING

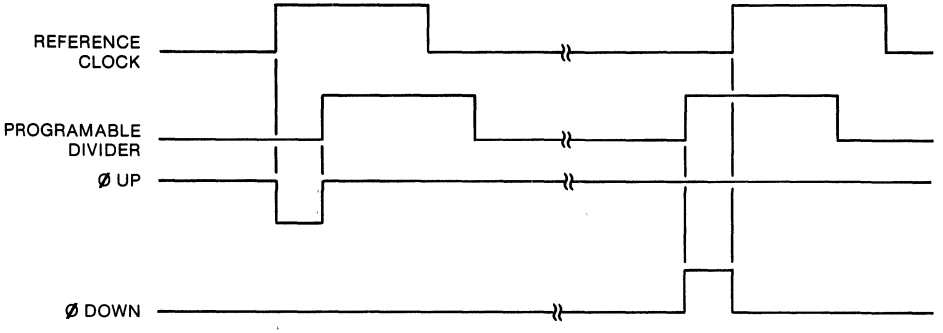


Fig. 3 PHASE DETECTOR OUTPUTS

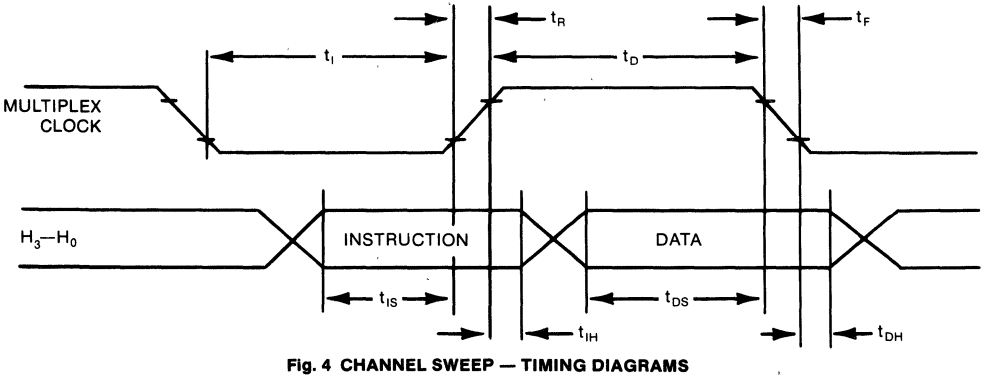


Fig. 4 CHANNEL SWEEP — TIMING DIAGRAMS

TUNING

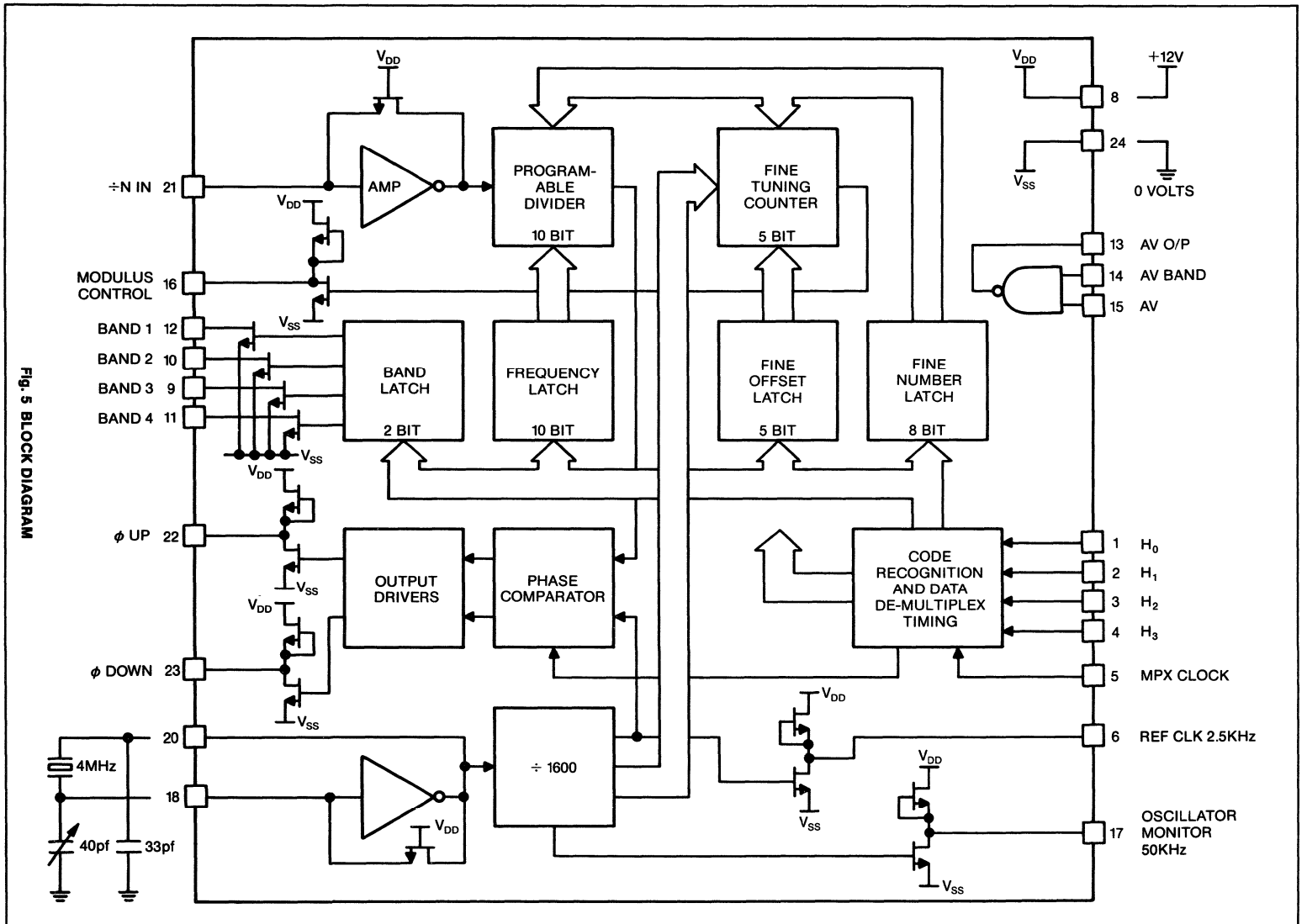


Fig. 5 BLOCK DIAGRAM

TUNING

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin (except Band and AV Outputs) with Respect to V_{SS} pin ..... −0.3V to +7V
Voltage on Band and AV Outputs with Respect to V_{SS} pin ..... −0.3V to +14V
Storage Temperature Range ..... −55° to +125°C
Ambient Operating Temperature Range ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage to these devices. This is a stress rating only and functional operation of these devices at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated):
$V_{SS} = 0$ V
$V_{DD} = +5V \pm 10\%$
$T_A = 0°C$ to $+70°C$
Nominal Reference Clock frequency = 4MHz

Characteristics	Sym	Min	Typ	Max	Units	Conditions
÷Input (21)						
Level	—	200	—	—	mV_{PP}	AC coupled Sine Wave
Capacitance	—	—	—	10	pf	
Frequency	F_{IN}	0.1	—	2.8	MHz	
H_0 to H_3 Data Inputs (1 to 4)						
Low Level	V_{IL}	—	—	0.8	V	
High Level	V_{IH}	$V_{DD}-1$	—	—	V	
Pull Up Resistance	—	2	—	6	KΩ	Note 1
Capacitance	—	—	—	10	pf	
Multiplex Clock Input (5)	MPX					
Low Level	V_{IL}	—	—	0.8	V	
High Level	V_{IH}	$V_{DD}-1$	—	—	V	
Leakage	—	—	—	10	μA	$V_{IN} = V_{DD}$
Capacitance	—	—	—	10	pf	
Frequency	—	DC	—	500	KHz	
Rise Time/Fall Time	t_R, t_F	—	—	200	ns	
AV Inputs (14 & 15)						
Low Level	V_{IL}	—	—	0.8	V	
High Level	V_{IH}	$V_{DD}-1$	—	—	V	
Leakage	—	—	—	10	μA	$V_{IN} = V_{DD}$
Capacitance	—	—	—	10	pf	
4MHz Clock Input (18) (if driven externally)						
Low Level	V_{IL}	—	—	0.8	V	
High Level	V_{IH}	$V_{DD}-1$	—	—	V	
Input Current:						
Low level source	I_{IL}	—	—	100	μA	$V_{IN} = 0.8V$ Note 2
High level sink	I_{IH}	—	—	100	μA	$V_{IN} = V_{DD}-1V$
Band & AV Outputs (9 to 13)						
Low Level	V_{OL}	—	—	5	V	$I_{OL} = 1mA$ sink
Off Leakage	—	—	—	10	μA	$V_{OUT} = 13.2V$
Reference Clock Output (6)						
Low Level	V_{OL}	—	—	0.4	V	$I_{OL} = 2mA$ sink
High Level	V_{OH}	$V_{DD}-0.5$	—	—	V	$I_{OH} = 0.5mA$ source
Modulus Control Output (16)						
Low Level	—	—	—	0.4	V	$I_{OL} = 0.3mA$ sink
High Level	—	$V_{DD}-0.5$	—	—	V	$I_{OH} = 0.1mA$ source
ϕ UP, ϕ DOWN and Oscillator Monitor Outputs (22, 23 & 17)						
Low Level	—	—	—	0.4	V	$I_{OL} = 0.8mA$ sink
High Level	—	$V_{DD}-0.5$	—	—	V	$I_{OH} = 0.1mA$ source
Supply current	I_{DD}	—	—	45	mA	Outputs/Inputs unloaded
Data to Clock timings (See Fig. 1)						
Data/Instruction time	t_D, t_I	1	—	—	μs	
Data/Instruction to Clock Set Up Time	t_{DS}, t_{IS}	400	—	—	ns	
Data Instruction to Clock Hold Time	t_{DH}, t_{IH}	100	—	—	ns	

NOTE:
1. Pull ups are configured with diffused resistors.
2. Current from the device is defined as source current, current into the device is sink current.

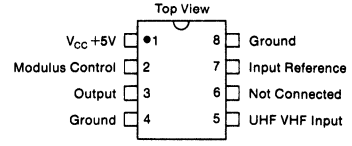
TUNING

1 GHz ÷ 380/400 Prescaler

FEATURES

- On Chip Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Low Output Radiation
- Single ECL Output
- 5V Logic Level Control Input
- Control Independent of Distortion and Delay

PIN CONFIGURATION



DESCRIPTION

The CT2010 is a 380/400 two modulus divider which will operate at frequencies between 80MHz and 1GHz. The device is the prescaler used in General Instrument Economega IV Tuning System.

The input is terminated by a nominal 50 ohms and should be AC coupled to the signal source. The reference pin should be AC decoupled. The decoupling should be effective over the full operating frequency range.

The divider contains a fixed divide by 20 followed by a divide by 19/20. The divide by 19/20 divides by 20 when no control pulses are applied to the control input. The divide by 19/20 will divide by 19 once for every positive going edge applied to the control pin. The control input edge is latched and synchronized so that the following output cycle, commencing with a negative edge, is produced by 380 input cycles to the whole divider stage, rather than 400. This means that the device is highly tolerant of delay in the control loop and distortion of the control waveform.

To ensure that there is an output cycle produced by 380 input cycles for every control pulse, the rate of control pulses should not exceed half the output frequency. (See timing diagrams).

The output source impedance is nominally 100 ohms. The output swing is nominally 300mV and swings down from the positive supply.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Supply Voltage, V_{CC} ..... +7V
UHF Input Voltage ..... 2.5V p-p
Storage Temperature ..... −55° to +125° C
Operating Ambient Temperature..... −10° C to +65° C

Standard Conditions (unless otherwise stated):

V_{CC} = 5V, T_{AMB} = 25° C

* Exceeding these ratings could cause permanent damage to these devices. This is a stress rating only and functional operation of these devicec at these conditions is not implied—operating ranges are specified in Standard Conditions Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristics		Pin	Min	Typ	Max	Units	Conditions
Operating Voltage Range		1	4.5	—	5.5	V	
Supply Current		1	—	90	110	mA	
Input Voltage, V_{IN}	80MHz	8, 6	17.5	—	200	mV	rms, sine wave 50Ω
	300MHz	8, 6	17.5	—	200	mV	rms, sine wave 50Ω
	500MHz	8, 6	17.5	—	200	mV	rms, sine wave 50Ω
	700MHz	8, 6	17.5	—	200	mV	rms, sine wave 50Ω
	1000MHz	8, 6	17.5	—	200	mV	rms, sine wave 50Ω
Output Voltage Swing		3	240	300	—	mV	p-p, no load
Output Impedance		3	—	100	—	Ω	
Control Input, High		2	2/3 V_{CC}	—	—	V	
Control Input, High		—	—	—	50	μA	
Control Input, Low		—	—	—	1/3 V_{CC}	V	
Control Input, Low		—	−10	—	—	μA	
Control Input Pulse Width		—	0.2	3	—	μs	

TUNING

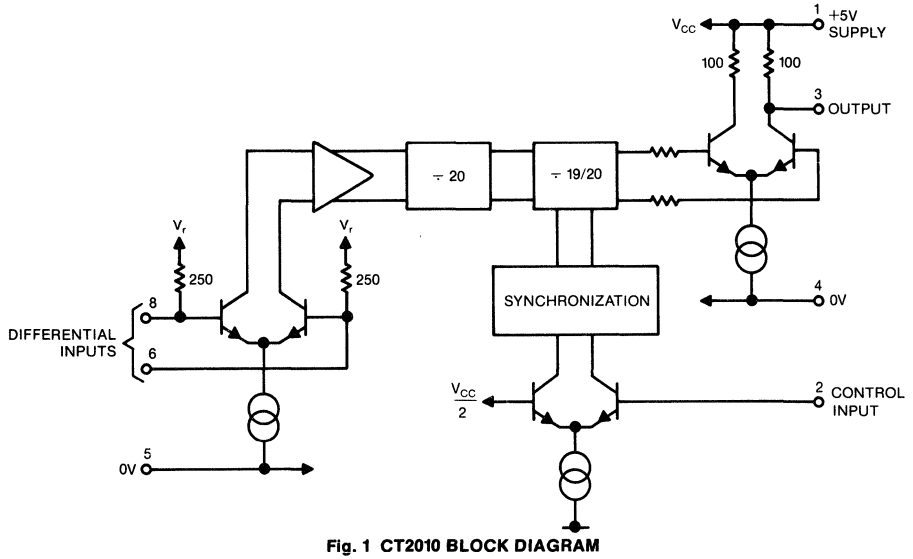


Fig. 1 CT2010 BLOCK DIAGRAM

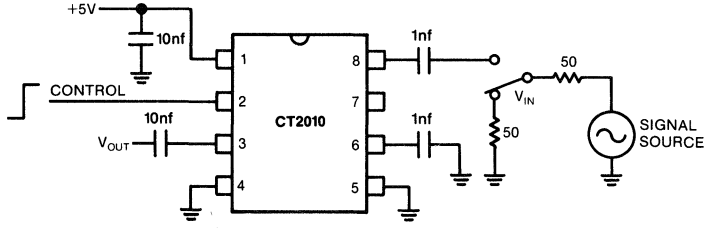


Fig. 2 TEST CONFIGURATION

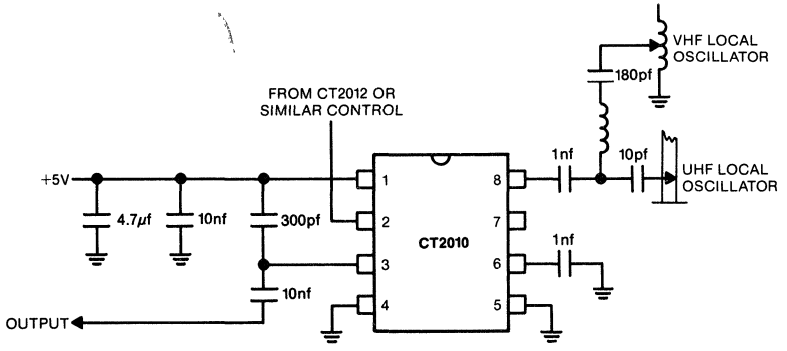
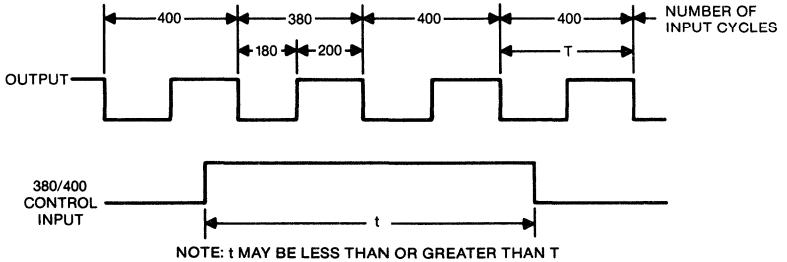


Fig. 3 TYPICAL APPLICATION WITH COMBINED INPUT



NOTE: t MAY BE LESS THAN OR GREATER THAN T

Fig. 4 TIMING DIAGRAM

TUNING

Synthesizer Tuning Interface

FEATURES

- Low Varicap Driver
- Active Filter Charge Pump
- Logic Level Control
- Signal Quality Detector
- AFC Input Option
- Auto Up, Auto Down Logic Level Tuning Correction
- Power Low Detector

DESCRIPTION

The CT2017 is designed for use in Frequency Synthesis Tuning Systems, in particular the Economega IV System.

The device contains a charge pump with a high impedance voltage follower, a signal detect circuit, a digital AFC circuit and a Power-On low detect circuit.

The charge pump is operated by two 5V logic inputs, UP (active low) and DOWN (active high). These inputs turn on a charge current and discharge current respectively. The charge pump circuit and its voltage follower operate from the +33V supply rail. The combined charge pump, external filter and voltage follower may be used as the filter and varicap driver for synthesis tuning systems.

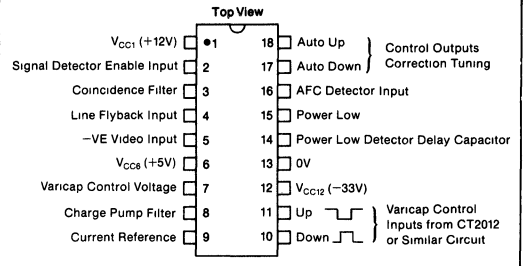
The signal detect circuit is used in tuning systems capable of automatically sweeping the received broadcast bands. The circuit examines the line synchronization pulse and line flyback pulse for coincidence. When a regular supply of adequate coincident line synchronization pulses occurs, the filter voltage falls. This indicates a received signal of a sufficient strength to produce a viewable picture.

When the signal detect filter voltage is higher than the signal detectors threshold the AUTO UP and AUTO DOWN outputs are clamped at Logic '0'. When the filter detect voltage is below the level detector's threshold the AUTO UP and AUTO DOWN outputs are enabled. The enabling of AUTO UP and AUTO DOWN may be used to indicate that a signal of adequate strength has been received and the sweep may be stopped.

Using appropriate external components, pin 5 may be used as a sync pulse separator, when fed with negative video or a positive line sync pulse input.

The signal strength recognized as adequate depends upon the signal to noise ratio at the input to pin 5. This will depend on the type of sync separation used, whether noise gating is used and the noise figure of the signal processing circuits. A digital AFC

PIN CONFIGURATION
18 PIN DUAL IN LINE



circuit, which comprises AFC level detector and correction tuning control, examines the AFC signal ('S' curve) produced by conventional television AFC circuits. The circuit produces an AUTO UP Logic '1' output when the AFC voltage is greater than the upper AFC threshold, and an AUTO DOWN Logic '1' output when the AFC voltage falls below the lower AFC threshold. Both outputs are Logic '0' when the AFC voltage is between the upper and lower thresholds.

CORRECTION TUNING

The AUTO UP and AUTO DOWN outputs may be used to adjust the correction tuning number of a synthesis tuning system and hence produce a digitally quantized AFC.

The power low detector circuit compares the +5V supply and the +12V supply against internal reference levels. When either supply falls below its relevant reference level the delay capacitor is discharged and the power low detector reset output is set to logic '1'. When the supplies exceed their relevant reference levels, the delay capacitor is charged to the threshold level, which turns on a transistor and the output is set to logic '0' after a delay.

The resulting output pulse may be used for setting the logic of the tuning synthesizer and for protecting the memory from corruption during power on and power off.

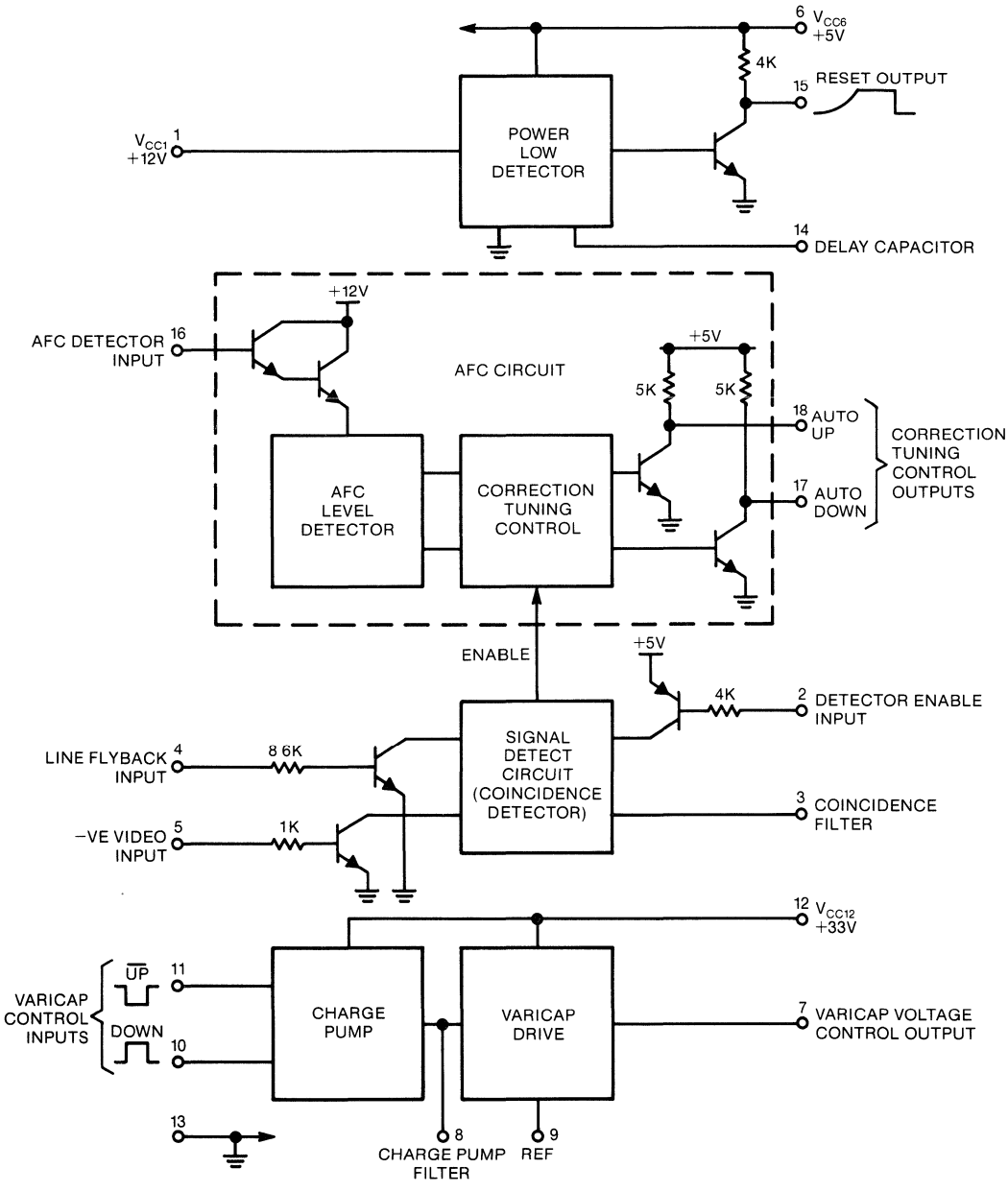


Fig. 1 CT2017 BLOCK DIAGRAM

TUNING

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

+12V Supply (V_{CC1}) ..... +20V
+5V Supply (V_{CC6}) ..... +20V
+33V Supply (V_{CC12}) ..... +40V
Operating Temperature Range ..... −10°C to +65°C
Storage Temperature Range ..... −55°C to +125°C

*Exceeding these ratings could cause permanent damage to these devices. This is a stress rating only and functional operation of these devicec at these conditions is not implied—operating ranges are specified in Standard Conditions Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise stated):

T_{amb} = 25°C, V_{CC1} = +12V, V_{CC6} = +5V, V_{CC12} = +33V
Test Circuit: Fig. 2

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Operating Voltage Range						
V_{CC1} (+12V)	1	10.8	—	13.2	V	
V_{CC6} (+5V)	6	4.5	—	5.5	V	
V_{CC12} (+33V)	12	31	—	36	V	
Supply Current						
V_{CC1} (+12V)	1	—	8	12	mA	
V_{CC6} (+5V)	6	—	12	20	mA	V_S = 0V, V_{10} = 0V, V_{11} = +5V
V_{CC12} (+33V)	12	3.3	4.5	5.5	mA	I_9 = 2mA, V_{10} = 0V, V_{11} = +5V
Varicap Control						
High Level Output Voltage	7	29.5	—	—	V	I_9 = 2mA, V_{CC12} = +33.0V
Continuous Source Current	7	—	—	1	mA	V_{CC12} = 33.0V
Low Level Output Voltage	7	0.5	—	0.9	V	
Transient Sink Currents	7	1.51	—	—	mA	I_9 = 0.1mA to 2.5mA
Filter Leakage Current	8	—	—	40	mA	V_{11} = +5V, V_{10} = 0V
$\overline{UP}$ Control Input Active	11	—	—	1	V	
$\overline{UP}$ Control Input Inactive	11	3	—	—	V	
$\overline{UP}$ Control Input Current	11	—	—	50	μA	V_{11} = +5V
DOWN Control Input Active	10	3	—	—	V	
DOWN Control Input Inactive	10	—	—	1	V	
DOWN Control Input Current	10	—	—	50	μA	V_{10} = +5V
AFC Control						
Detector High Threshold	16	7	7.5	8	V	
Detector Low Threshold	16	4.1	4.5	4.9	V	
Detector Window	16	2.8	3	3.2	V	
Input Current	16	—	—	2.5	μA	V_{16} = +12V
Correction Tuning Outputs (AUTO UP, AUTO DOWN)						
Voltage High	17, 18	4.5	—	—	V	V_{17} (high) = DOWN, V_{18} (high) = UP Current Source = 50μA
Voltage Low	17, 18	—	—	0.5	V	Both low = inactive current sink = 2mA
Line Flyback Threshold						
High	4	2	—	—	V	
Low	4	—	—	0.7	V	
Negative Video Input						
Threshold	5	—	0.7	—	V	
Sync Pulse Switching Current	5	—	—	12	μA	
Leakage Current	5	—	—	0.3	μA	V_S = −5V
Coincidence Detector						
Enable	2	4.5	—	—	V	
Inhibit	2	—	—	2	V	
Threshold	3	—	2.4	—	V	
Power on Detector						
Output Voltage	15	4.5	—	—	V	Current source = 50μA
Normal	—	—	—	0.5	V	Current sink = 2mA
Detector Threshold						
V_{CC1} (+12V)	1	9.2	9.9	10.6	V	See Fig 4
V_{CC6} (+5V)	6	3.7	4	4.3	V	See Fig 4
Delay Capacitor Charging Current	14	—	10	—	μA	
Delay Threshold	14	—	9	—	V	

TUNING

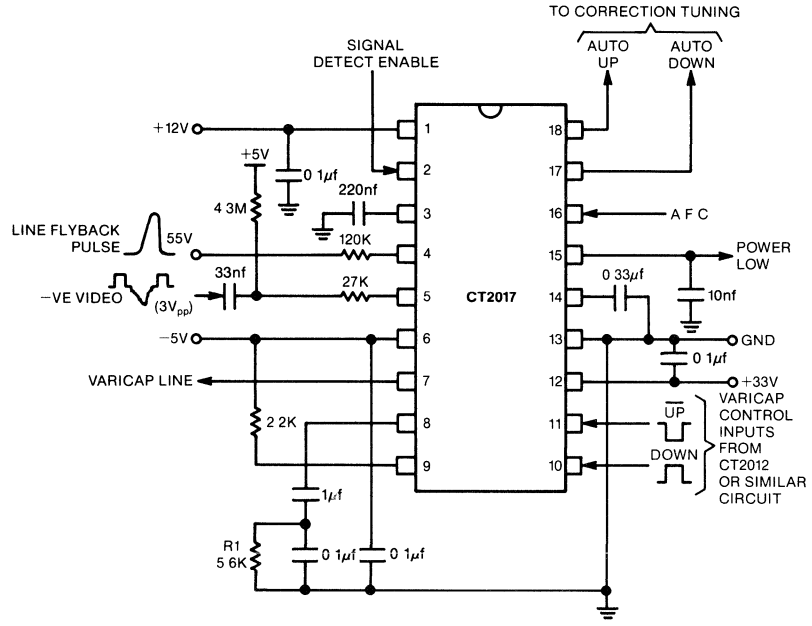
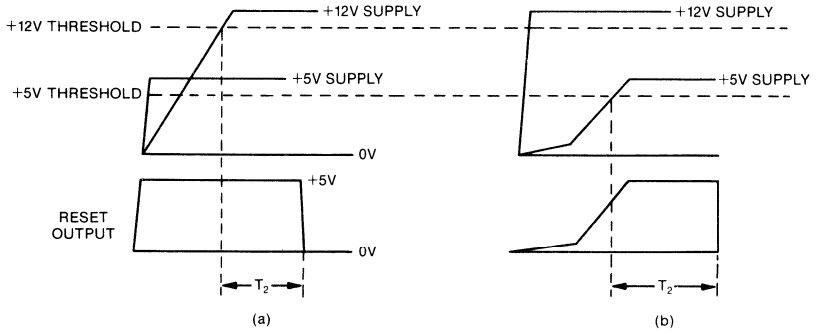


Fig. 2 TEST CONFIGURATION



NOTES:
1. T_2 period timed by delay capacitor.
2. Output is connected to +5V supply via pull-up resistor.
3. T_2 is set by value of capacitor, changing current, and output threshold voltage. Changing current is normally 10μA. Threshold voltage is normally 9V.

Fig. 3 POWER LOW DETECTOR TIMING DIAGRAM (POWER ON)

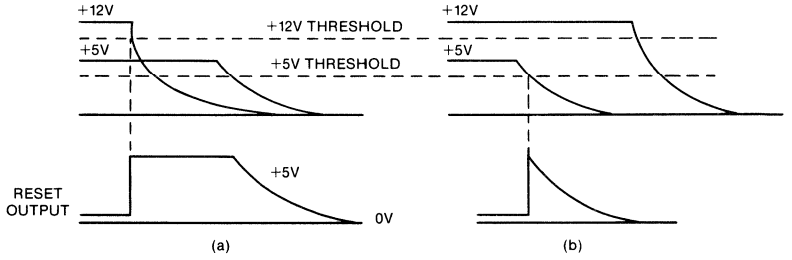


Fig. 4 POWER LOW DETECTOR TIMING DIAGRAM (POWER OFF)

TUNING

Economega IV TV PPL Tuning System Control

FEATURES

- 100 Channel Tuning Capability — Includes CCIR Standard Channels, Italian and German Cable Channels
- 32 Favorite Program Storage in Non-Volatile Memory (ER1400)
- Automatic Sweep Tuning Option (with Automatic Fine Tune)
- Fine Tune in 50KHz Steps (Manual or Automatic)
- Two Digit Channel Number Display
- Two Digit Program Number Display
- Fast Lock Up Time, 10ms (typ)
- Parallel Remote Control Input
- 38 9MHz IF
- Easily Reprogramed for Different Channels (e g U S A.), Features and Interfaces (Inquire for Alternative Versions)

DESCRIPTION

This specification describes a PIC1650-020 microcomputer which is used as a control chip in a phase locked loop television tuning system. The microcomputer interfaces with a number of subsystems which are detailed below.

1 AY-3-8475 I.R. Receiver. The PIC1650-020 accepts program numbers from the receiver thus allowing remote program selection.

2 ER1400. Electrically Alterable ROM The ER1400 is used to store Channel, Fine Tune and AFT data for each program. Information is stored and recalled by the PIC1650-020 as required.

3. CT2012 Frequency Synthesizer. The PIC1650-020 sends frequency and band data to the synthesizer. This data is ultimately used to determine the local oscillator frequency. The PIC1650-020 also controls the AVIN signal to the synthesizer chip.

4. CT2017 Tuning Interface. Signals from this chip are monitored by the PIC1650-020 when operating in CHANNEL SWEEP or AUTO MODES. The Tuning Interface chip also controls the PIC1650-020 master clear input via an external inverter.

5. User controls including SN7447A, BCD to Binary decoder/driver.
   (a) Four 7 segment displays which are used to display Program and Channel information.
   (b) One LED to indicate if AUTO mode is selected.
   (c) Seven push button switches for channel selection, local Program Selection, Fine Tuning and AUTO Mode selection.

6. The PIC1650-020 supplies a MUTE signal to mute the TV sound during Program and Channel change.

OPERATION

Program Selection (A0-A5)

32 remote programs can be entered via inputs (A0-A4) from the I.R. receiver AY-3-8475 These lines contain valid program information only when the STROBE input (A5) is low. Information on A0-A4 is in the range 0-31 representing programs 1-32 respectively.

The PIC1650-020 will tune the TV to a new program only if the STROBE is low and the program data on A0-A4 is different from the current program data.

Program numbers are used to address the ER1400 allowing the user to allocate a TV channel to each program.

The TV sound is muted for 600ms at each program change.

Changes in program number are ignored if any of the local switches are pressed.

ER1400 Interface (B0-B4)

To enable the ER1400 inputs to be pulled high to V_{XX}, PIC1650-020 pins (B0-B4) have open drain outputs with external pull up resistors as shown in Fig. 2.

The ER1400 contains 100 words of 14 bits. Two words are needed to store the 17 bits of information required for each program.

CHANNEL information for PROGRAM N is stored at ER1400 address N. The corresponding FINE TUNE NUMBER and AFT information is stored at address N +40.

Address Formats

Address	MSB	DATA	
N	XX XXXX	CT.CT.CT.CT.	CU.CU.CU.CU.
N + 40	XX XXXAFT	FT.FT.FT.FT.	FT.FT.FT.FT.

X = Not Used
CT = BCD digit for CHANNEL TENS data
CU = BCD digit for CHANNEL UNITS data
AFT = AUTO/MANUAL mode. AFT = 1 = AUTO mode
FT = FINE TUNE NUMBER

Data is written to the ER1400 when:

1. Either the CHANNEL TENS or CHANNEL UNITS switch is released.
2. Either the FINE TUNE UP or FINE TUNE DOWN switch is released.
3. AUTO switch is pressed.
4. AUTO mode is entered from CHANNEL SWEEP.

Data is read from the ER1400 when a new program is selected. The data is converted to a suitable format and then transferred to the synthesizer. If the Channel data read from the ER1400 is not a valid BCD number then the channel number is set to 00. Under these conditions it is likely that the Fine Tune data from the ER1400 will also be non-valid. No attempt is made to correct this data. It is sent to the synthesizer as read from the ER1400.

Frequency Synthesizer Interface (B6, B7, C0-C3)

AVOUT — (B6)

This output is normally low and goes high when programs 16 or 32 are selected. It is routed via the synthesizer and can be used to modify the time constant of the video synchronizing circuit of the television for use with video recorders.

Data Highway & Clock — (B7, C0-C3)

Tune information is transferred to the synthesizer on a 4 bit highway which is shared with the display decoder/driver The synthesizer ignores data on the highway unless a clock is present. Clock signals (SYN CLK) are generated by the PIC1650-020 as required. A timing diagram is shown in Fig. 3

When the power is initially switched on 16 clock pulses, with random data, are sent to initialize the synthesizer. Under normal operating conditions 11 clock pulses are required to transfer Tune data and 5 clock pulses are required to transfer Fine Tune Data.

TUNE DATA FORMAT

	H3	H2	H1	H0		
SC1	0	0	0	1	}	Control Code to
SC2	1	1	0	1	}	synthesizer
SD1	0	0	0	0		
SD2	0	0	0	0		
SD3	0	0	0	0		
SD4	B1	B0	Q9	Q8	}	Band and
SD5	Q7	Q6	Q5	Q4	}	Frequency
SD6	Q3	Q2	Q1	Q0	}	Number Data
SD7	0	0	0	R4	}	Fine Offset
SD8	R3	R2	R1	R0	}	data
SC3	X	X	X	X		Not Specified

NOTES:

1. Band Information is coded as follows:

B1	B0	
0	0	BAND 1 — VHF I
0	1	BAND 3 — VHF III
1	0	BAND 4 — UHF
1	1	BAND 2 — NOT USED

2. Q9-Q0 is a binary number representing the required tune frequency in MHz. The frequency is in the range 84MHz to 914MHz. Q9 is the most significant bit.
3. R4-R0 is a binary number in the range 0-19. This is used to modify the tune frequency in 20 steps of 50KHz. R4 is the most significant bit. An increase in the Fine Offset number means a corresponding decrease in frequency.

FINE TUNE DATA FORMAT

	H3	H2	H1	H0		
SC1	0	0	0	1	}	Control Code to
SC2	1	1	1	0	}	Synthesizer
SD1	F7	F6	F5	F4	}	FINE TUNE
SD2	F3	F2	F1	F0	}	NUMBER Data
SC3	X	X	X	X		Not Specified

NOTES:

1. F7-F0 is a binary coded modular 20 number which is used to modify the tune frequency in 160 steps of 50KHz. F7 is the most significant bit. An increase in the Fine Tune Number means a corresponding decrease in frequency.

TUNING

Tuning Interface (CT2017)

UP and DOWN (A6, A7)

These inputs are derived from an AFC circuit within the television. They perform two functions. They signal a Stop Sweep when in CHANNEL SWEEP and they control the television Fine Tuning when in AUTO mode.

Master CLear (MCLR)

The PIC1650-020 Master Clear signal is controlled via an external inverter by the POWER ON DET signal from the Tuning Interface chip. The Master Clear signal must be held low for at least 1ms after all power supplies become valid. When the Master Clear signal goes high the PIC1650-020 will tune the TV to the channel allocated to Program 1.

User Controls

Four common anode 7 segment displays are used to display Channel and Program information. Two digits are used to display channel information in the range 00 to 99. Leading zeros are not blanked. The remaining 2 digits display the selected program. Program information lies in the range 1-32. Leading zeros are blanked.

Digits are displayed in turn by enabling 1 of the 4 digit driver transistors (C4-C7) and simultaneously outputting the corresponding segment code on C0-C3. Each digit is enabled for approximately 3ms in any 12ms period.

As the segment outputs share a common highway with the synthesizer the display is blanked, by switching off all 4 digit drivers, during a data transfer to the synthesizer. This blanking is not noticeable during normal operation.

It is not possible to maintain the displays when writing to the ER1400. Displays are blanked for 80ms each time a WRITE takes place.

Seven push button switches are mounted on the front panel. Only one switch is serviced at any one time, all other switches being inhibited until the current switch is released.

The following functions are controlled by the switches:

1. Increment Channel Tens
2. Increment Channel Units
3. Fine Tune Up
4. Fine Tune Down
5. Program Step
6. Channel Sweep
7. Auto

Increment Channel TENS or UNITS (D0, D1)

These switches enable the television to be tuned to any of 100 channels in the range 00-99.

Closure of the Channel Tens switch causes the Channel Tens display to increment one step and thereafter one step every 0.5 sec, overflowing from 9 to 0, until the switch is released. At each step the appropriate TUNE data is transferred to the synthesizer and MUTE is activated for 600ms.

Closure of the Channel Units switch causes the Channel Units to increment similarly, there being no overflow to Channel Tens.

In both cases, at every step, the Fine Tune Number is set to its mid-point (128) and transferred to the synthesizer.

On release of either switch the current channel and Fine Tune Number are stored at the appropriate ER1400 address.

Fine Tune Up and Fine Tune Down (D3, D4)

Closure of a switch causes a single Fine Tune step, in the appropriate direction, to be executed. This is followed by a pause of 0.4 sec, thereafter steps occur at 50ms intervals. The pause allows single step Fine Tuning to be carried out. At each step the new Fine Tune Number is transferred to the synthesizer.

On release of the switch current Channel and Fine Tune Number are stored at the appropriate ER1400 address.

NOTE: Fine Tune Up means decrease in Fine Tune Number which gives a corresponding increase in frequency.
Fine Tune Down acts in a similar fashion.

The Fine Tune Number allows tuning of +4MHz, −3.95MHz, in 50KHz steps around the allocated channel frequency.

Program Step (D6)

Closure of the Program Step switch causes the displayed program number to increment one step and thereafter one step every 0.5 sec, overflowing from 32 to 1, until the switch is released. At each step the channel display is updated and the appropriate TUNE information is sent to the synthesizer. The MUTE signal is activated for 600ms at each step.

Channel Sweep (D5)

The Channel Sweep enables the user to sweep through each channel in turn (in order of increasing Channel Number, with roll over from 99 to 00) stopping when a valid stop signal, as indicated by the UP and DOWN inputs, is detected. The sweep is implemented by decrementing the Fine Tune Number in steps of 5, at 12ms intervals, which is equivalent to increasing the frequency in steps of 250KHz.

Band 1 and Band 3 channel widths are 7MHz and are swept −3.45MHz, +3.3MHz around the allocated channel frequency. UHF band channel widths are 8MHz and are swept −3.95MHz, +3.8MHz around the allocated channel frequency

When the switch is initially closed the sweep starts from the bottom of the next channel. A pause of 250ms is initiated before continuing. On succeeding channel boundaries there is a 12ms pause unless a bank change is involved in which case there is a 0.5 sec pause.

For normal operation the sweep switch should be closed momentarily and then released. If the switch is held closed and a STOP is detected, AUTO mode is entered where the appropriate Channel and Fine Tune data is stored in the ER1400. At this point because the sweep is closed, the sweep is restarted from the bottom of the next channel.

The sweep mode can be terminated at any time by pressing any of the push buttons (other than CHANNEL SWEEP) on the front panel or by selecting a new program. A STOP signal, indicating a TV station has been found, is recognized by UP going high then low followed by DOWN going high (Fig. 4). When a TV station is found the PIC1650-020 enters the AUTO mode.

Auto (D2)

Auto mode is entered either by pressing the AUTO push button or from channel sweep when a STOP is detected. Current Channel information is stored in the appropriate ER1400 address.

The FINE TUNE number stored is the current FINE TUNE number plus 20 FINE TUNE steps. This is equivalent to off-setting the frequency by −1MHz to give a symmetrical AFC capture range. Note: The above −1MHz offset is a maximum value. If by off-setting by −1MHz a channel boundary is crossed the offset is reduced to stay within the current channel.

The AFT bit is stored as a 1 to indicate Auto mode is selected. To exit from the 'Auto' mode and cancel the AFT bit, either the Fine Tune Up, Fine Tune Down, Channel Tens or Channel Units switch must be operated.

In Auto mode if UP is high the Fine Tune number is decremented by one every 12ms until UP goes low. Similarly if DOWN is high the Fine Tune number is incremented by one until it goes low. The maximum tuning range is −3.95MHz, +4MHz around the allocated channel frequency. No roll over occurs when these limits are reached, i.e. the system will only tune down from the +4MHz limit and up from the −3.95MHz limit.

Auto Fine Tune Indicator (D7)

This is a LED which is ON when the system is operating in the AUTO mode. The state of the LED is determined by the AFT bit from the ER1400.

Mute — (B5)

The Mute signal is normally high but goes active (low) for 600ms each time TUNE data is transferred to the synthesizer i.e. during a channel or program change or when the power is initially switched on. In the Channel sweep mode the MUTE is active continuously from the start of sweep until 600ms after a STOP is detected. The Mute does not go active if only Fine Tune information is transferred to the synthesizer.

The Mute output serves to mute the sound of the television when disturbances are made to the tuning.

OSC

This is an RC network which provides the basic oscillator frequency for the PIC1650-020. A 47K potentiometer is provided to allow accurate setting of the frequency to 1.0MHz.

Channel-Frequency Conversion

The channel data read from the ER1400 is converted by the PIC1650-020 into Frequency, Band and Offset information. The table below lists the Frequency Number (Q), Band (B) and Offset (R) allocated to each of the 100 channels.

For example the Tune data for channel 21 is as follows:—

Q = 514
B = 2
R = 17

This information is transferred to the synthesizer in the Tune Data format specified earlier. If the Fine Tune data is set to 128 and transferred to the synthesizer then the local oscillator will be tuned to a frequency of 510.15MHz.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Voltage on any Pin with Respect to V_{SS} ..... −0.3V to +12V

Standard Conditions (unless otherwise noted):

Operating Temperature (Ambient) T_A = 0°C to +70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	4.5	—	7	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10	V	
Supply Current	I_{DD}	—	30	55	mA	No Load
Output Buffer Supply Current	I_{XX}	—	1	5	mA	No Load (see Note 1)
All Inputs						
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
I/O Ports With Internal Pull-up						
Input High Voltage	V_{IH}	2.4	—	V_{DD}	V	
$\overline{MCLR}$, $\overline{RTCC}$ & OSC						
Input High Voltage	V_{IH}	V_{DD} −1	—	V_{DD}	V	
All Outputs Except CLK OUT						
Output Low Voltage	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA (see Note 2, 3, 4) V_{XX} = 4.5V
	—	—	—	0.90	V	I_{OL} = 5mA (see Note 2, 3, 4) V_{XX} = 4.5V
	—	—	0.50	—	V	I_{OL} = 5mA (see Note 2, 3, 4) V_{XX} = 9V
	—	—	0.9	—	V	I_{OL} = 10mA (see Note 2, 3, 4) V_{XX} = 9V
CLK OUT						
Output Low Voltage	V_{OL}	—	—	0.45	V	V_{XX} = 9.0V I_{OL} = 1.6mA (see Note 2, 3, 4)
All Outputs With Internal Pull Up						
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = 100μA (see Note 2, 3, 4)
All I/O Ports With Internal Pull Up						
Input Low Current	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V (see Note 4)
Input High Current	I_{IH}	−0.1	−0.4	—	mA	V_{IH} = 2.4V (see Note 4)
$\overline{MCLR}$, $\overline{RTCC}$						
Input Leakage Current	I_{LC}	−10	—	10	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$ (see Note 4)
I/O Ports With Open Drain Outputs						
Input High Voltage	V_{IH}	2.4	—	V_{XX}	V	
Input Leakage Current	I_{CL}	−10	—	10	μA	$V_{SS} \leq V_{IN} \leq V_{XX}$ (see Note 4)

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
OSC						
Oscillator Frequency	f	0.2	—	1	MHz	
Instruction Cycle Time	t_{CY}	4	—	20	μs	(see Note 6)
CLK OUT & I/O Ports with Internal Pull Up						
Rise Time	t_R	—	—	200	ns	1 TTL Load + 100pf
Fall Time	t_F	—	—	200	ns	1 TTL Load + 100pf
I/O Ports with Internal Pull Up						
Output Mode						
CLK OUT to Data Valid	t_{PD}	0	500	.800	ns	
Input Mode						
Data Set Up Time	t_S	0	—	¼ t_{CY}	ns	
Data Hold Time	t_h	0	—	25ns	ns	
$\overline{RTCC}$ Input						
Period	t_{RT}	t_{CY}	—	—	μs	
High Pulse Width	t_{RT1}	½ t_{CY}	—	—	μs	(see Note 7)
Low Pulse Width	t_{RTH}	½ t_{CY}	—	—	μs	

NOTES:
1. Maximum I_{XX} occurs when all I/O ports are high.
2. Total I_{OL} for all outputs (I/O ports + CLK OUT) must not exceed 175mA.
3. V_{XX} supply drives I/O ports. The V_{DD} supply drives CLK OUT.
4. Positive Current indicates current flow into the device. Negative Current indicates current flow out of the device.
5. Oscillator circuit as shown in Fig. 1.
6. Both the instruction Cycle Time and CLK OUT period are equal to four times the oscillator frequency i.e. t_{CY} = 4/f secs.
7. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RTCC}$ input, CLK OUT may be directly tied to the $\overline{RTCC}$ without any loss of counts.

CHANNEL FREQUENCY ALLOCATIONS

Channel Number	Channel Name	L.O. Freq MHz	Band	Q (Freq) Number	R (Offset) Number	Band AY-3-2012 Output	Band B	Channel Width
00	1	80.15	1	84	17	BAND 1	0	7MHz
01	1	80.15	1	84				
02	2	87.15	VHFI	91				
03	3	94.15		98				
04	4	101.15	CCIR	105				
05	5	214.15		218		BAND 3	1	
06	6	221.15		225				
07	7	228.15		232				
08	8	235.15	VHF III	239				
09	9	242.15	CCIR	246				
10	10	249.15		253				
11	11	256.15		260				
12	12	263.15		267				
13	A1	108.15		112		BAND 1	0	
14	B1	115.15		119				
15	C1	122.15		126				
16	D1	129 15		133				
17	E1	136.15		140				
18	F1	85.15		89				
19	G1	98.15		102				
20	H1	132.15		136				
21	21	510.15		514		UHF	2	8MHz
22	22	518 15		522				
23	23	526.15		530				
24	24	534.15		538				
25	25	542 15		546				
26	26	550.15		554				
27	27	558.15		562				
28	28	566.15	UHF	570				
29	29	574 15	CCIR	578				
30	30	582 15		586				
31	31	590 15		594				
32	32	598.15		602				
33	33	606 15		610				
34	34	614.15		618				
35	35	622.15		626				
36	36	630.15		634				
37	37	638.15		642				
38	38	646 15		650				
39	39	654.15		658				
40	40	662.15		666				
41	41	670.15		674				
42	42	678.15		682				
43	43	686.15		690				
44	44	694.15		698				
45	45	702.15		706				
46	46	710.15		714				
47	47	718.15		722				
48	48	726.15		730				
49	49	734.15	UHF	738				
50	50	742.15	CCIR	746				
51	51	750.15		754				
52	52	758.15		762				
53	53	766.15		770				
54	54	774.15		778				
55	55	782.15		786				
56	56	790.15		794				
57	57	798.15		802				
58	58	806.15		810				
59	59	814.15		818	17	UHF	2	8MHz

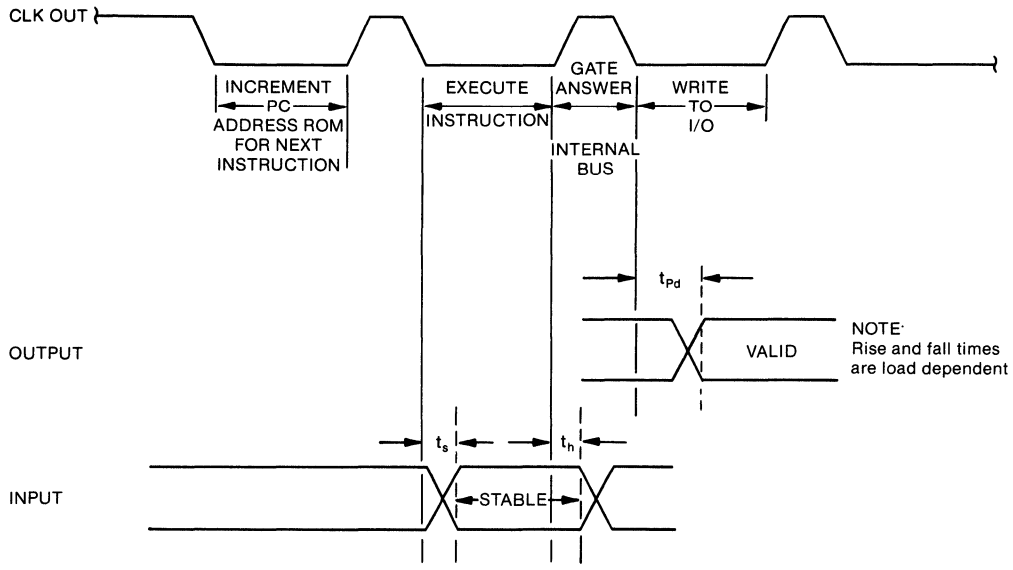
TUNING

CHANNEL FREQUENCY ALLOCATIONS

Channel Number	Channel Name	L.O. Freq MHz	Band	Q (Freq) Number	R (Offset) Number	Band AY-3-2012 Output	Band B	Channel Width
60	60	822.15		826	17	UHF	2	8MHz
61	61	830.15		834				
62	62	838.15		842				
63	63	846.15		850				
64	64	854.15		858				
65	65	862.15		866				
66	66	870.15		874				
67	67	878.15		882				
68	68	886.15		890				
69	69	894.15		898				
70	70	902.15	UHF	906				
71	71	910.15	CCIR	914	17		2	
72	A	92.65		96	7	BAND 1	0	7MHz
73	B	101.15		105	17		0	
74	C	121.15		125	17		0	
75	D	214.15	ITALIAN	218	17	BAND 3	1	
76	E	222.65		226	7			
77	F	231.15		235	17			
78	G	240.15		244				
79	H	249.15		253				
80	S1	144.15		148				
81	S2	151.15		155				
82	S3	158.15		162				
83	S4	165.15		169				
84	S5	172.15		176				
85	S6	179.15		183				
86	S7	186.15		190				
87	S8	193.15		197				
88	S9	200.15		204				
89	S10	207.15	GERMAN	211				
90	S11	270.15	CABLE	274				
91	S12	277.15		281				
92	S13	284.51		288				
93	S14	291,15		295				
94	S15	298.15		302				
95	S16	305.15		309				
96	S17	312.15		316				
97	S18	319.15		323				
98	S19	326.15		330				
99	S20	333.15		337	17	BAND 3	1	7MHz

TUNING

I/O TIMING



TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE

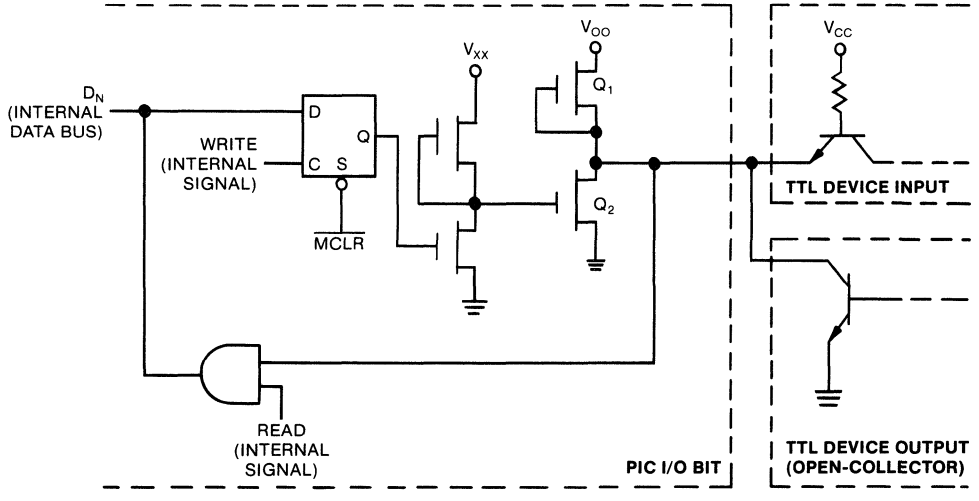
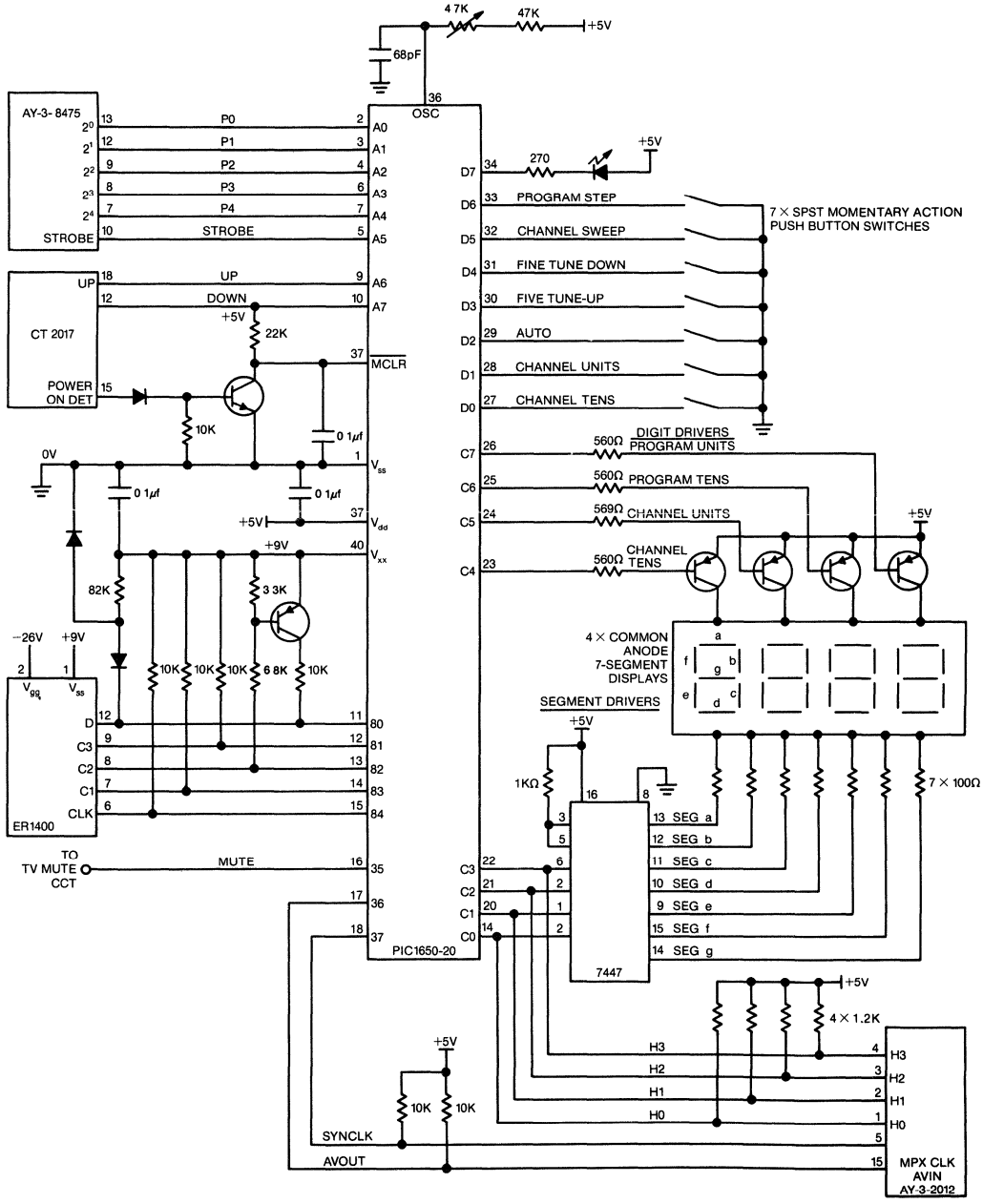


Fig. 1 I/O TIMING AND INTERFACE

TUNING

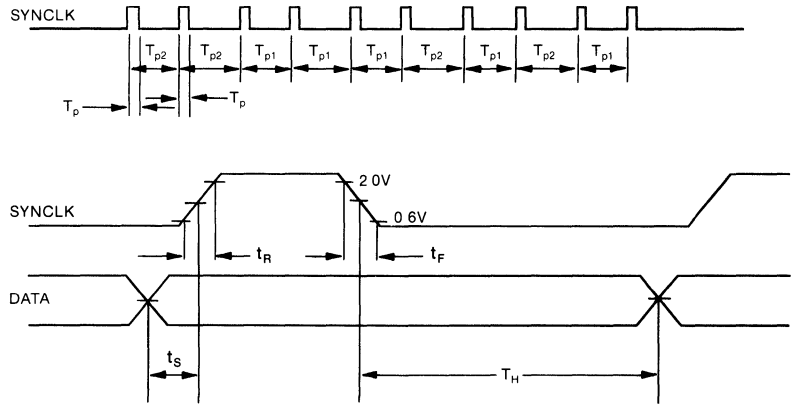


NOTES:

1. I/O's B0, B1, B2, B3, B4, B5, C0, C1, C2, C3 & D7 have open drain outputs.
2. Unless otherwise noted:
   a. Diodes are IN914
   b. NPN Transistors are 2N3904
   c. PNP Transistors are BC327

Fig. 2 CIRCUIT DIAGRAM

TUNING

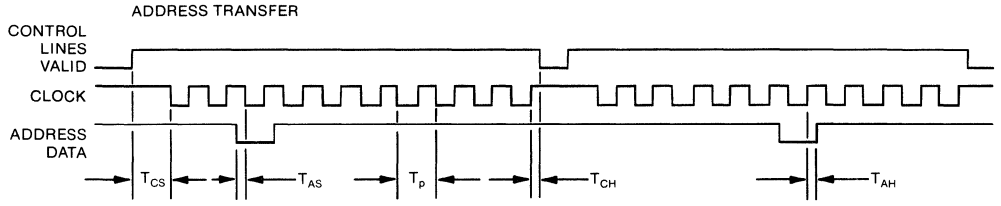


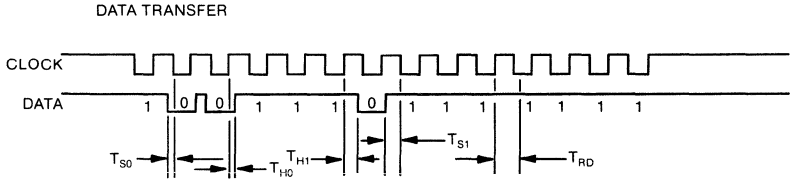
Parameter		Notes
Clock Pulse Width	T_p	4μs
Clock Period	T_{p1}	56μs
	T_{p2}	44μs
Data Set Up Time	t_s	4μs
Data Hold Time	T_m	>36μs
Clock or Data Rise Time	t_r	200ns
Clock or Data Fall Time	t_f	200ns

NOTES.
1. Rise and Fall times are maximum values. Other times are typical values with a tolerance of ± 250ns.
2. Times other than rise or fall times are based on a PIC1650 clock frequency of 1MHz.
3. Logic Levels: '0' <0.5V; '1' > 2.0V.

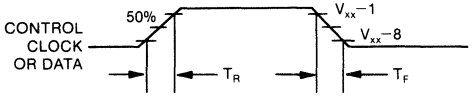
TUNING

Fig. 3 PIC1650 — TIMING DIAGRAMS





Parameter		Value
Clock Period	T_P	72μs
Clock Duty Cycle		50%
Control Set Up Time	T_{CS}	52μs
Control Hold Time	T_{CH}	4μs
Address Set Up Time	T_{AS}	8μs
Address Hold Time	T_{AH}	4μs
Write Data Set Up Time		
Logic 0	T_{S0}	16μs
Logic 1	T_{S1}	32μs
Write Data Hold Time		
Logic 0	T_{H0}	4μs
Logic 1	T_{H1}	20μs
Read Data sample Time	T_{RD}	36-40μs
Control or Clock Rise Time	t_R	1μs
Control or Clock Fall Time	t_F	1μs
Data Rise Time	T_R	8μs
Data Fall Time	T_F	4μs



NOTES:
1. Rise and fall times are maximum values. Other times are typical values with a tolerance of ±250ms. Times are measured to 50% values.
2. Times other than rise and fall times are based on a PIC1650 clock frequency of 1MHz.
3. Address transfer is shown for ER1400 address of 74.
4. ER1400 Erase/Write cycles—continuous clock pulses for 18.5ms.
5. Logic Levels: '0' $<(V_{XX}-8)$ Volts; '1' $>(V_{XX}-1)$ Volts.

Fig. 4 PIC1650/ER1400 TIMING DIAGRAMS

TUNING

GENERAL INSTRUMENT

Synthesizer/Counter

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
FREQUENCY SYNTHESIZER/ COUNTER	Provides a time base for frequency synthesizer counting.	AY-5-8105	10-44

Frequency Synthesizer/Counter

FEATURES

- Three Display Ranges: MW 9,999KHz, FM 399.99MHz, SW 39,999KHz
- AM IF Offset: Five User Programable Frequencies (0, 455, 459, 460, 468KHz)
- FM IF Offset: Five User Programable Frequencies (10.64, 10.67, 10.70, 10.73, 10.76MHz)
- High Voltage Capability for Direct Drive of Fluorescent Displays
- Together with PIC1650A Controller, Forms the Economega III E and F Tuning Systems

DESCRIPTION

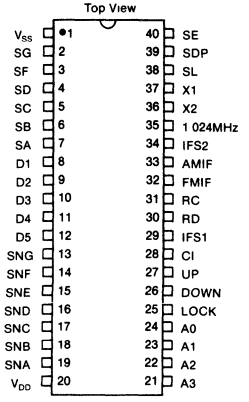
The AY-5-8105 is a PMOS integrated circuit containing a 39,999 count frequency synthesizer/counter for use in radio receivers Three main display ranges are provided: 39,999KHz for SW, 399.99MHz for FM and 9,999KHz for MW. FM frequencies can also be displayed in the standard European channel format (0 to 99+).

The timebase is provided by an on-chip oscillator using a 4.096MHz quartz crystal A 50Hz output derived from this oscillator is available to serve as the timebase for an AY-5-1200A digital clock which can share the same display.

Digit and segment outputs have high voltage capability and will drive fluorescent displays.

The AY-5-8105 is configured to work in conjunction with the PIC1650 family of controllers The bidirectional SERIAL LINK provides the path for data exchange between the two devices to form a synthesized frequency-locked radio tuning system.

PIN CONFIGURATION



TUNING

OPERATION

AY-5-8105 Synthesizer Under PIC1650 Control

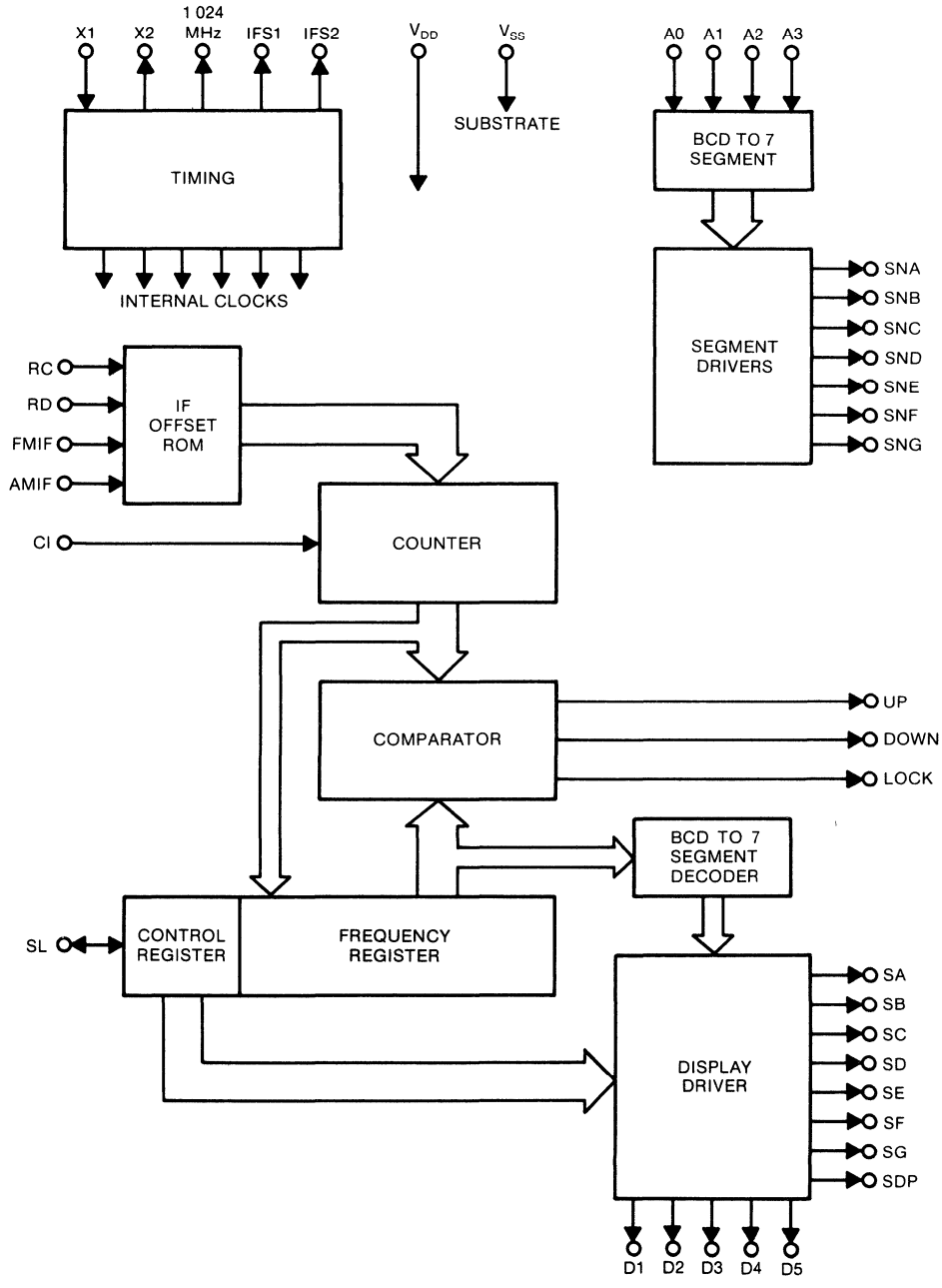


Fig. 1 AY-5-8105 BLOCK DIAGRAM

TUNING

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any Pin with Respect to V_{SS} pin (except Segment and Digit outputs) ..... +0.3 to −20V
Voltage on Segment and Digit outputs with Respect to V_{SS} pin ..... +0.3V to −35V
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation — 40 pin package 800mW

*Exceeding these ratings could cause permanent damage to these devices. This is a stress rating only and functional operation of these devices at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

$V_{SS} = 0V$
$V_{DD} = -12V \pm 1.2V$
Operating Temperature range = 0°C to +70°C
Crystal frequency = 4.096MHz ± 0.01%

Characteristic	Min	Max	Units	Conditions
All Inputs				
Capacitance	—	15	pf	at 1MHz
CI (Note 1)				
Input Frequency	0.05	2	MHz	
Input Pulse Width (High or Low)	2	—	ns	
Input Low	V_{DD}	−4	V	
Input High	−1	V_{SS}	V	
Input Source Current	— 0.15	3 —	mA mA	$V_{IN} = -4.9V$ $V_{IN} = -1V$
AM IF, FM IF (Note 2)				
Input Low	V_{DD}	−4	V	
Input High	−1.2	V_{SS}	V	
Input Sink Current	— 30	0.3 —	mA μA	$V_{IN} = V_{SS}$ $V_{IN} = -5.4V$
A0-A3, RC, RD (Note 1)				
Input Low	V_{DD}	−4	V	
Input High	−1	V_{SS}	V	
Input Source Current	— 20	0.3 —	mA μA	$V_{IN} = V_{DD}$ $V_{IN} = -1V$
SL (as input) (Note 1)				
Input Low	V_{DD}	−4	V	
Input High	−1	V_{SS}	—	
Input Source Current	— 50	2.5 —	mA μA	$V_{IN} = V_{DD}$ $V_{IN} = -1V$
SL (as output) (Note 3)				
High Voltage	−2	V_{SS}	V	$I_{SOURCE} = 0.2mA$
Off Current (Leakage)	—	10	μA	$V_{OUT} = V_{DD}$
1.024MHz, UP, DOWN (Note 3) **LOCK**				
High Voltage	−2	V_{SS}	V	$I_{SOURCE} = 1mA$
Off Current (Leakage)	—	2	μA	$V_{OUT} = V_{SS} - 5V$
IFS1 (Note 3)				
High Voltage	−0.5	V_{SS}	V	$I_{SOURCE} = 3mA$
Off Current (Leakage)	—	10	μA	$V_{OUT} = V_{DD}$
IFS2 (Note 3)				
High Voltage	−0.5	V_{SS}	V	$I_{SOURCE} = 0.5mA$
Low Voltage	V_{DD}	−8.5	V	$I_{SINK} = 0.1mA$
Segment Outputs (Note 4)				
High Voltage	−2	V_{SS}	V	$I_{SOURCE} = 2mA$
Off Current (Leakage)	—	10	μA	$V_{OUT} = -33V$
Digit Outputs D2-5 (D1) (Note 4)				
High Voltage	−3	V_{SS}	V	$I_{SOURCE} = 7mA$ (14mA)
Off Current (Leakage)	—	10	μA	$V_{OUT} = -33V$
Supply Current	—	40	mA	$V_{DD} = -13.2V$

NOTES:
1. These inputs have pull-ups to V_{SS}.
2. These inputs have pull-downs to V_{DD}.
3. These are open-drain outputs. Maximum applied negative voltage = 15V.
4. These are open-drain outputs. Maximum applied negative voltage = 33V.

TUNING

EAROM

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
512 BIT EAROM	512 bits organized 32 x 16.	ER2051	10-48
		ER2051 IR	10-48
		ER2051 HR	10-48

GENERAL INSTRUMENT

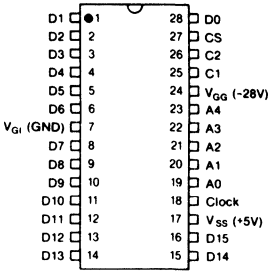
ER2051
ER2051IR
ER2051HR

512 Bit Electrically Alterable Read Only Memory

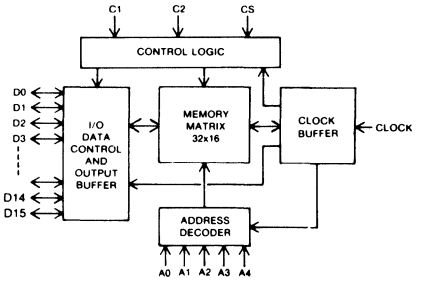
- 32 Word x 16 Bit Organization
- 5 Bit Binary Addressing
- +5, −28 V Power Supplies
- Word Alterable
- 10 Year Data Storage for ER2051 (at +70° C)
- 1 Year Data Storage for ER2051IR (at +85° C) and ER2051HR (at +125° C)
- TTL Compatibility with Pull-Up Resistors on Inputs
- Tri-State Outputs
- Read Time: 1μs (ER2051), 2μs (ER2051IR and ER2051HR)
- Write/Erase Time: 50ms (ER2051), 100ms (ER2051HR)
- No Voltage Switching Required
- Chip Select
- Two Extended Temperature Ranges;
  −40° C to +85° C ER2051IR
  −55° C to +125° C ER2051HR

PIN CONFIGURATION

28 LEAD DUAL IN LINE Top View



BLOCK DIAGRAM



DESCRIPTION

The ER2051, ER2051IR and ER2051HR are fully decoded 32 x 16 electrically erasable and reprogramable ROMs. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

The EAROM may be operated with the V_{SS} power supply between +5V and +10Volts, as long as the V_{SS}—V_{GG} always equals 33 Volts. Thus, V_{SS} can be +5Volts for TTL compatibility or up to +10Volts for CMOS compatibility, if V_{GG} is appropriately adjusted.

The ER2051IR and ER2051HR are screened to Mil Std. 883B/ method 5004.1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. They are available in 28 lead ceramic dual in line packages.

OPERATION

Data is stored in a two transistor memory cell After the cell is preconditioned by an erase signal (which causes a positive shift in the threshold of both transistors), data is written into one of the transistors making its threshold more negative. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending upon which transistor is written.

It is important to note two things. first, that an erase is required before a wire to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

The ER2051, ER2051IR and ER2051HR EAROM's use internal dynamic, edge triggered circuits. This requires either a mode change, a clock, or a transition of the chip select between successive operations. Thus successive operations in the same mode must be separated by transitions of one of these four lines. Clock pulses are not normally required during erase or write operations, but are needed for successive operations if the chip select is held high, i.e., applications where one EAROM is used.

PIN FUNCTIONS

Pin No	Name	Function
19, 20, 21, 22	A_0-A_4	5-Bit Word Address.
1-6, 8-14, 28	D_0-D_{15}	Data input and output pins.
27	CS	Chip Select. Chip selected at logic "1". When chip select is at logic "0", outputs are open circuit, read, write and erase are disabled. Power is reduced.
25, 26	C1, C2	Mode Control Inputs. C1 C2 0 1 Erase Mode: stored data is erased at addressed location. 1 Don't Care Read Mode: addressed data read after clock pulse. Output data retained at output pins until chip deselected or control lines switched. 0 0 Write Mode: input data written at addressed location. Clock not required.
18	CLK	Clock input. Pulse to logic "1" for read operation.
17	V_{SS}	Substrate supply. Normally at +5 volts.
7	V_{GI}	Ground Input.
24	V_{GG}	Power Supply Input. Normally at −28 volts.

TUNING

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Inputs and Outputs (with Respect to V_{SS}) ..... −35V to +0.3V
Storage Temperature ..... −65°C to +150°C
Soldering Temperature of Leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (for TTL compatibility)

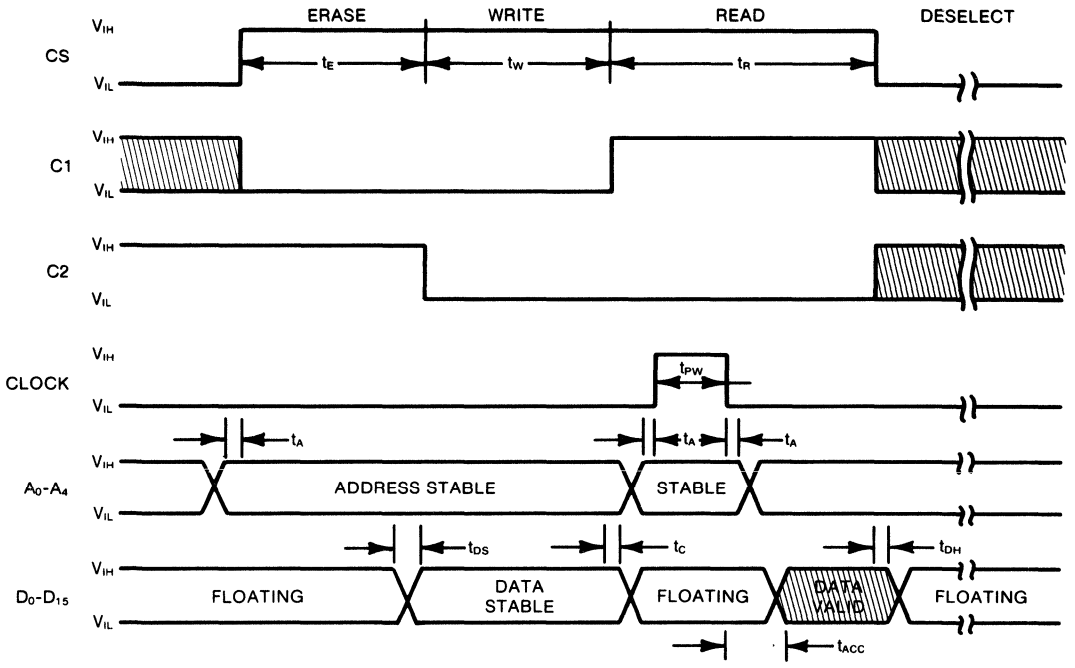
V_{SS} = +5V ±5%
V_{GG} = −28V ±5%
v_{GI} = GND
Operating Temperature T_A = 0°C to +70°C for ER2051
T_A = −40°C to +85°C for ER2051 IR
T_A = −55°C to +125°C for ER2051 HR
Output Load = 100pf, 1 TTL load

		ER2051			ER2051 IR/ER2051 HR				
Characteristics	**Sym**	**Min.**	**Typ.****	**Max.**	**Min.**	**Typ.****	**Max.**	**Units**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1.5	—	V_{SS} +0.3	V_{SS}−1.5	—	V_{SS} +0.3	V	
Input Logic "0"	V_{IL}	V_{SS} −15	—	0.8	V_{SS}−10	—	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} −1 5	—	—	V_{SS}−1.5	—	—	V	I_{OH} = 100μA
Output Logic "0"	V_{OL}	—	—	0.6	—	—	0.6	V	I_{OL} = 1.6mA for V_{SS} = +5V
Input Leakage	I_L	—	2	10	—	2	10	μA	V_{IN} = V_{SS} −15
Output Leakage	I_O	—	2	10	—	2	10	μA	Chip deselected
Power Supply Current									
Read	I_{GG}	—	—	14	—	—	18	mA	I_{GG} returned through V_{SS}
Write	I_{GG}	—	—	11	—	—	15	mA	
Erase	I_{GG}	—	—	11	—	—	15	mA	
Deselected	I_{GG}	—	—	9	—	—	12	mA	
AC CHARACTERISTICS									
Access Time	t_{ACC}	—	—	1	—	—	2	μs	
Clock Pulse Width	t_{PW}	2	—	20	2	—	20	μs	
Erase Cycle Time	t_E	50	—	200	100	—	200	ms	
Write Cycle Time	t_W	50	—	200	100	—	200	ms	
Read Cycle Time	t_R	3.5	—	24	4.5	—	25	μs	
Address to Clock Time	t_A	50	—	—	50	—	—	ns	
Data Set Up Time	t_{DS}	50	—	—	50	—	—	ns	
Data Hold Time	t_{DH}	50	—	—	50	—	—	ns	
Control to Address & Data Change	t_C	0	—	—	0	—	—	ns	
Number of Reads/Word Refresh	N_{RA}	10''	—	—	10''	—	—		
Number of Erase/Write Cycles	N_W	10^6	—	—	10^5	—	—	—	
Input Capacitance (all pins)	C_{IO}	—	8	15	—	8	15	pf	
Unpowered Data Storage Time	t_S	10	—	—	1	—	—	Years	at max temperature
Power Dissipation Read Cycle	P_D	—	450	500	—	450	500	mW	at 25°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	500	mW	at 125°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	600	mW	at −55°C V_{SS} = +5, V_{GG} = −29
Pulse Rise, Fall Time	t_{r_1} t_f	10	—	100	10	—	100	ns	

**Typical values are at +25°C and nominal voltages

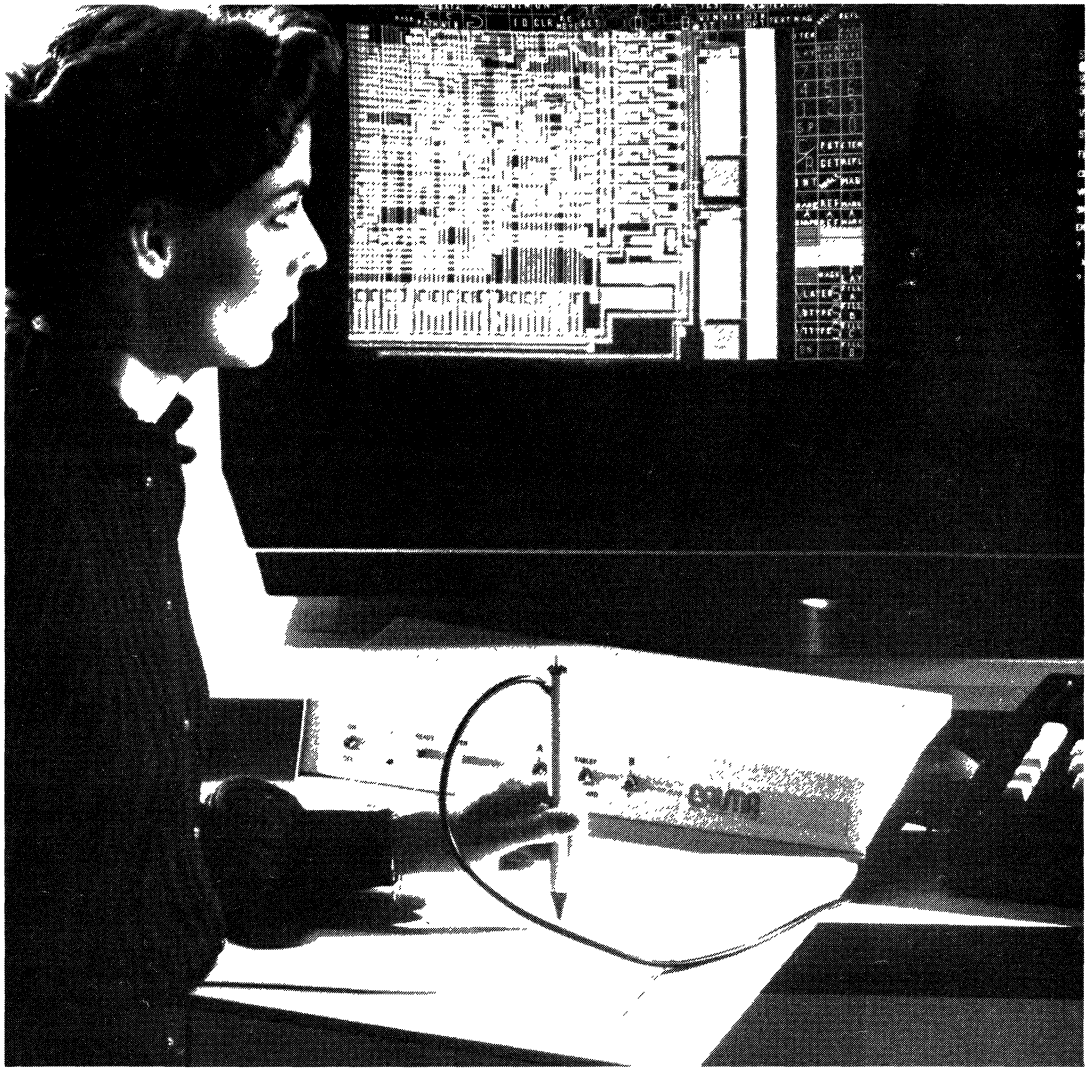
TUNING

TIMING DIAGRAM

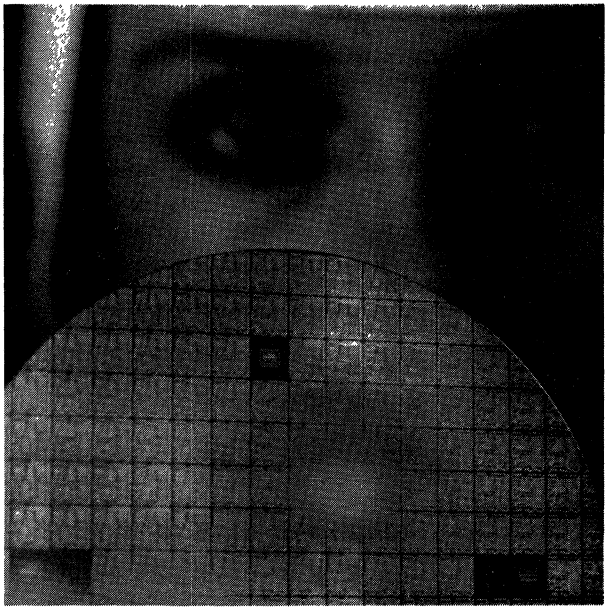


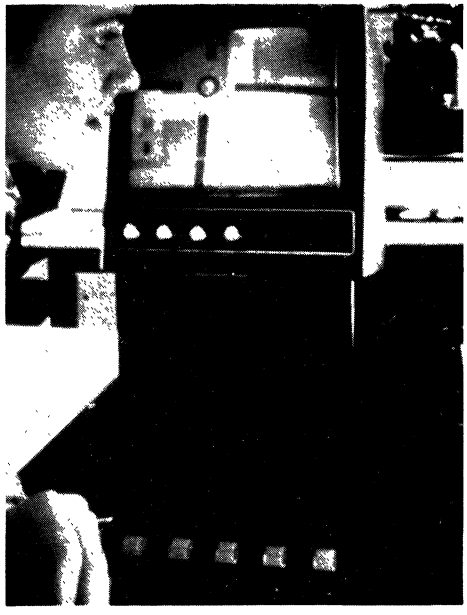
TUNING

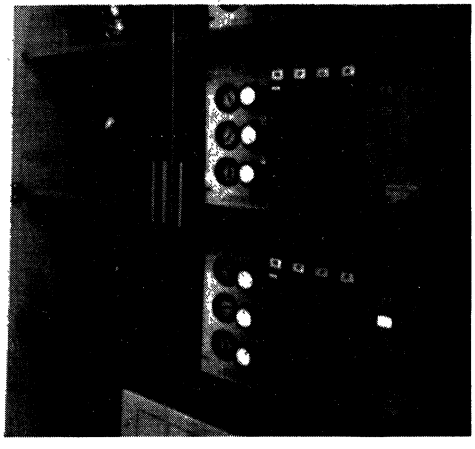
General Information 11



A Total Technological Service







A Total Technological Service

The Microelectronics Group of General Instrument Corporation is one of the world's leading manufacturers of LSI (Large Scale Integrated) microcircuits. A pioneer in MOS in 1966, General Instrument is a worldwide source of microcircuits utilizing MOS and Hybrid technologies in service to the consumer, communications, computer, industrial and military marketplaces.

The Microelectronics Group has facilities in every major market providing customers with a full spectrum of services including immediate delivery...new product development...applications engineering...and high volume circuit manufacturing.

Strategically Located Plants

The Microelectronics Group operates four main production facilities in the United States, Europe and Far East. Plants at Glenrothes, Scotland; Chandler, Arizona; and Hicksville, New York, have complete capability for product design, mask making, diffusion, assembly, test and quality assurance. The factory in Kaohsiung, Taiwan, is dedicated to high volume assembly, test, quality assurance and applications of Microelectronics products.

In addition to providing reliable sources of supply on three continents, General Instrument operates each plant as a backup facility to the others, to insure uninterrupted delivery. Common processes and equipment are employed and major product styles are always produced in at least two separate locations. To maintain uniform standards from plant to plant, the quality assurance and process control groups at each facility are directed by quality control policy established at Group and Corporate levels.

Processes

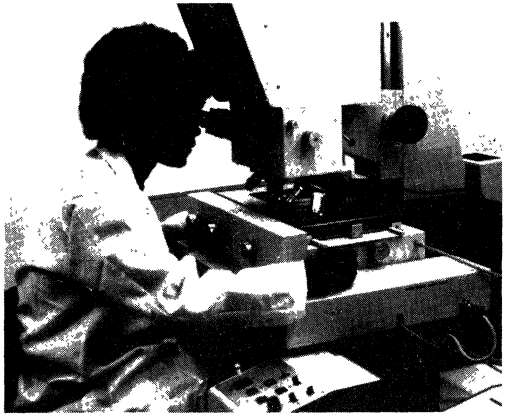
Products produced by the Microelectronics Division are in accordance with technologies that are standard to the Microelectronics industry. Production capability exists for CMOS Silicon Gate, N-Channel Silicon Gate, CMOS Metal Gate, N-Channel Metal Gate, and P-Channel Metal Gate. In addition, General Instrument is the world's leading manufacturer of products in the Non-Volatile Nitride Memory technology. This broad repertoire provides you, the customer, with the best process for the job every time.

Product Quality

With a major investment in product test and in-line quality control equipment, the Microelectronics Division of General Instrument is dedicated to achieving the reliability its customers require. All products receive final test at elevated temperature. Extensive burn-in facilities exist for 100% preshipment stress to insure outgoing product quality.

Customer Service

General Instrument Microelectronics believes in CUSTOMER SERVICE. Customer Service departments are maintained on a worldwide basis to provide immediate response to questions concerning order service and delivery. Our customer service personnel are trained to consider our customer's needs as their most urgent requirement. Call on them and let us prove that we are dedicated to responsive services.



Advanced Design Centers

To provide our customers with the latest in LSI technology, General Instrument Microelectronics maintains R&D centers at Glenrothes, Scotland; Hicksville, New York; and Chandler, Arizona. The Microelectronics activity is also supported by general research in various fields carried out with such prestigious organizations as the Massachusetts Institute of Technology, the State University of New York at Stony Brook and the University of Utah.

In addition to its extensive catalog of standard products, General Instrument Microelectronics is happy to provide custom design services to satisfy special requirements. In some cases, the application is best served by a software or firmware modification of one of our standard microprocessors. In other cases, a programable logic array is more cost effective. These services may be arranged through any of the Microelectronics sales offices.

Applications Assistance Around the Globe

To provide the special applications assistance that customers may require, General Instrument Microelectronics maintains fully staffed Applications Centers at strategic locations around the world...

U.S.A. — Hicksville, New York and Los Angeles, California.

EUROPE — Glenrothes, Scotland; London, England; Paris, France; and Munich, Germany.

ASIA — Tokyo, Japan; and Hong Kong.

Arrangements can be made for immediate assistance from these centers by contacting any of the sales offices listed in this catalog.

Corporate Support

General Instrument Microelectronics is backed by the full resources of the General Instrument Corporation, which has for over 50 years been among the leaders in the application of modern technology to entertainment, industrial, military, data and communications electronics. The skills, production know-how, and technological capability of the entire General Instrument organization are utilized by the Microelectronics Group to further improve its products and customer services.

Among the many other electronic components manufactured by General Instrument are discrete semiconductors, relays, miniature lamps, and TV components. General Instrument is a leading manufacturer of cable TV products, off-track and on-track wagering systems, point-of-sale equipment and apparatus for defense applications.

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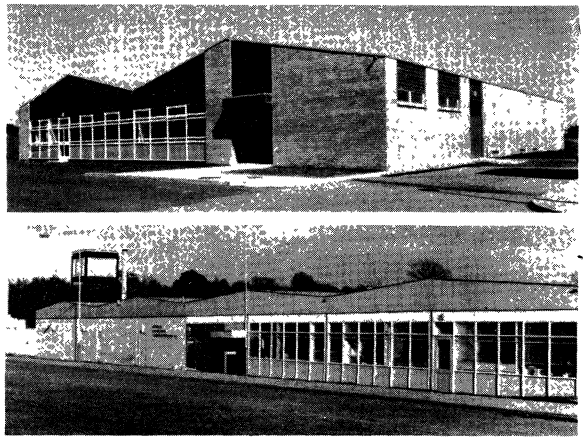

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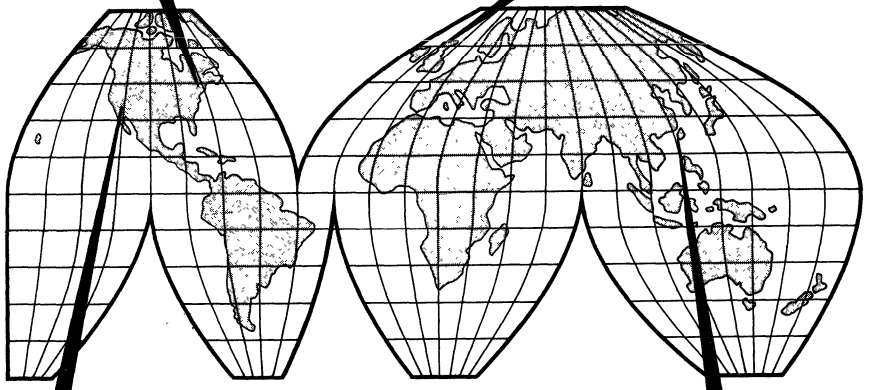

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KAOHSIUNG, TAIWAN

GENERAL INFORMATION

Package Outlines

PACKAGE OUTLINES

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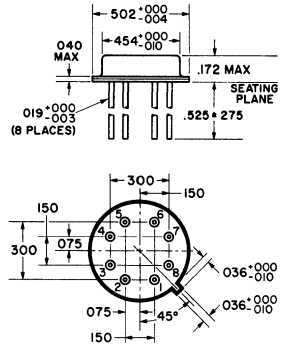

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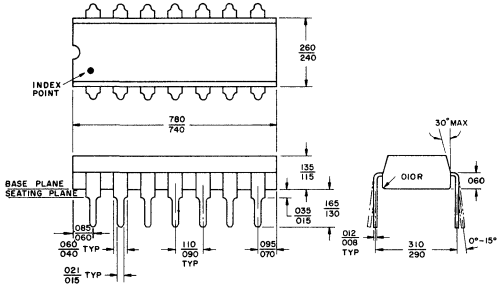

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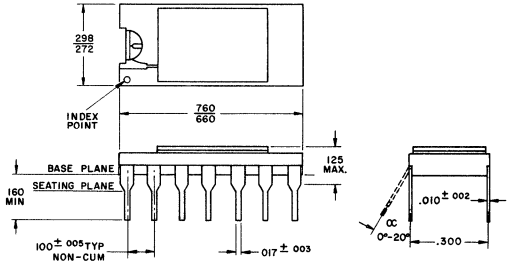

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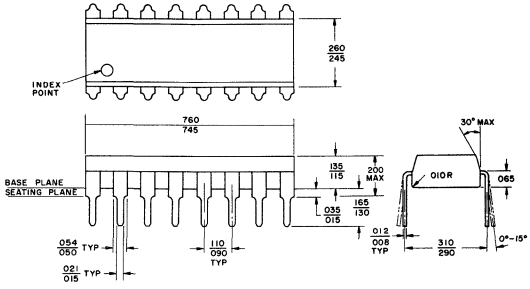

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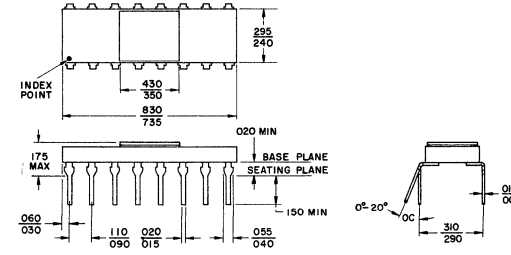

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GENERAL INFORMATION

PACKAGE OUTLINES

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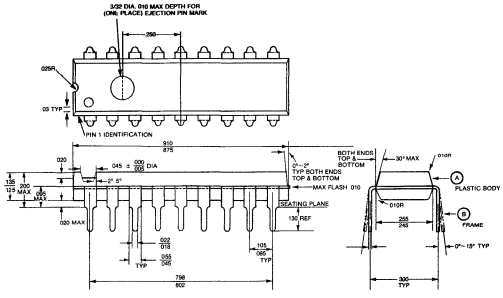

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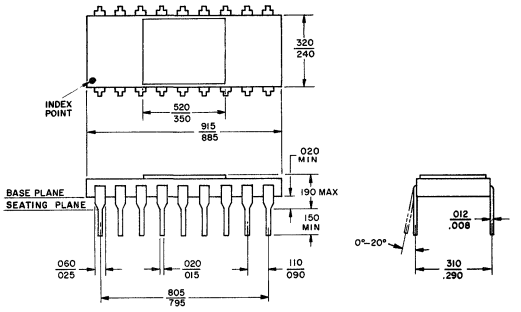

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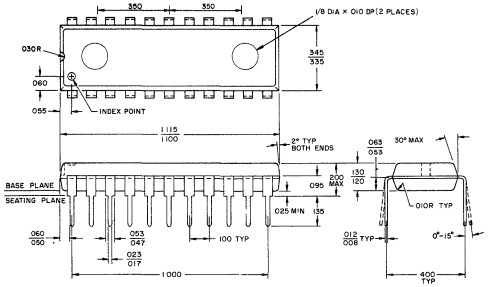

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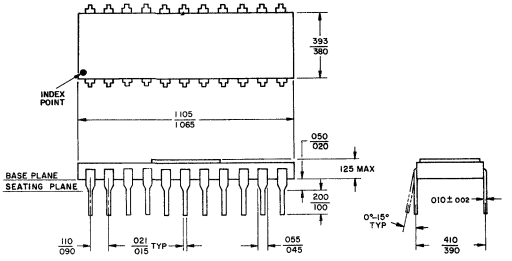

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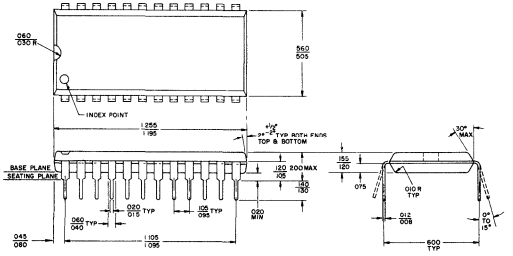

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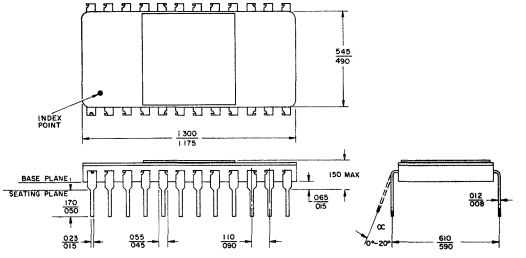

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GENERAL INFORMATION

Package Outlines

PACKAGE OUTLINES

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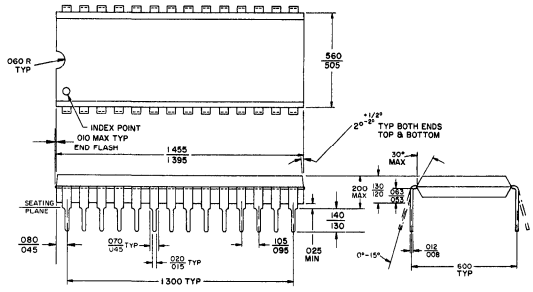

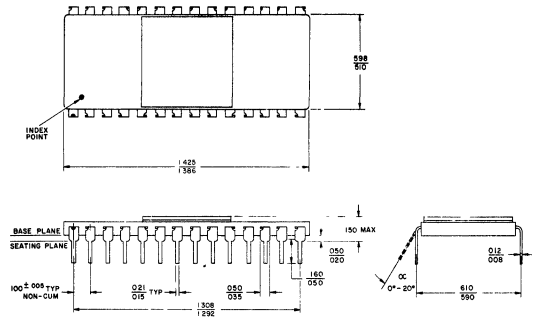

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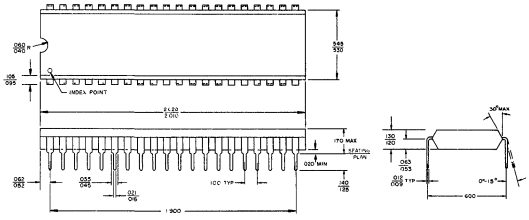

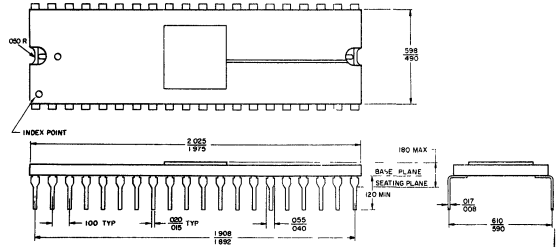

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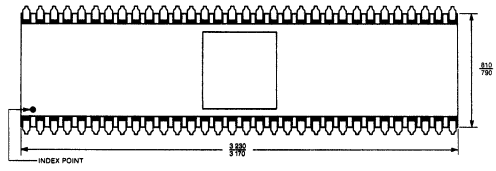

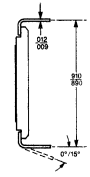

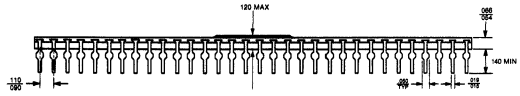

CERAMIC

GENERAL INFORMATION

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Tel: 03455-3150
Telex: 40259

Vekano
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1950 Kraaynem
Tel: 720 9204
Telex: 21923

DENMARK
A/S Nordisk—Elektronik
Transformervej 17
DK-2730 Herlev
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Telex: 35200

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SF-02101 Espoo 10
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Telex: 270191

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c/, Castello, n.25, 2° D
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P.O. Box 2101
183 02 Taby
Tel: 468 768 0560
Telex: 10912

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Fellenbergerstrasse 281
CH-8047 Zurich
Tel: 01 54 11 00
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Elbatex AG
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Keighley, W. Yorks
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Pass Street
Werneth, Oldham Lancs,
Tel: 061-652 6316
Telex: 668250

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Campbell Collins Ltd.,
162 High Street
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Telex: 825610

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Gothic Crellon Ltd.
380 Bath Road
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Tel: 06286 4434
Telex: 847571

West Drayton
Semiconductor Specialists Ltd.
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159 High Street, Yiewsley
West Drayton, Middlesex
Tel: West Drayton 45522
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Telex: 34439

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Transvaal
Pace Electronic Components (Pty.) Ltd.
P.O. 701
Isando 1600, Transvaal
Tel: (011) 361213
Telex: 83196

TERMS OF SALE

1. FORMATION OF CONTRACT. Any term of Buyer's order or of releases pertaining thereto or in any communication from Buyer, which is in any way inconsistent with or in addition to these Terms of Sale, shall not be applicable hereto or binding upon Seller Buyer's failure to object to any of these Terms of Sale in writing prior to the commencement of performance by Seller or the acceptance of any of the goods or services described on the front hereof (the "items") shall be conclusively deemed to be acceptance of all these Terms of Sale (without regard to whether Buyer makes or may make any inspection with respect to such items) Seller's failure to object to terms contained in any communication from Buyer shall not be deemed to be a waiver of these Terms of Sale

2. PRICES. Prices are F O B Seller's plant, unless otherwise specified on the front hereof Prices do not include any taxes or duties, now or hereafter enacted, applicable to the items or to this transaction, all of which taxes and duties shall be Buyer's responsibility Such taxes and duties shall be added by Seller to the sales price hereunder, where appropriate

3. PAYMENT TERMS. If Seller extends credit to Buyer, terms of payment will be net thirty (30) days after date of invoice After the due date, the lesser of one and one-half (1½%) percent of the unpaid balance (annual rate of 18%) or the maximum late payment penalty charge permitted by law will be added for each month or part thereof that payment is delayed Seller has the right, at any time, to change the amount of credit or terms of payment or to withdraw credit, and to require partial or full payment in advance as a condition of making further shipments If Seller delivers in installments, each installment shall be deemed to be a separate delivery for purposes of this paragraph Payment shall be made without regard to whether Buyer has made or may make any inspection or tests Anything herein to the contrary notwithstanding, if shipments are delayed at Buyer's request, payments shall be due on the date Seller is prepared to make shipments Goods held thereafter by Seller or carrier for Buyer shall be at Buyer's sole risk and expense.

4. RISK OF LOSS AND SHIPMENT; TITLE. Liability for loss or damage passes to Buyer when Seller puts the goods into possession of a carrier for shipment to Buyer (the carrier being deemed to be acting as Buyer's agent) Seller has the right to ship in installments Shipping dates are approximate only Seller shall not be liable for any loss or expense (consequential or otherwise) incurred by Buyer if Seller fails to meet such dates for any reason, including, but not limited to, the contingencies stated in paragraph 7 hereof or any other unavoidable production delays, delays in prompt approval of samples by Buyer, modification of specifications previously agreed upon or delays in submission of specifications acceptable to Seller Delays in shipment, non-conformity or non-shipment of an installment shall not relieve Buyer of its obligations hereunder with respect to any other installments, each installment being deemed to be a separate contract Buyer hereby authorizes Seller to produce all or substantially all of the total quantity of any product set forth on the front hereof in advance of the estimate shipment date(s) and hold for shipment in accordance with such date(s) Unless specified on the front hereof, Seller shall select the mode of transportation and the carrier All right, title and interest in and to all items covered by Buyer's order are reserved to Seller until the full purchase price for all such items has been paid Buyer hereby authorizes Seller to execute and file, at any time or times, one or more financing statements with respect to such items, signed only by Seller

5. INSPECTION AND ACCEPTANCE. The electrical performance specifications for the product shall be in accord with the Seller's customer procurement specifications referenced on the front hereof or in lieu thereof, Seller's published data sheet The Buyer shall inspect and accept the products within three weeks of date of Buyer's receipt or six weeks from the date of the Seller's shipment, whichever is the shorter period Any claim for goods nonconforming to conditions of inspection must be made in writing within this period Seller has the right to examine at Buyer's premises any items the Buyer claims are nonconforming Seller has the right to impose a rescreening charge of not less than 25¢ per unit if shipments returned to the Seller are found to be within a 65% inspection level. Repairs that are the Seller's responsibility may, at Seller's election, be made at Buyer's premises

6. QUANTITIES. Any variation in quantities shipped over or under the quantities ordered (not to exceed 5% for standard products or 10% for custom and custom-patterned products) shall constitute compliance with Buyer's order and the unit price shall continue to apply All claims for shortages in excess of such variations shall be made within ten (10) days after date of receipt of shipment

7. CONTINGENCIES. Seller shall not be liable for any delay in performance or for non-performance, in whole or in part, caused by a labor dispute or the occurrence of any contingency beyond the reasonable control either of Seller or Seller's suppliers, including, but not limited to, war (whether an actual declaration thereof is made or not), sabotage, insurrection, riot or other act of civil disobedience, act of a public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof affecting the terms of this contract or otherwise, judicial action, accident, fire, explosion, flood, storm or other act of God, shortage of labor, fuel, raw materials, tools, dies, or equipment, or technical or yield failure Any such delays shall excuse Seller from performance, and Seller's time for performance shall be extended, for the period of the delays and for a reasonable period thereafter If any contingency occurs, Seller may allocate production and deliveries among any or all of Seller's customers as Seller may determine, including, without limitation, regular customers not then under contract and Seller's (including Seller's subsidiaries' and affiliates') own requirements for further manufacture or other use

8. SUBSTITUTION AND MODIFICATION OF GOODS. Seller has the right to modify the specifications of goods designed by Seller and substitute substantially equivalent goods manufactured to such modified specifications

9. WARRANTIES. Seller, except as otherwise herein provided, warrants that the goods shall be free from defects in materials and workmanship (under normal use and services) from the earlier of a) date of invoice or b) date code indicated on the goods for the following periods

A Packaged LSI Devices - 1 year

B Processed Semiconductor chips - 30 days

Seller's warranties shall not extend to any items subjected to accident, misuse, neglect, alteration, improper installation, improper testing or unauthorized repair

Seller makes NO WARRANTY as to experimental or developmental goods or goods not manufactured by Seller As to goods not manufactured by Seller, at Buyer's request, Seller, to the extent permitted by Seller's contract with its supplier, shall assign to Buyer any rights Seller may have under any warranty of the supplier thereof

Seller's warranties extend to the Buyer and to no other person or entity

Seller's warranties as hereinabove set forth shall not be enlarged, diminished or affected by, and no obligation or liability shall arise or grow out of, Seller's rendering of technical advice or service in connection with Buyer's order of the goods furnished hereunder

The foregoing are in lieu of all warranties, express, implied or statutory, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose and any other warranty obligation on the part of the Seller.

10. PROPRIETARY RIGHTS AND CONFIDENTIALITY.

(a) All information, know-how, programming, software, trademarks, trade secrets, plans, drawings, specifications, designs and patterns furnished or created by Seller or by Seller's agents or contractors (other than Buyer) and any and all property rights embodied therein are and shall remain the sole property of Seller and neither Buyer nor any other party shall have or acquire any interest therein

(b) Buyer recognizes and acknowledges that certain confidential, secret or proprietary information possessed by Seller ("Information") is a valuable business asset of Seller and that disclosure of the Information would cause grave and irreparable injury to Seller Buyer shall at all times, whether during the term of this contract or subsequent thereto, honor, maintain and protect the confidentiality and secrecy of such of the Information as Seller may disclose to Buyer or its agents Buyer shall not make any copies of any of the Information without prior written consent of Seller and will take appropriate action to restrict access to the Information to those of its employees and agents who have an actual need for such access in the course of their duties This provision shall survive the performance, termination or cancellation of this contract

11. TOOLING. Unless otherwise expressly provided, Seller will retain title to, possession of, and the right to exclusive use of, all jigs, dies, fixtures, molds, patterns, gauges, taps, equipment, manufacturing aids and similar devices, made or obtained for the performance of this contract, without regard to whether a separate charge is made for the same

12. PATENT INDEMNITY. Seller will defend any suit or proceeding brought against Buyer to the extent that such suit or proceeding is based on a claim that goods manufactured and sold by Seller to Buyer constitute a direct infringement of any valid United States patent and Seller shall pay all damages and costs awarded by final judgment (from which no appeal may be taken) against Buyer, on condition that Seller (i) is promptly informed and furnished a copy of each communication, notice or other action relating to the alleged infringement, (ii) is given authority, information and assistance necessary to defend or settle such suit or proceeding in such manner as Seller shall determine, and (iii) is given sole control of the defense (including the right to select counsel), and the sole right to compromise and settle such suit or proceeding Seller shall not be obligated to defend or be liable for costs and damages if the infringement arises out of compliance with Buyer's design or specifications or from a combination with, an addition to, or modification of the goods after delivery by Seller, or from use of the goods, or any part thereof, in the practice of a process No license, express or implied, is granted under any United States or foreign patent covering the goods manufactured and delivered by Seller, or from the use of the goods or any part thereof, in the practice of a process

If any goods manufactured and supplied by Seller to Buyer are held to directly infringe any valid United States patent and Buyer is enjoined from using the same, or if Seller believes such infringement is likely, Seller will exert reasonable efforts, at its option and at its expense, (i) to procure for Buyer the right to use such goods free of any liability for patent infringement, or (ii) to replace (or modify) such goods with a non-infringing substitute otherwise complying substantially with all the requirements of the contract, or (iii) upon return of the goods, refund the purchase price and the transportation costs of such goods If the infringement is alleged prior to completion of delivery of the goods, Seller has the right to decline to make further shipments without being in breach of contract. If Seller has not been enjoined from selling such goods to Buyer, Seller may (at Seller's sole election), at Buyer's request, supply such goods to Buyer, in which event Buyer shall be deemed to extend to Seller the same patent indemnity hereinabove stated

The same patent indemnity shall be deemed to be extended to Seller by Buyer if any suit or proceeding is brought against Seller based on a claim that the goods manufactured by Seller in compliance with Buyer's specifications infringe any valid United States patent.

The foregoing states the sole and exclusive liability of the parties hereto for infringement or the like of patents, trademarks and copyrights, whether direct or contributory, and is in lieu of all warranties, express, implied or statutory in regard thereto, including, without limitation, the warranty against infringement specified in the Uniform Commercial Code.

13. SOFTWARE INDEMNIFICATION AND DISCLAIMER.

(a) In the event any software used by Seller in the products shown on the front hereof is furnished or created by someone other than Seller, Buyer shall indemnify and hold Seller harmless from and against any and all loss, claim, damages, liability, cost, expense (including reasonable attorneys' fees) and any causes of action whatsoever, arising out of or in connection with claims by third parties of any description or nature concerning any such software, including, but not limited to, a claim that such software is owned by a third party

(b) Seller hereby disclaims any and all liability for any claims or damages of any description or nature arising from (1) the unknowing duplication or use of Buyer's software, in whole or in part, in products manufactured by Seller for others, or (2) alleged error in any software furnished or created by (i) any person other than Seller or (ii) Seller if Buyer has approved such software

14. TERMINATION. Except as provided in paragraph 15(a) this contract may not be terminated by Buyer without Seller's prior written consent If Seller so consents to such termination, Buyer shall be liable for termination charges including, without limitation, a price adjustment based on the quantity of goods actually delivered and all costs, direct and indirect, incurred and committed for this contract together with reasonable allowance for prorated expenses and anticipated profits

15. REMEDIES AND DAMAGES.

(a) Where Buyer rightfully and timely rejects or justifiably revokes acceptance of items, or where Buyer has accepted nonconforming items and has timely notified Seller of a breach of warranty, Seller's sole and exclusive liability will be (at Seller's option) to repair, replace or credit Buyer's account with respect to any nonconforming goods returned to Seller during the applicable warranty period set forth above, and with respect to any nonconforming services, on condition that (i) Seller is, promptly upon Buyer's discovery of the nonconformity, notified in writing with a detailed explanation, (ii) Seller issues a Return Material Authorization (RMA) number for return of goods, F O B Seller's designated plant, such RMA shall be effective for 60 days from issuance date, and (iii) Seller's examination discloses that such items are nonconforming

Where Seller fails to make shipment or repudiates or breaches any other material provisions of this contract (other than the warranty against patent infringements), including, without limitation, Seller's obligations with respect to nonconforming items, Buyer shall promptly give written notice to Seller. In the event that Seller does not cure any such failure to ship, repudiation or breach within 60 days after receipt of such notice, then Buyer shall have the right, at its option, to cancel the specific quantity of goods not shipped, or terminate this contract as to the items as to which such repudiation or breach related, and that shall be Buyer's sole and exclusive remedy. If Buyer desires to exercise such right of cancellation or termination it shall give further written notice to Seller.

Except as set forth above, in no event will Seller be liable to anyone for direct, indirect, special, incidental or consequential damages for breach of any of the provisions of this contract, including, but not limited to, breach of provisions regarding warranties, indemnities and patent infringement. Such excluded damages include, without limitation, costs of removal and reinstallation of items, loss of goodwill, loss of profits and loss of use.

(b) Seller has the right to terminate this contract if, in Seller's sole judgement, Buyer's financial condition does not justify the terms of payment applicable from time to time, and upon demand Buyer does not immediately comply with any modification of payment terms required by Seller in accordance with paragraph 3

If Seller exercises such termination right, Buyer shall be liable for the charges referred to in paragraph 14 in addition to any other remedies Seller may have hereunder or at law

16. WAIVER. In the event of any default or breach by Buyer, Seller has the right to refuse to make further shipments Seller's failure to enforce at any time or for any period of time any of the provisions of this contract shall not constitute a waiver of such provisions or of the right of Seller to enforce each and every provision

17. GOVERNING LAW. The validity, construction and performance of this contract and the transactions to which it relates shall be governed by the laws of the State in which the chief executive offices of the Seller are located, without regard to conflict of laws principles All actions, claims or legal proceedings in any way pertaining to this contract or such transactions shall be commenced and maintained in the courts of such State or in a federal court of the United States physically situated in such State and in no other court or tribunal whatsoever, and the parties hereto each agree to submit themselves to the jurisdiction of such court

18. GOVERNMENT CONTRACTS. If the items to be furnished hereunder are to be used in the performance of a United States Government contract or subcontract and a United States Government contract number appears on Buyer's order or other written communication to Seller, those clauses of the applicable United States Government procurement regulation which are mandatorily required by federal statute to be included in United States Government subcontracts will be deemed incorporated herein by reference and will control if inconsistent with any provisions of this contract

19. ASSIGNMENT. This contract is binding upon and inures to the benefit of the parties hereto and the successors and assigns of the entire business and goodwill of either Seller or Buyer or that part of the business of either used in the performance of this contract, but will not be otherwise assignable except that Seller has the right to assign accounts receivable, or the proceeds of this contract Nothing in this contract shall inure to the benefit of or be deemed to give rise to any rights in any third party, whether by operation of law or otherwise

20. SEVERABILITY. If any of these Terms of Sale is declared invalid by a court, agency, commission or other tribunal or entity having jurisdiction thereof, the application of such provisions to parties or circumstances other than those as to which it is held invalid or unenforceable shall not be affected thereby, and each term not so declared invalid or unenforceable shall be valid and be enforced to the fullest extent permitted by law and the rights and obligations of the parties shall be construed and enforced as though a valid commercially reasonable term consistent with the undertakings of the parties under this contract had been substituted in place of the invalid provision

21. SET-OFF. Buyer may not set-off any amount owing from Seller to Buyer against any amount payable by Buyer to Seller, whether or not related to this contract

22. MERGER. This contract constitutes the final written expression of all terms of the agreement relating to the transactions described on the front hereof and a complete and exclusive statement of those terms. This contract supersedes all previous communications, representations, agreements, promises or statements, either oral or written, with respect to such transactions (including, without limitation, any terms proposed by Buyer) and no communications, representations, agreements, promises or statements of any kind made by any representative of Seller, which are not stated herein, shall be binding on Seller. No addition to or modification of any printed provision of this contract will be binding upon Seller unless made in writing (referring specifically to Buyer's order) and signed by an officer of Seller. No course of dealing or usage of trade or course of performance will be deemed relevant to explain or supplement any term expressed in this contract.

NOTES

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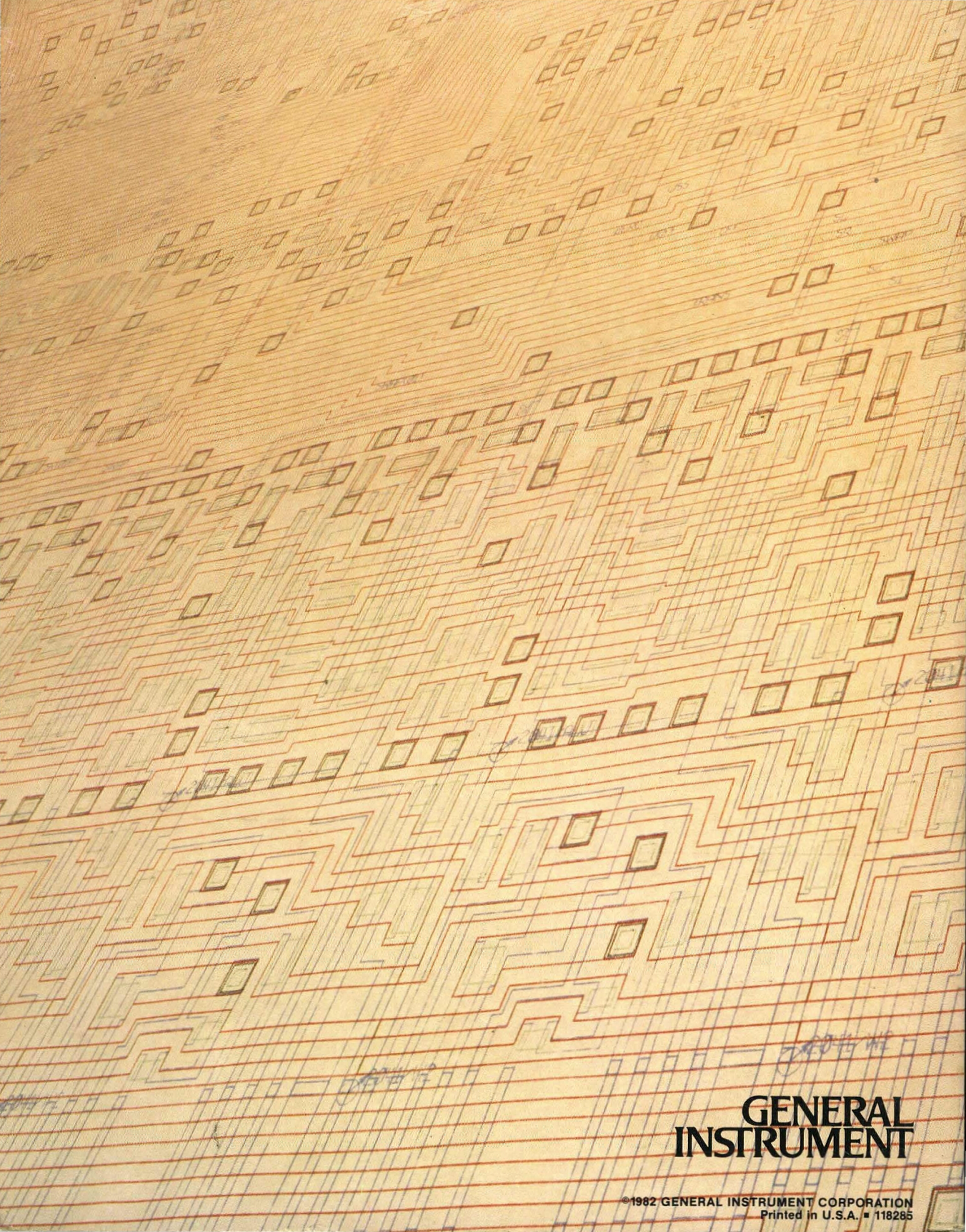

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